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Design And Implementation Of An X-Band Passive Rfid Tag

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Design and Implementation of an X-band Passive RFID Tag

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Biographical Sketch

Melaka Senadeera was born in Kandy, Sri Lanka, where he completed his elementary and secondary education at Kingswood College, Kandy. Melaka has received two Bachelor's degrees in Sri Lanka and USA of which the first one is in Physical Science from the University of Peradeniya, Sri Lanka obtained in 1998 and the second one is in Computer Science from Wright State University, Dayton, Ohio, USA obtained in 2001.

He earned his Master's degree in Electrical Engineering from Wright State University in 2005. While completing the Master's degree, Melaka worked in the capacities of a research assistant and a teaching assistant in Wright State University from 2002 to 2005. After obtaining his Master's degree in Electrical Engineering, Melaka worked as an Electrical Engineer at Tandon Lanka (Pvt) Ltd, Sri Lanka in 2005 and 2006. Subsequently Melaka returned to USA and worked as a Java/XML/XSL developer at Bearing Point, Fairfax, Virginia from 2007 to 2008 and at Perot Systems, Fairfax, Virginia from 2008 to 2009.

Melaka commenced his studies for a Ph.D. in Electrical Engineering at North Carolina A & T State University, Greensboro, North Carolina in 2009. Melaka received several scholarly awards at North Carolina A & T State University including the award for scholarly accomplishment and academic excellence by the International Students and Scholars Office (ISSO) consecutively from 2009 to 2012. He won the 2nd place in the graduate students poster competition held at the College of Engineering, North Carolina A & T State University in 2012. He has been a recipient of the Wadaran L. Kennedy 4.0 Scholars award granted by the School of Graduate Studies in 2009, 2010 and 2011. Melaka is also a member of the Institute of Electrical Engineers (IEEE) and Phi Kappa Phi honor Society. While working on his PhD program, Melaka

presented his findings in a number of national and international conferences. He has authored several scientific papers which remain published in IEEE.

After finishing his Ph.D. degree, Melaka intends to continue his career in research and teaching in mixed signal radio frequency systems.

Dedication

To my son Manuka, who has brought immense happiness and joy to my life in the last stages of writing the dissertation.

To my wife Madhavi, who provided me unending love, encouragement, support, and confidence making the task of completing the dissertation pleasant and rewarding.

To my parents who guided me from my infancy to appreciate the importance of learning.

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Table of Contents

List of Figures

List of Tables

Nomenclature

AC Alternative Current

AM Amplitude Modulation

ASK Amplitude Shift Keying

FCC Federal Communication Commission

IC Integrated Circuit

IF Intermediate Frequency

IIP2 Input 2nd order Intercept Point

IIP3 Input 3rd order Intercept Point

IM2 2nd order Inter-Modulation product

IM3 3rd order Inter-Modulation product

ITRS International Technology Roadmap for Semiconductors

ITU-R International Telecommunication Union – Radio-communications

KCL Kirchhoff's Current Law

KVL Kirchhoff's Voltage Law

LP Loop Filter

LPF Low Pass Filter

RFID Radio Frequency Identification

VCO Voltage Control Oscillator

Abstract

This research presents a novel fully integrated energy harvester, matching network, multi-stage RF-DC rectifier, mode selector, RC oscillator, LC oscillator, and X-band power amplifier implemented in IBM 0.18-µm RF CMOS technology. We investigated different matching schemes, antennas, and rectifiers with focus on the interaction between building blocks. Currently the power amplifier gives the maximum output power of 5.23 dBm at 9.1GHz. The entire RFID tag circuit was designed to operate in low power consumption. Voltage sensor circuit which generates the enable signal was designed to operate in very low current. All the test blocks of the RFID tag were tested. The smaller size and the cost of the RFID tag are critical for widespread adoption of the technology. The cost of the RFID tag can be lowered by implementing an on-chip antenna. We were able to develop, fabricate, and implement a fully integrated RFID tag in a smaller size (3 mm X 1.5 mm) than the existing tags. With further modifications, this could be used as a commercial low cost RFID tag.

CHAPTER 1

Introduction

The idea of Wireless Power Transmission (WPT) was first discovered in 1899 by Nikola Tesla. He attempted to distribute ten thousand horsepower under a voltage of one hundred million volts [1, 2]. In the work of Tesla, there was a need for energy transducer. At present for WPT work the energy conversion from RF to DC is realized based on a rectenna circuit. The rectenna was systematically studied in the second half of the twentieth century resulting in high overall efficiency systems. In the mid 1980's [3]Radio Frequency IDentification System (RFID) appeared in which electromagnetic coupling antenna was used for both power transmission and as a communication link.

RFID technology is one of the most rapidly growing technologies. RFID has a wide range of applications in areas such as automated data management, tracking of objects, manufacturing process, and highway toll collection [4-7]. RFID is a term that is often used for systems which transmits the identification (ID) of a certain object using the wireless technology. Barcode technology is widely used for identification purposes. The optical nature of the barcode requires labels are to be seen by lasers[8]. The line of sight between the label and the reader is often difficult and impractical in industrial environments. In order to work properly the barcode, the reader must have clean, clear optics and the label must be clean and free of scratch, and the reader and the label must be oriented with respect to each other. In addition the information on a barcode is fixed and cannot be changed. However the data on a RFID tag can be updated. More information can also be stored to the tag compared to the barcode strip. The main disadvantage of using barcode is low capacity and inability to be programmed although they are very inexpensive. A possible solution for the low capacity is to store the data on a chip. Therefore the

best solution would be the contactless data transfer between the device and the reader. This solution leads to the RFID technology. Unlike earlier barcode technology, RFID enables identification from a distance without the requirement of line of sight[9]. RFID systems can discern many different tags located in the same general area without human assistance. In contrast in a super market check-out counter, you must orient each bar-coded item toward a reader before scanning it[9]. RFID has many advantages like longer reading/writing distance, more complex data management, faster processing speed, robustness and reliability compared to the conventional bar-code system[10]. RFID systems have the ability to identify moving elements, large area of coverage and automatic integration with back end solutions which provides the end to end integration of data in real time.

RFID systems are more expensive compare to the barcodes. Also they are bulkier, due to the embedding of electronic components in the tag. In addition, the RFID system tags should be designed for specific applications because they are vulnerable to electrical and physical damages due to the environmental conditions.

1.1 Objective

The overall objective of this research is to design, develop, fabricate, and implement a low power fully integrated X-band passive RFID tag in a smaller size (3 mm X 1.5 mm) than the existing tags.

The specific objectives are

1. To develop energy harvester, matching network, a multi-stage RF-DC rectifier, mode selector, RC oscillator, LC oscillator, and X-band power amplifier implemented in IBM 0.18-µm RF CMOS technology.

2. To investigate different matching schemes, and rectifiers with focus on the interaction between building blocks.

1.2 Organization of the Dissertation

Chapter 1 contains the introduction and objective of this study. Chapter 2 reviews the literature on RFID Technology and Applications. It identifies the problem and discusses several approaches other researchers have taken to solve it. Chapter 3 presents the general overview of the proposed RFID system. The proposed passive RFID tag operating in the 5.8 GHz ISM band is explained in this chapter. Chapter 4 explains the design of the proposed X-band RFID tag which includes the details of the block level. Chapter 5 presents the design of the X-band antenna. Chapter 6 includes the experimental results and discussion of the designed and fabricated RFID tag. Chapter 7 summarizes the conclusions and suggestions for future work.

CHAPTER 2

RFID Technology and Applications

2.1 History of Radio-Frequency Identification

RFID work was first published in a paper by Harry Stockman, Communication by Means of Reflected Power, in 1948. The development of RFID started in 1960s. The British engaged RFID principals in world war II to identify their aircrafts using IFF (Identification friend or Foe) system[9]. The complete expansion of RFID came in 1970s and early 1980s. Mario W. Cardullo has received the first US patent for an active RFID tag with rewriteable memory on January 23, 1973[11, 12]. There was a great deal of attention to RFID by researchers, developers and academic institutions including Los Alamos Scientific Laboratory and the Swedish Microwave Institute Foundation[13]. It included RFID tags into employee badges to automatically identify people and limit the access to secure areas. Modern RFID was also used to identify animals, label airline luggage, and locate lost items. Wal-mart, Tesco, and US department of defense target to lower the operational costs by streamlining the tracking of stocks, sales, and orders with RFID based system. RFID can identify individual items as they move factories or warehouses when used in combination with computerized databases. The greatest interests in the United States were for transportation and personal access. Industrial and business applications were the interests in Europe. The period 1990-2000 was a significant decade in the development of RFID, because of the deployment of electronic toll collection in US and over three million RFID tags on rails and cars in North America. Compact RFID tags were built using two components such as single custom CMOS integrated circuit and an antenna. The size of the tag is mainly limited by the constraints of the antenna. The two main challenges of the development of RFID were the

design of suitable antennas and the search for better nonvolatile memory. The small size and cost of the RFID tag are critical factors for adoption of the RFID technology[14]

2.2 RFID Operation

The basic operation of an RFID system is data transfer between a reader and a tag as shown in Fig.2.1(wireless communication).

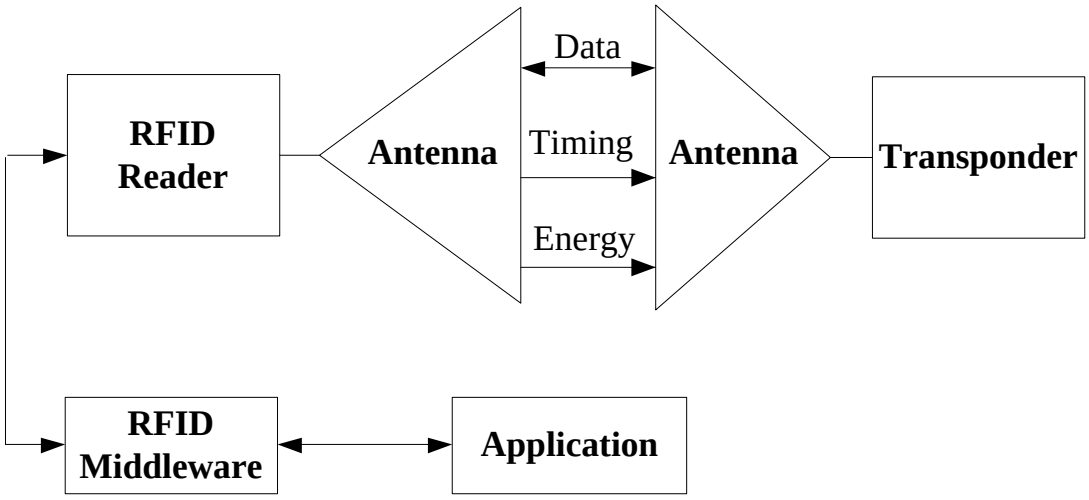


Figure 2.1 RFID system operation

The communication between the reader and the tag depends on the application requirements such as the cost, size, speed, and read range and accuracy. There are two fundamentally different approaches exist for transferring data from reader to tag. They are either magnetic induction or electromagnetic(EM) wave capture. Inductively coupled RFID systems have a short range compared to RFID systems that have electromagnetic coupling. A very important parameter in the operation of an RFID is the frequency of operation between the reader and the tag. Specific frequency selection is determined by the application requirements

such as speed, accuracy, environmental conditions, and standards and regulations of specific applications.

2.3 RFID Technology

A typical RFID system consists of tags, readers, transmitting and receiving antenna and a communication method.

2.3.1 Tag

The tag is also known as the transponder. It is a small object that can be attached to or incorporate into a product, animal or person. For example tags can be attached to insects to track their movements and habits. Tags contain antennas to allow them to receive and respond to radio frequency queries from an RFID reader or interrogator [12, 15]. When the tag is interrogated by the reader, tag sends the unique ID and data to the reader for processing [12]. The most common tags consist of an integrated circuit (IC) that includes digital and analog circuits such as memory, RF to DC rectifier, modulators, oscillators, and amplifiers. An RFID tag is shown in Figure 2.2

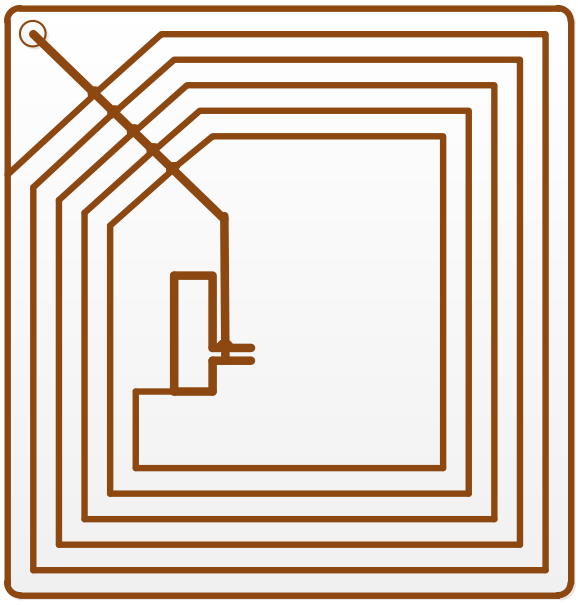


Figure 2.2 RFID Tag

When the tag is interrogated the data stored in its memory is transmitted to the reader. The tag memory can be read only (RO), write once-read many(WORM), or read/write(RW). The tag has an identity (ID) that can be broadcast to a reader that is operating on the same frequency. RFID tags can be divided into four categories; (i) active tags (battery-powered), (ii) semi-active tags, (iii) semi-passive tags (battery-assisted), and (iv) passive tags (battery-free)[4].

i. Active tag

Active tags require a power supply. They are either connected to a powered infrastructure or use energy stored in a battery[9]. It supports longer communication distance and can supply power to sensors as sensor enabled RFID system. The active tags have power supply embedded in them. Therefore active tags have the ability to respond to a weak signal from the reader. The active tag can communicate long distances because it has a dedicated power supply. At present, the smallest active transponders are about the size of a coin[15]. However active tags have several disadvantages, such as short battery life, the number of read operations, large volume, and high cost [9, 16-18]. One example of an active tag, is the transponder attached to an aircraft that identifies its national origin. The active tags are impractical for the retail trade because of their cost, size, and lifetime of the battery.

ii. Semi-active tag

The semi active tag has a small battery which keeps the microchip alert which makes faster tag response. This type of tag is powered by an internal battery to run the microchip's circuitry and to broadcast a signal to the reader.

iii. Semi-passive tag

The semi-passive tag, also known as a Battery Assisted Passive (BAP) tag can provide a greater reading range and readability than passive tags. The battery in the BAP tag runs the microchip's circuitry and reflects the radio waves generated by the reader. A non-BAP tag uses some of the readers signal to power its microchip and a BAP tag reflects back more of the reader's radio waves.

Passive tags are downlink limited to power constraints. In semi passive tag the battery eliminates the power constraints and then become uplink due to finite reader sensitivity. Semi passive tags also communicate using backscatter modulation like passive tags.

iv. Passive tag

Passive RFID is of interest because the tags don't require batteries or maintenance[9]. These tags also have indefinite operational life. Compared to active tags they are small enough to fit into a practical adhesive label. These tags are powered by the RFID reader. These tags can be produced at very low cost because they require no battery power [19]. When the tag is within the radio frequency field, the reader sends electromagnetic waves which power the microchip on the tag. Once the power of the microchip meets the minimum voltage, the microchip can send back information on the same wave. Passive tag can communicate with the reader without a battery by using the transmitted power from the reader (RF to DC rectifier). Passive tag consists of three parts: an antenna, semiconductor chip attached to the antenna, and some method of encapsulation. The tag antenna captures the energy and transfers the tag's ID. The encapsulation maintains the tag's reliability and protects antenna from environmental conditions.

Passive tags are much cheaper to manufacture because they do not depend on a battery. Passive tags (chip and antenna mounted on a substrate) average cost is 7 to 15 US cents in comparison to active tags cost $25 dollars.[14]

Due to the limited power, the response of a passive RFID transponder is brief: typically just an ID number.

Table 2.1 *Characterization of Active and Passive RFID Tags*

	Active RFID	**Passive RFID**
Tag power source	Internal to tag	Energy transferred from the reader via RF
Tag battery	Yes	No
Availability of tag power	Continuous	Only within field of reader
Communication range	Long range(100m)	Short range(up to 15m)
Data storage	Large read/write data storage	Small read/write data storage

2.3.2 Reader

RFID reader, also referred to as the interrogator is a device that can read data from and write data to compatible RFID tag. RFID reader is also responsible for interfacing with a host computer. A RFID reader is shown in Figure 2.3 In case of passive and semi-active tags the reader provides the energy to activate or energize the tag in the reader's electromagnetic field. The reach of the field is determined by the size of the antenna in both sides and power of the reader.

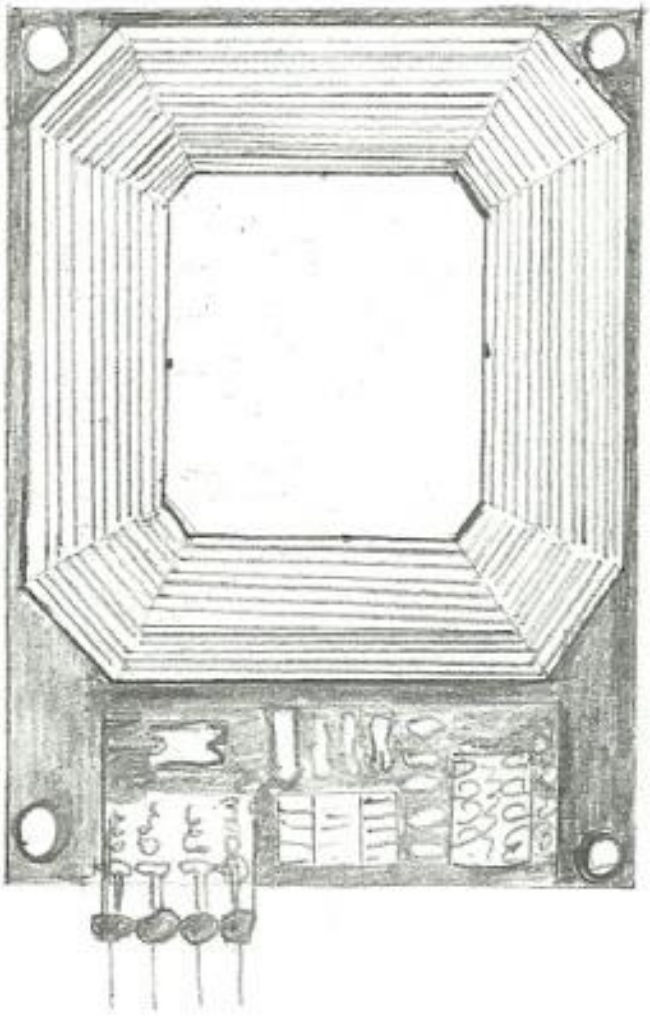


Figure 2.3 RFID Reader

Communication between tag and reader enables the location information of an item to be recorded and transferred to a server through a computer network, thus allowing the movement of the item to be tracked and traced. Handheld, vehicle-mounted, post-mounted and hybrid are the four types of RFID readers. The first three types are used to read either passive or active tags.

2.3.3 Antenna

Antenna is very essential for the communication of data between the reader and the tag. Antenna design and placement play a significant factor in coverage zone, range, and accuracy of

communication of a tag, because the antenna both draws the energy from the reader's signal to energize the tag and sends the data that are received from the reader. Antennas in the RFID front end have been designed to match 50Ω load. A RFID tag antenna has to be directly matched to the IC chip, which primarily exhibits complex input impedance. Maximum power must be delivered from the antenna to the IC to maximize the performance of the transponder.

The power arrived at the antenna, P_r, can be calculated using the Friss free-space equation. The Friss free-space equation in dBm is as follows:

$$P_r = P_t + G_t + G_r - 20log_{10}(4\pi d/\lambda) \quad (2.1)$$

where, P_t is the power transmitted by the transmitting antenna, G_t is the gain of the transmitting antenna, G_r is the gain of the receiving antenna, λ is the wavelength of the RF signal, and d is the distance between the receiving and transmitting antenna.

2.3.4 Communication method

2.3.4.1 Near Field coupling

There are two types of near field coupling, capacitive and inductive coupling. Capacitive coupling enables the transfer of energy from one circuit to another by means of the mutual capacitance between the circuits where as in inductive coupling the transfer of energy from one circuit to another is obtained by the mutual inductance between the circuits[15]. Low frequency tags (125 KHz and 13.56 MHz) rely on inductive coupling. The advantage of inductive coupling is that it operates in water, and disadvantage is that it limits the wireless range to 1m.

The basis for near field coupling between the reader and the tag is Faraday's principal of magnetic induction. The reader passes a large alternating current through the reader coil which results an alternating magnetic filed in its locality (Figure 2.4). If a tag incorporates a small coil

is placed in this field an alternating voltage will be generated across the coil. If this voltage is rectified through a power harvesting circuit and coupled to a shunt capacitor, a large amount of charge can be accumulated, and that can be used to power the tag chip. The tag responds to the reader by changing its input load which results in the amplitude and phase variation of the primary coil's voltage. This method is also called load modulation. The range of the magnetic induction approximates to $c/2\pi f$, where c is a constant (speed of light) and f is the frequency. When the frequency of operation increases, the distance over the near field decreases. Another limitation is the energy available for the induction as a function of distance from the reader coil drops off as a factor of $1/r^3$, where r is the separation of the tag and the reader. Therefore near field coupling systems are only useful for low frequency RFID systems.

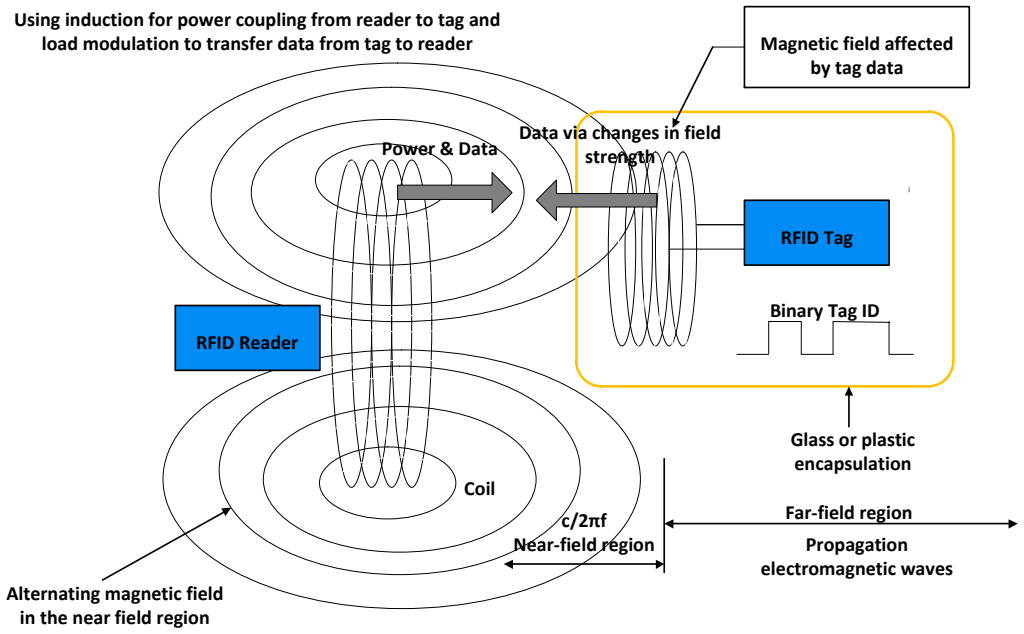


Figure 2.4 Near field power/communication mechanism for RFID tags operating at less than 100MHz

2.3.4.2 Far Field coupling

In the far field RFID system the communication between the tag and the reader is performed through transmission, propagation, and reception of electromagnetic waves. RFID tags based on far-field communication capture electromagnetic waves propagating from an antenna attached to the reader. However unlike inductive designs, the tags are beyond the region of the reader's near field. Therefore the information cannot transmit back to the reader using the load modulation. The method use for far-field RFID communication is backscattering technique (Figure 2.5). If an antenna is designed with precise dimensions, it can be tuned to a particular frequency and most of the energy that reaches in that frequency. However, when an impedance mismatch occurs at that frequency, the antenna will reflect back some of the energy towards a reader. Therefore by changing the antenna's impedance, the tag can reflect back more or less of the incoming signal in a pattern that contains the tag's ID. Tag can be detuned by placing a transistor across the antenna. The far field system range is limited by the amount of energy that reaches the tag from the reader. In far filed coupling the electromagnetic field strength attenuates according to the relationship d^{-1} and corresponds to a power damping factor of *20log(d)*. Far field communication systems are useful for ISM bands at 433 MHz, 900 MHz, 2.45 GHz, 5.8 GHz, and 24.125 GHz considering the power decay relation as a function of distance. These tags have the opposite properties of inductively coupled tags. They work poorly near water and long wireless ranges up to 20 m.

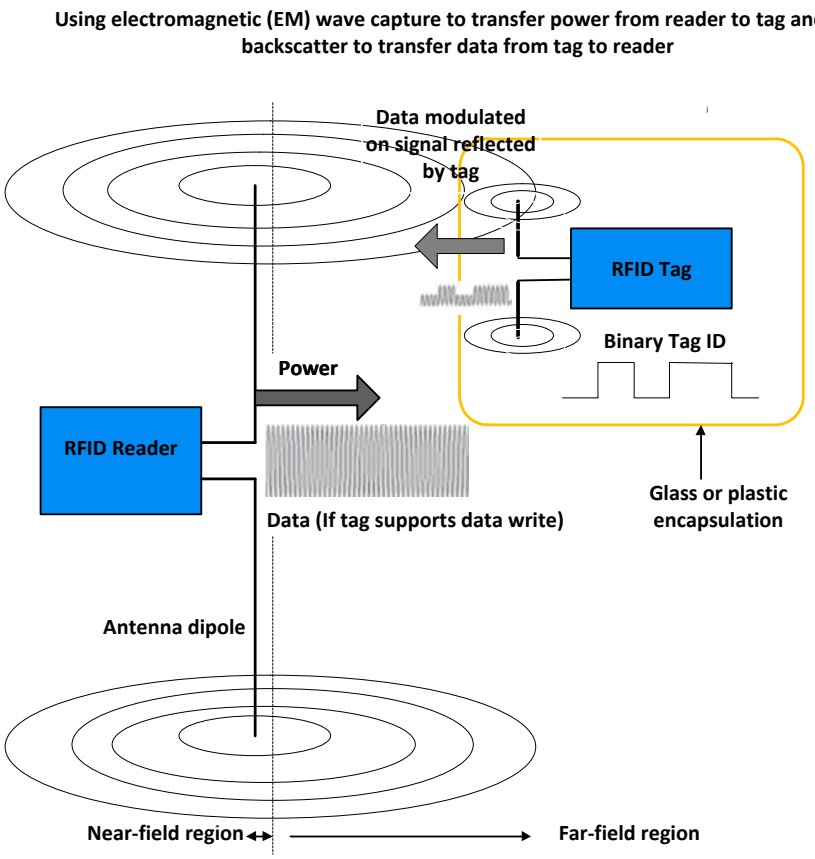


Figure 2.5 Far field power/communication mechanism for RFID tags operating at greater than 100MHz

2.3.4.3 Backscatterring modulation technique

This technique is based on the variation of the reflection coefficient Γ at the input of a transponder. Γ can vary in amplitude or in phase (Figure 2.6). Therefore two modulation types are possible: Amplitide Shift Keying (ASK) and Phase Shift Keying (PSK)

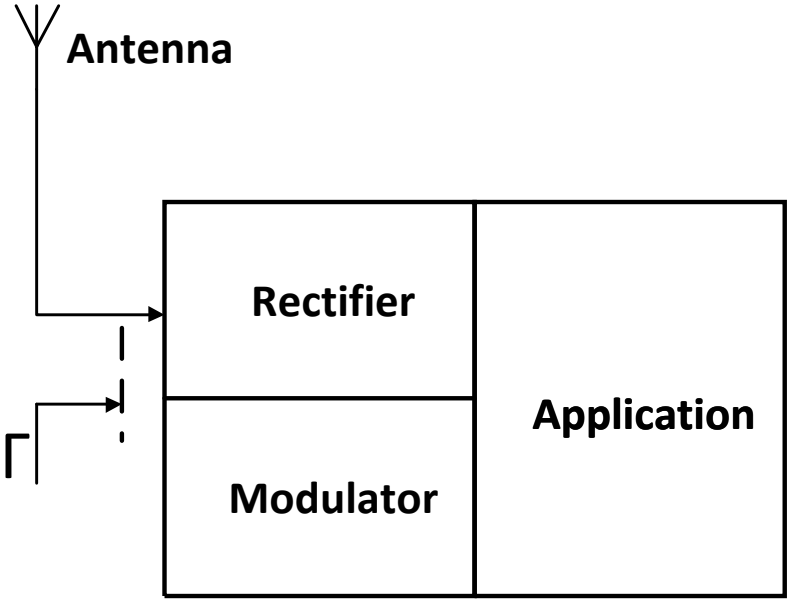


Figure 2.6 Passive Transponder system architecture[15]

In ASK modulation scheme, the reflected power is switched between two or more values at a given rate. In passive tags, Binary Amplitude Shift Keying (BASK) is sufficient, considering the amount of data to be transmitted.

PSK backscattering modulation scheme relies on the relative phase variation between the incoming and the reflected waves at the antenna. The transponder switches its input impedance between two values depending on the modulation angle between the power waves being reflected in Binary Phase Shift Keying (BPSK).

2.3.4.4 Bit-by-bit active transmission

Most RFID systems operate in lower frequencies backscattering modulation[20]. However at mm-wave frequencies limited TX-RX isolation, higher phase noise, and limited dynamic range in the tag reader will limit the use of backscattering[21]. The reader sends

continuous wave (CW) signals to power up the tag and listens to the tag response between bursts (Figure 2.7). The tag harvests sufficient energy from the reader CW bursts and then responds by transmitting back one bit using pulse width modulation when the reader is in the listening mode. The tag then waits in low power, standby mode for the next input CW burst. In this architecture the transmitter never transmits and receives the bits, reduces limited TX-RX isolation. The tag stores the harvested energy on an integrated storage capacitor, reducing the energy per transmitted bit. It also reduces the size of the capacitor and as a result the size of the tag.

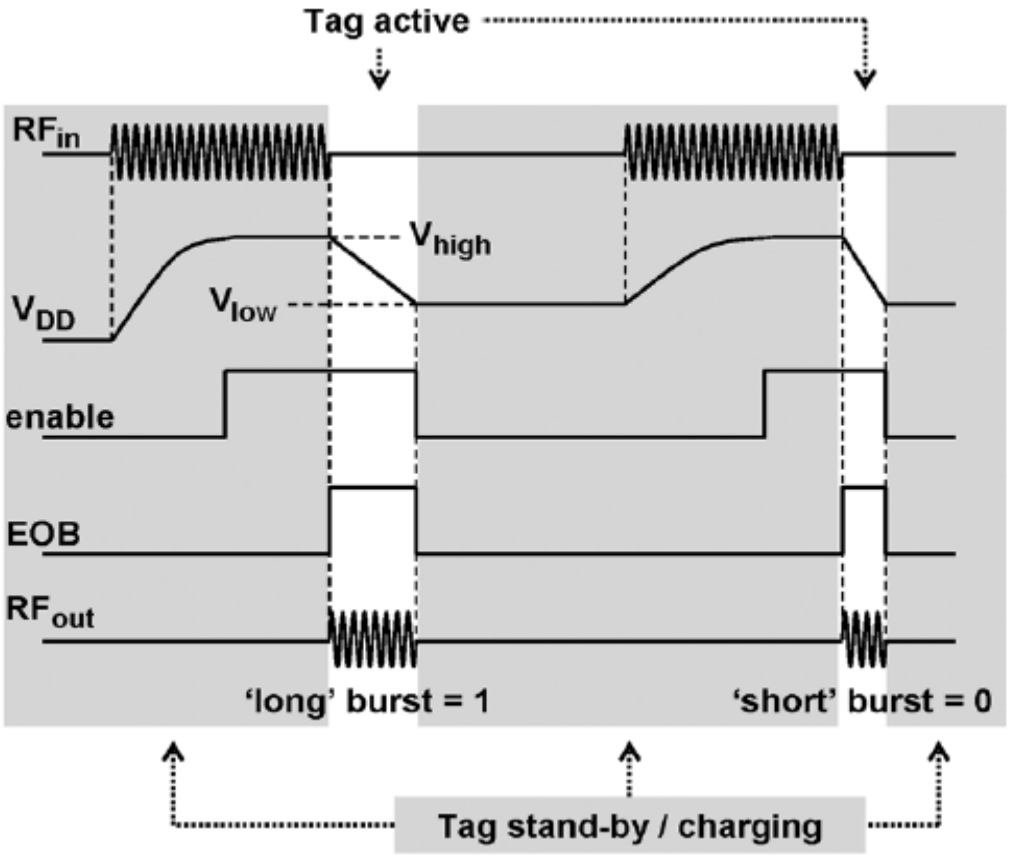


Figure 2.7 Conceptual drawing of some internal signals of mm-wave RFID tag transmision

2.4 RFID Applications

RFID is an emerging technology that has been successfully applied in supply chain management, manufacturing, and logistics, but its range of application extends far beyond these areas. Increasing numbers of companies have already started pilot schemes or successfully used it in real-world environments. Based on the reviewed literature, we classify this category as follows.[11]

i. Insect tracking
ii. Aviation – Airlines and airports provide a unique demand. In this industry there can be significant cost savings, almost unquantifiable improvements in security[3]
iii. Access control – Access control is a commodity market with very competitive pricing, which has a lot of benefits from RFID. Transponders can be provided in a credit card or badge format, readable form a meter distance, even if in a bag, pocket or concealed by clothing[3].
iv. Construction
v. Enterprise feedback control
vi. Fabric and clothing
vii. Food safety
viii. Sensing [9] – RFID sensing in relation to perishable goods such as meat, fruits and dairy products should not exceed a critical temperature during transportation. Otherwise they are not suitable for consumption. RFID temperature sensor could both identify goods and ensure that the goods remain within a safe temperature range.
ix. Asset Protection – Low frequency systems have a good penetration of non metallic materials meaning tags can be embedded into items which need surveillance. A latest

application is tagging of babies in hospital maternity departments allowing urgent alarm and the unique number ensuring the baby is quickly identified[3].

x. Motor car industry – Tags control all the stages of vehicle build, provide location data during distribution to dealers, can provide electronic VIN identity for owner security[3]

xi. Road tolling – Many approaches have been adopted for automatic charging of toll road use. They are short range communication (5-30 meters), wide area systems, and video based systems. RFID technology is used for short range systems. In short range based system the communication dialog is established between a road-side communication station and a tag mounted in a vehicle[22]. Short range communication system has sensor equipment, vehicle mounted system, roadside interrogator systems, roadside linking interrogators, and photographic or video registration system. Short range system has three modes, namely simplex mode, half-duplex mode, and full-duplex mode.

Another distinguished feature of modern RFID is that it contains more information than a simple ID. It can incorporate additional read only or read-write memory to interact with the reader. Read only memory can contain additional product information that don't need to be read every time, a tag is interrogated, but are available when required. For example, a tag memory might contain a batch code, if some products are found to be damaged; the batch code can help identify the other items with the same defects.

Tag memory can also be used to enable tags to store self-describing information. Whether the tag's unique ID can be used to recover it's records from a database, communication with the database might not always be possible. For example if a package is misdirected during transportation, the receiving organization might not be able to determine its correct destination.

Additional destination address stored in the tag would eliminate the requirement of a fully networked very expensive tracking system.

2.5 RFID Frequencies

A very important aspect of an RFID system is the operating frequency of the reader and the tag. In general, operating frequency defines the data rate between the tag and the reader. Lower operating frequency usually means slower data rate. In addition to the data rate, operating frequency also determines the tag size. For example high operating frequency means smaller antenna and tag size. RFID operating frequencies mainly fall into three categories namely, low frequency (LF – 125KHz), high frequency (HF – 13.56MHz), and ultra-high frequency (UHF – 900MHz) [23]. UHF-900 MHz RFID systems are a better solution for next generation auto-ID applications because they have fast transmission throughput and long distance communication. All of these systems work using electromagnetic far-field radiation of waves in the UHF range. Most of these systems are widely known as backscatter systems. Table 2.2 shows LF-HF and UHF-900 MHz RFID reader and tag. Table 2.2 summarizes the most popular frequency bands and their applications.

Table 2.2 *Different frequency ranges and their applications*

Frequency range	**Key Characteristics**	**Description**	**Application**
Low Frequency (LF) Less than 135KHz	• In use since 1980s and widely deployed • Lowest data rate • Read range measured in inches	LF, inductive coupling	• Animal identification • Industrial automation • Access control

High Frequency (HF) 13.56 MHz	• In use since mid 1990s and widely deployed • Common worldwide standards • Lower tag costs than LF tags • Poor performance around metal	HF, inductive coupling	• Anti-counterfeiting • Various item level tracking applications such as for books, luggage, and garments • People identification and monitoring
Ultra High Frequency 868 MHz – 870 MHz 902 MHz – 928 MHz	• In use late 1990s • Longer read range (10 + feet) • Potential to offer lowest cost tags	UHF, backscatter coupling	Supply chain tracking such as inventory control, warehouse management, and asset tracking
Microwave 2.45GHz – 5.8 GHz	• In use for several decades • Fast data transfer rate • Common in active and semi-active modes • Poor performance around liquid and metal	Super high frequency (SHF), backscatter	• Highway toll collection • Industrial automation • Access control

2.6 RFID Standards

As in many technological sectors, many standards exist in RFID. Transponder format, communication protocols, frequency of operation, the code or ID can be part of the standard. The available standards are Electronic Product Code (EPC) Global initiative, and the ISO 18000 standard. ISO only deals with the air interface, whereas EPC also includes the data structure of the ID.

2.6.1 The EPC standard

The auto-ID center has proposed a new EPC to identify products just like the bar code does.

Table 2.3 EPC Transponder classes

EPC Class	**Feature**	**Transponder Type**
Class 0	Read only	Passive (64 bits only)
Class 1	Write once, Read many (WORM)	Passive (96 bits minimum)
Class 2	Read/Write	Passive (96 bits minimum)
Class 3	Read/Write with embedded energy to enhance the operating range	Passive (96 bits minimum)
Class 4	Read/Write active transmitter	Passive (96 bits minimum)

2.6.2 The ISO standard

The ISO standard is active in the developments of RFID standards for supply chain management. The ISO 14443 is used for proximity cards and ISO 15693 is used for vicinity cards. In UHF and higher frequencies ISO18000 part 4 to part 7 are a set of RFID specifications for item management. They define the operating frequency, operating channel accuracy, occupied channel bandwidth, maximum EIRP, modulation type, bit rate, bit rate accuracy, bit transmission order, and chip rate.

2.7 RFID Generations

There are three generations of RFID tags.

Generation 1: Only capable of communicating with a unique identifier

Generation 2: Capable of programmed and reprogrammed communicating as needed.

Generation 3: Not only programmed and reprogrammed but also communicating with RFID readers and other RFID Tags.

CHAPTER 3

X-band RFID Tag Architecture

In this chapter a general overview of the proposed system is presented. A block diagram of the proposed passive RFID tag operating in the 5.8 GHz ISM band is given in Figure 3.1

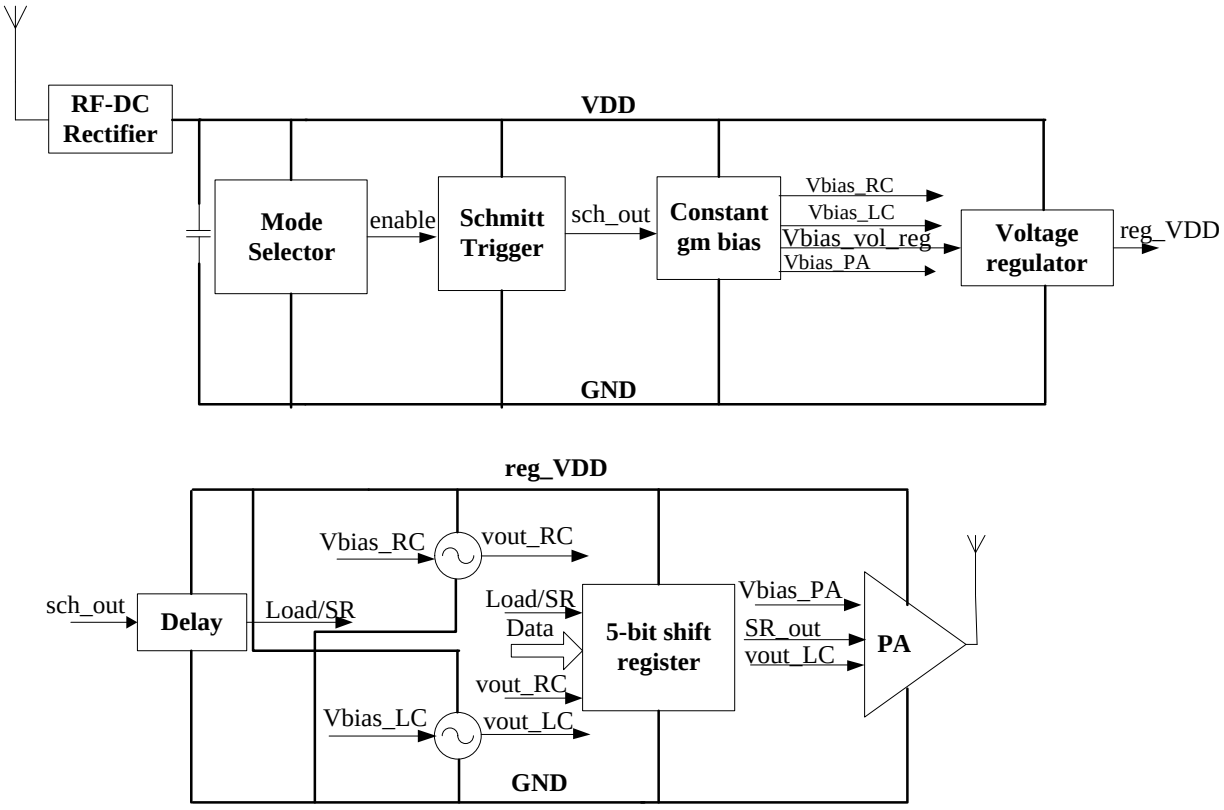


Figure 3.1 Block diagram of the RFID tag

The RF-DC rectifier which generates useful DC voltage values with electromagnetic waves (EM) coming from the receiving antenna. The mode selector is used to put the system into stand by mode, while the system is collecting enough energy to operate itself. Once enough energy is collected, the system is enabled from the mode selector block. The system is transmitting data until it is put back into stand by mode. This dual mode operation allows the

useful energy to be scavenged from an incident RF signal. The voltage regulator is used to provide stable power supply for the rest of the circuits in the RFID tag. The CMOS switch in the power amplifier is used to provide ASK modulation for the bits of the RFID tag. Storage capacitor is used to store the energy from RF to DC rectifier. The stored energy of the storage capacitor is used to transmit the bits of the RFID tag. The power stored in storage capacitor must use effectively because the discharging time of the storage capacitor is low. Therefore all circuit blocks are designed to work with low supply voltages with low power dissipation.

RF-DC Rectifier : Collect EM energy and convert it to DC This generates a DC output ($\mathbf{V_{DD}}$) for the other blocks from a 5.8GHz incident RF signal.

Mode selector : Monitors the supply voltage V_{DD} and compares it with V_{high} and V_{low} to determine whether the tag is ready to transmit or not. This will generate the enable signal for the circuit. Enable signal is obtained by the comparator circuit (by comparing V_{high} and V_{low}).

Schmitt trigger : Is used to convert the sloppy enable signal generated from the voltage sensor circuit to a digital signal.

Voltage regulator : Is used to provide contant V_{dd} from the unregulated V_{dd} for the rest of the circuits.

Bias Generator : Provides stable bias voltages for the Injection locked LC oscillator, RC oscillator, Voltage regulator, and Power amplifier circuits. This circuit is active only if the enable signal is high.

Delay circuit : Is used to generate the Load or Shift signal for the 5-bit shift register.

Injection locked LC oscillator : LC oscillator is injection locked to superharmonic of the incident RF signal. This generates a 11.6 GHz sine wave from a 5.8 GHz incident RF signal

RC oscillator : Generates the 500 MHz clock signal for the digital circuit.

Five bit Parallel in/Serial out shift register : The five bit data is read from the ROM. Parallel bits are converted to serial bits.

Power amplifier : Drives the antenna to transmit the RF signal.

CHAPTER 4

Design of the Proposed X-band RFID Tag

4.1 RF-DC Rectifier

4.1.1 10 GHz RF-DC rectifier design

A multi-stage rectifier circuit was used to convert input RF power to DC power (Figure 4.1). Each unit cell consisted of two diode-connected NMOS transistors in series to transfer charges from the capacitor of the previous cell except for the first cell. Both coupling and storage capacitors along with parasitics play critical roles in the rectifier X-band performance. The ZVT (zero-threshold) NMOS transistors are used to maximize rectifier performance [2].

The capacitance C_0 has negligible impedance at the frequency of the RF input and is open for DC. Thefore node A follows the "RF in" input. The capacitor C_0 and diode connected transistor form the forms a half wave rectifier and generates a DC output at node B with the value of the incident RF signal amplitide. The node voltage at C is the sum of the DC value and the AC value of that node, which can be written as

$$V_c = V_p + V_p Sin(wt) \quad (4.1)$$

Then C_0 and diode connceted transistor M_4 create second half wave rectifier. Thefore the value genereated at node D is equal to $2Vp$. Therefore the DCoutput voltage generated by the RF-DC rectifier is

$$V_{out} = N(V_{rf} - V_{th}) \quad (4.2)$$

Where N is the number of cells in RF rectifier, V_{rf} is the input RF amplitude at the coupling capacitor terminal, V_{th} is the threshold voltage of ZVT (actually ~22mV). The voltage multiplication efficiency is defined as

$$\eta = \frac{N(V_{rf})}{V_{out}} X\ 100 \quad (4.3)$$

Using the charge conservation principle, we derived the final DC output voltage as,

$$V_{out} = 2N\left(V_{rf} - V_{th}\right) - \frac{I_{out}}{f}\left(\sum_{k=1}^{N}\frac{1}{Co_k} + \sum_{k=1}^{N}\frac{1}{CL_k}\right) \quad (4.4)$$

where V_{out} is the DC output voltage and I_{out} is the DC output current, N is the number of cells in RF rectifier, V_{rf} is the input RF amplitude at the coupling capacitor terminal, V_{th} is the threshold voltage of ZVT (actually ~22mV).

We then define C_{eff} as,

$$\frac{1}{C_{eff}} = \sum_{k=1}^{N}\frac{1}{CO_k} + \sum_{k=1}^{N}\frac{1}{CL_k} \quad (4.5)$$

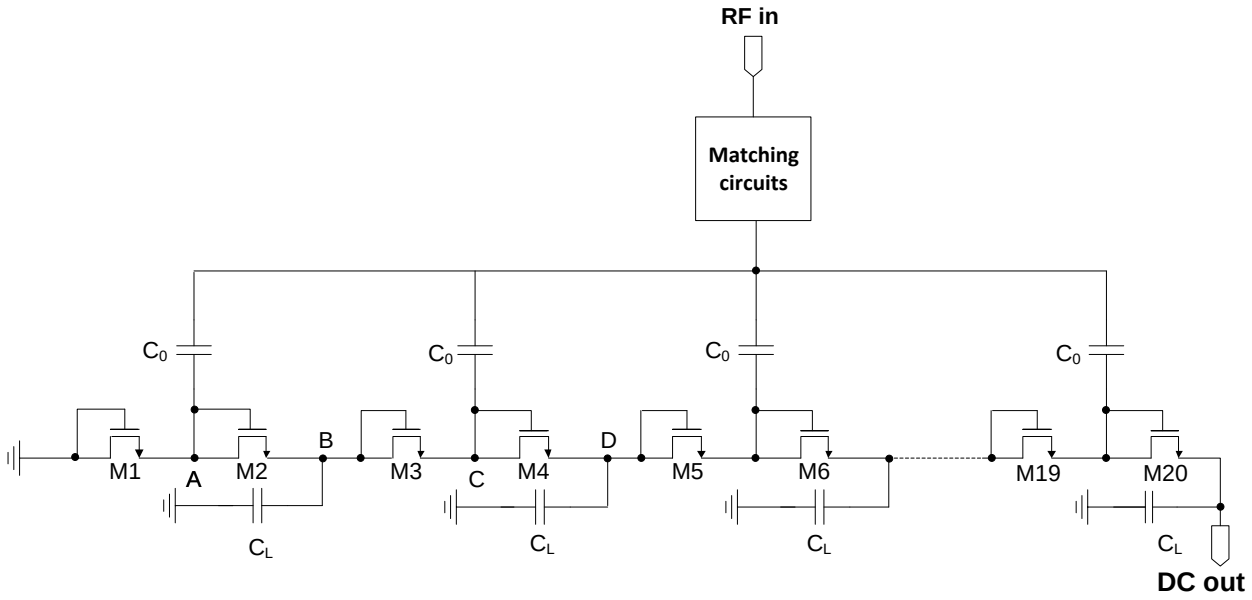


Figure 4.1 Schematic of the energy harvester for passive RFID transponder

V_{out} is expressed as,

$$V_{out} = 2N\left(V_{rf} - V_{th}\right) - \frac{I_{out}}{f.C_{eff}} = V_{oc} - I_{out}R_{out} \quad (4.6)$$

where

$$V_{oc} = 2N(V_{rf} - V_{th}), R_{out} = \frac{1}{f.C_{eff}} \quad (4.7)$$

V_{oc} is the open-circuit voltage and R_{out} is the internal resistance of the rectifier.

Essentially, C_{eff} is equivalent to the series connection of all load capacitors and coupling capacitors in the rectifier units. The parasitic capacitances of transistors were omitted in this analysis. In practice, they can be considered to be absorbed into coupling and storage capacitors. Contrary to the conventional design rule of thumb where C_o needs to be much larger than C_L, the above analysis shows that C_o and C_L contribute equally to C_{eff}. They also contribute equally to the input impedance of the rectifier block. As we can see, when I_{out} is zero, (4.4) becomes the same as the first order estimation. The output resistance of the DC source is given by $1/(f\ C_{eff})$. This provides guidance in choosing coupling and load capacitances.

The size of all the diode-connected transistors is also constrained by their parasitic capacitances, i.e. wide transistors provide large charging current for capacitors but require more charges to turn them on or off. Transistor sizes also contribute to the overall admittance and directly impact the matching network design.

4.1.2 Matching network

Due to the nonlinear nature of the rectifier, the matching network design differs from the one for a linear RF system. Voltage boosting was emphasized because the Zero-VT transistors require a non-zero voltage (~22 mV) to turn on.

Many different matching networks were considered and simulated. The cases shown in Figures 4.2(a) and 4.2(b) are among the most promising solutions, while that in Figure 4.2(c) is no-matching case (direct feed into the rectifier). All three cases were extensively optimized and implemented in the final layout.

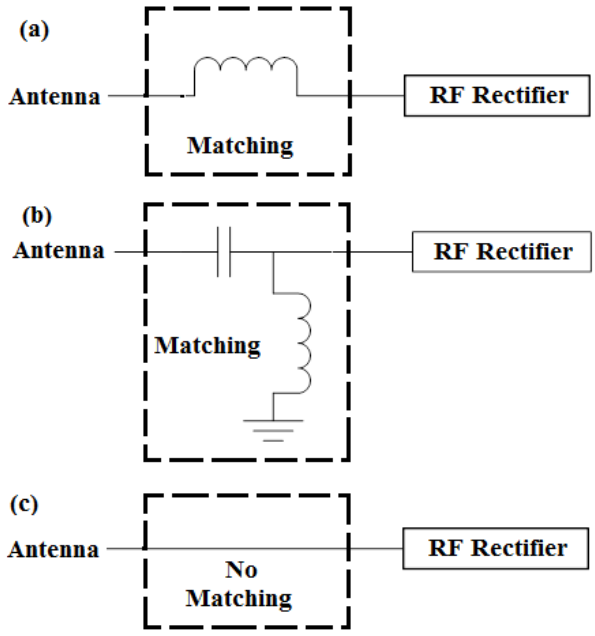


Figure 4.2 Matching network for multistage rectifier, (a) series inductor matching; (b) series capacitor-shunt inductor matching; (c) direct feed through without matching

4.1.3 Rectifier efficiency

The conversion efficiency η_c is defined as

$$\eta_c = \frac{DC\ Ouput\ power}{Incident\ RF\ Power - Reflected\ RF\ power} \tag{4.5}$$

Whereas the overall efficiency η_c is equal to

$$\eta_o = \frac{DC\ Ouput\ power}{Incident\ RF\ Power} \tag{4.6}$$

Table 4.1 and Table 4.2 present the values of the circuit components, transistor sizes, and simulated rectifier performance of the X-Band CMOS rectifier with series inductor matching and parallel inductor/series capacitor matching.

Table 4.1 Design Values

Technology	IBM 0.18µm RF CMOS
Number of Rectifier stages number	6
Coupling capacitors	MIM Cap, C_{eff} =150fF
Load capacitors	MIM Cap, C_{eff} =150fF
Transistors	ZVT W/L=3µm/0.7µm
Operating Frequency	~10GHz
RF amplitude	300mV

Table 4.2 Simulated performance of two cases

	Series Inductor	**Parallel Inductor**
Layout area	200µm x 150µm	100µm x 150µm
Matching	L_S=2.76nH	L_P=1.37nH C_S=128.17fF
Vout @250KΩ	1.76V@ -8.1dBm	1.32V@ -8.1dBm
Conv. Eff.	8% @ -8.1dBm	3.09%@ -8.1dBm
Equiv. Rs	~100KΩ	~100KΩ

The rectifier circuit was simulated by both AC and transient analysis. Transistors were ZVT NMOS with gate length of 700 nm. We compared rectifiers with 3 to 10 stages. With the increased number of stages, matching became more difficult. Our analysis revealed that about 6 stages provide the best performance. When the rectifier has more than 6 stages, increased transistor parasitic losses reduced the total rectified voltage.

4.2 5.8 GHz RF-DC Rectifier Design

10 stage rectifier transient simulations with series and parallel matching are shown in Figure 4.3. and Figure 4.4. Rectifier stage optimization (Table 4.3) was carried out through cadence parametric sweep.

Table 4.3 RF-DC rectifier stage number optimization

Stage no	Width (μm)	Couple cap	Load cap	Amplitude (mV)	Vout (V)	Load resistance (KΩ)	dc_current (μA)
16	6	900 fF	900 fF	300	1.10	250	4.11
		1.05 pF	1.05 pF	300	1.06	250	4.11
		1.2 pF	1.2 pF	300	1.03	250	4.11
		1.35 pF	1.35 pF	300	1.00	250	4.11
		1.5 pF	1.5 pF	300	0.98	250	4.11
10	3	900 fF	900 fF	300	1.24	250	4.95
	6	900 fF	900 fF	300	1.238	250	4.95
	7.5	900 fF	900 fF	300	1.02	250	4.95
	9	900 fF	900 fF	300	0.823	250	4.95
	10.5	900 fF	900 fF	300	0.647	250	4.95
	12	900 fF	900 fF	300	0.519	250	4.95
8	3	900 fF	900 fF	300	1.16	250	4.56
	6	900 fF	900 fF	300	1.14	250	4.56
	7.5	900 fF	900 fF	300	0.986	250	4.56
	9	900 fF	900 fF	300	0.828	250	4.56

	10.5	900 fF	900 fF	300	0.678	250	4.56
	12	900 fF	900 fF	300	0.555	250	4.56

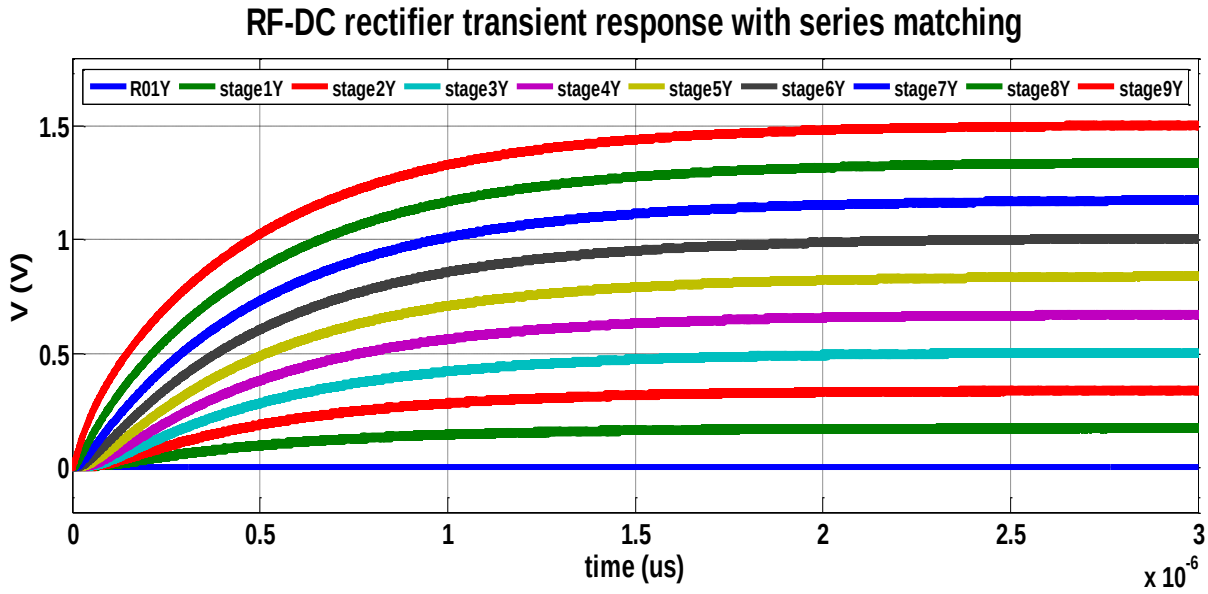


Figure 4.3 10 stage RF-DC rectifier transient response with series matching

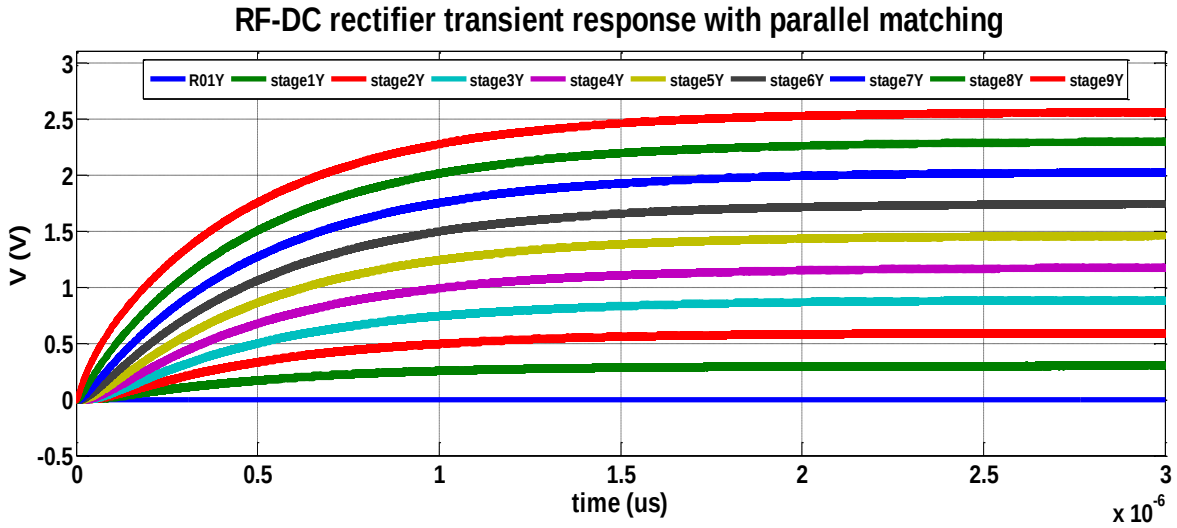


Figure 4.4 10 stage RF-DC rectifier transient response with parallel matchi*ng*

4.3 Mode Selector

The rectifier rectified and multiplied the incident RF signal, and stored the energy on a large storage capacitor. During this time, it is crucial that the current dissipation in the whole system be kept to a minimum. In the standby mode (always on), the system waits to capacitor to charge and consume very little current.

The system was enabled by the mode selector circuit when the voltage stored on the storage capacitor exceeds a upper threshold value. Figure 4.5. shows the schematic of the voltage sensor circuit. Voltage comparator transistor sizes are given in Table 4.4. The Mode selector (voltage sensor) monitors the supply voltage V_{DD} and compares it against with V_{high} and V_{low} to determine whether the tag is ready to transmit or not. Hysteresis in the comparator generates the enable signal was obtained by adjusting the comparison reference voltages according to the current state of the enable signal. V_{high} and V_{low} are the two reference voltages of the comparator (Figure 4.6).

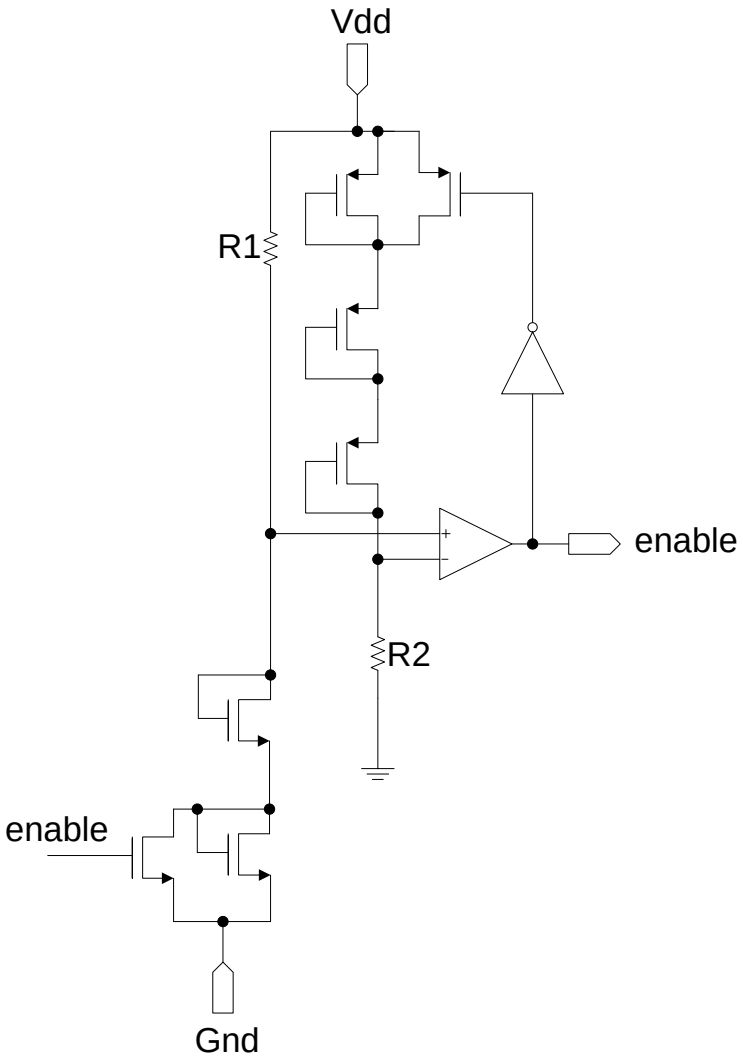


Figure 4.5 Voltage sensor schematic

When the switch is open

$$V_{DD} - 3V_{TH} > 3V_{TH} \quad (4.5)$$

$$V_{DD} > 6V_{TH} \quad (4.6)$$

When the switch is closed

$$V_{DD} - 2V_{TH} > 2V_{TH} \quad (4.7)$$

$V_{DD} > 4V_{TH}$ (4.8)

Therefore V_{DD} $(V_{\text{high}}) \approx 4V_{\text{TH}}$

When the switch is open

$V_{low} > 3V_{TH}$ (4.9)

When the switch is closed

$V_{low} > 2V_{TH}$ (4.10)

Therefore V_{DD} $(V_{\text{low}}) \approx 2V_{\text{TH}}$

where V_{TH} is the device threshold.

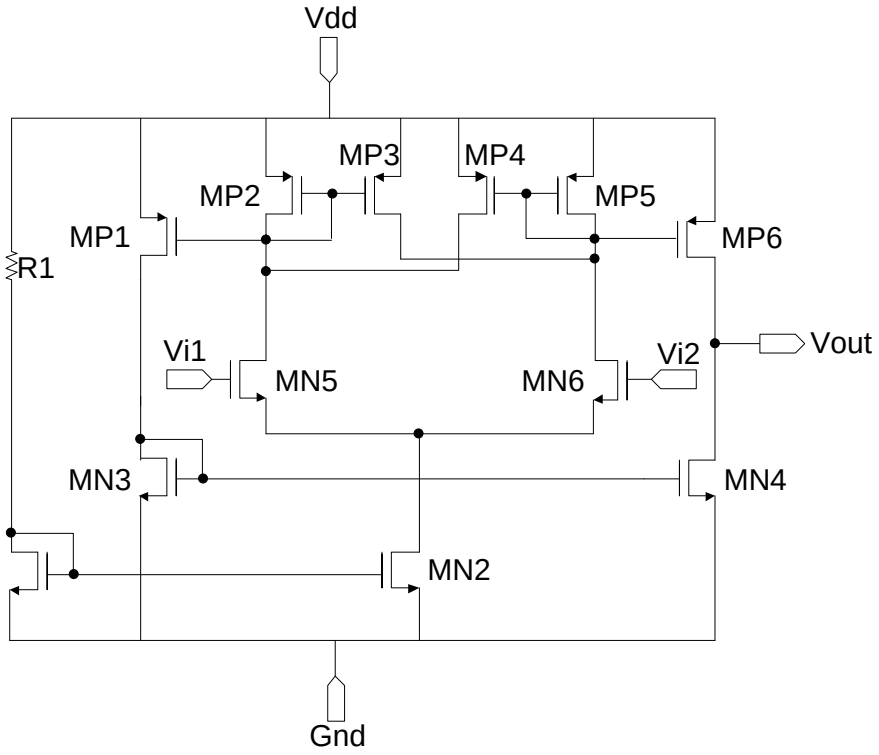


Figure 4.6 Voltage comparator circuit

Table 4.4 Voltage compartor transistor sizes

Component name	Size
MN1	W = 0.75 µm L = 4 µm
MN2	W = 3 µm L = 4 µm
MN3	W = 4 µm L = 2 µm
MN4	W = 4 µm L = 2 µm
MN5	W = 100 µm L = 0.18 µm
MN6	W = 100 µm L = 0.18 µm
MP1	W = 5 µm L = 1 µm
MP2	W = 2 µm L = 1 µm
MP3	W = 20 µm L = 2 µm
MP4	W = 20 µm L = 2 µm
MP5	W = 2 µm L = 1 µm
MP6	W = 5 µm L = 1 µm
R1	13.195MΩ

Since the voltage sensor is a always on circuit, the voltage sensor must be designed to consume very low current. The voltage sensor circuit was designed to consume less than 0.5 µA current. Therefore the comparator, negative and positive branches of the voltage sensor should consume less than 0.5 µA.

In order to reduce the current though the comparator, resistance (R_1) was increased, the size of MN1 was decreased, and to maintain the same current flows through MN2, the sizes of MN5 and MN6 were increased, and the sizes of MP3 and MP4 were increased. (Table 4.5)

Table 4.5 Voltage comparator transistor sizes for total current consumption less than 0.6μA

Resistor (Ω)	**Current (μA)**	**MP4 Current (μA)**	**W/L**	**MP3 rrent (μA)**	**W/L**	**MN1 Current (μA)**	**W/L**	**MN2 Current (μA)**	**W/L**	**Com. Current (μA)**	**Left branch (MΩ)**	**Right branch (MΩ)**	**Total current (μA)**
9.22	0.238	0.156	4/2	0.135	4/2	0.101	1.5/4	0.275	3/4	0.604	0.321	0.248	1.173
11.53	0.121	0.95	8/2	1.15	8/2	0.107	0.75/4	0.351	3/4	0.525	0.131	0.109	0.765
13.19	0.101	0.101	20/2	0.017	20/2	0.101	0.75/4	0.342	3/4	0.387	0.158	0.114	0.659
13.19	0.101		100/2		100/2					0.142	0.107	0.591 Not working	

When enabled, the system draws current from the capacitor, discharging it. Then system put back to standby mode, when the voltage on a storage capacitor drops below a threshold value (V_{low}). Mode selector circuit works both in stand by and active modes. Therefore it should consume less current. Therefore the mode selector circuit was designed to consume a current less than 1µA. Mode selector circuit transient response is shown in Figure 4.7.

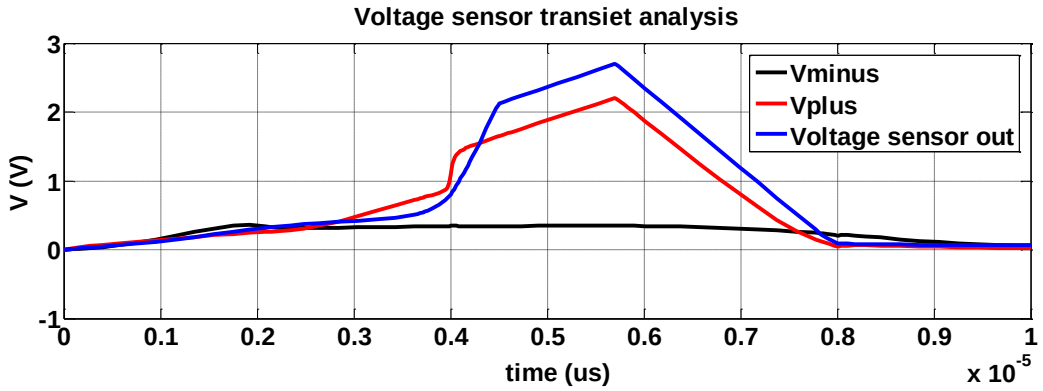


Figure 4.7 Voltage sensor transient analysis

The DC sweep simulation of the voltage of the output node of the mode selector (voltage sensor) circuit is given below (Figure 4.8). It should be noted, when VDD voltage changing during active operation (i.e. the storage capacitor is discharging), the value of the output voltage varies as it tracks the supply voltage.

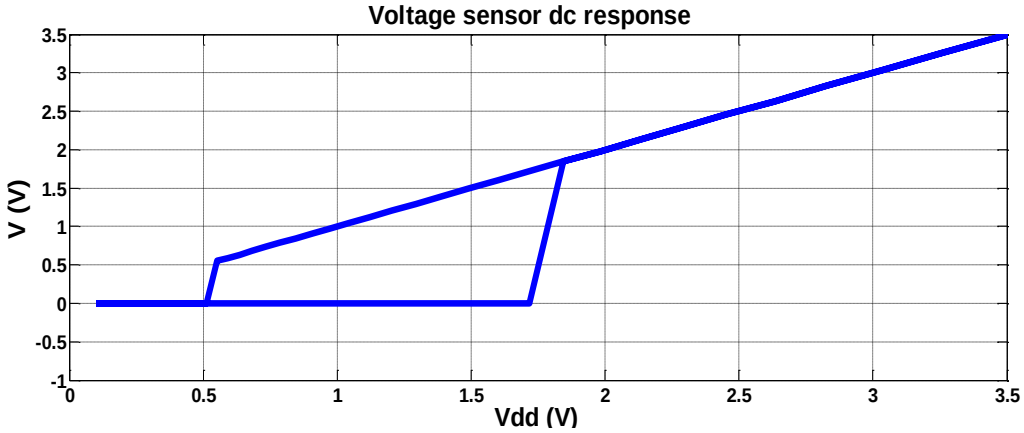


Figure 4.8 DC sweep simulation of the enable output of the voltage sensor

4.4 Schmitt Trigger

Schmitt trigger is a device that responds to a slowly changing input waveform with a fast transition time at the output. One of the main uses of Schmitt trigger is to turn a noisy or slowly varying input signal into a clean digital output signal. Schmitt trigger circuit uses the concept of positive feedback.

The schematic of the schmitt-trigger circuit is given below (Figure 4.9).

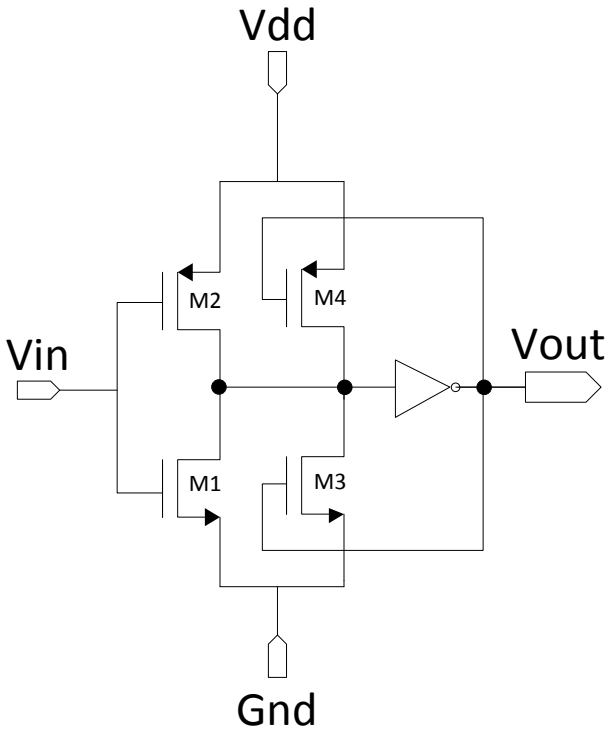


Figure 4.9 Schmitt trigger circuit

Suppose that V_{in} is initially equal to 0, so that $V_{out} = 0$ as well. The feedback loop biases the pmos transistor M_4 in the conductive mode while M_3 is off. The input signal effectively connects to an inverter consisting of two pmos transistors in parallel (M_2 and M_4) as a pull-up network, and a single NMOS transistor (M_1) in the pull down chain. This modifies the effective transistor ratio to $k_{M1}/(k_{M2} + k_{M4})$, which moves the switching threshold upwards.

When the inverter switches, the feedback loop turns off M_4, and the nmos device M_3 is activated. This extra pull down device speeds up the transition and produces a clean ouput signal with steep slopes.

A similar behavior can be observed for the high-to-low transition. In this case, the pull-down network originally consists of M_1 and M_3 in parallel, while the pull-up network is formed by M_2. This reduces the value of the switching threshold to V_{M-}

In passive RFID tag design schmitt trigger circuit is used to convert the sloppy enable signal generated from the voltage sensor circuit to a digital signal. The input pin v_{in} is connected to the output of the voltage sensor circuit. The output $v_{out}$of this circuit is connected to the constant g_m bias circuit. Schmitt trigger circuit works both in stand by and active modes. Therefore it was designed to consume less current. Schmitt trigger transistor sizes are given in Table 4.6.

Table 4.6 Schmitt Trigger circuit transistor sizes

Component name	**Size**
M1	W = 0.7 μm L = 0.25 μm
M2	W = 3 μm L = 0.25 μm
M3	W = 0.5 μm L = 0.25 μm
M4	W = 1.5 μm L = 0.25 μm
M5	W = 4 μm L = 0.18 μm
M6	W = 2 μm L = 0.18 μm

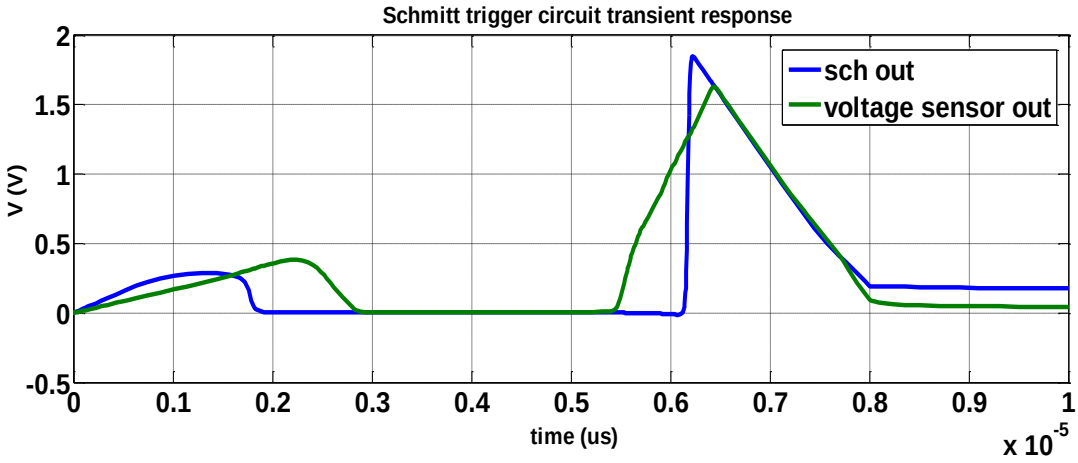


Figure 4.10 Schmitt trigger circuit transient response

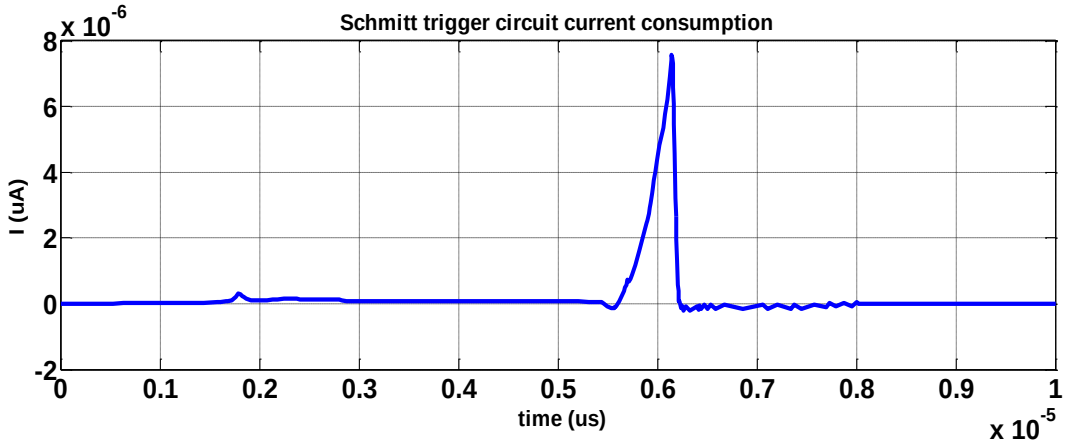


Figure 4.11 Schmitt trigger circuit current consumption

Schmitt trigger circuit transient response is shown in Figure 4.10. Schmitt trigger circuit consumes 7.409µA current in the active mode according to Figure 4.11. It also turns the slowly varying voltage sensor input signal into a clean digital output signal.

4.5 Voltage Regulator

Voltage regulator (Figure 4.12) was designed to maintain constant DC voltage for RC oscillator, LC oscillator and power amplifier circuits in the passive RFID tag design.

The differentiator of the voltage regulator was designed to yield desired transient response, while stabilizing the overall system transfer function. The input and output nodes of M_{19}, forming the first stage amplifier in the inverting differentiator, are the most critical nodes. The inverting differentiator sums into the error amplifier output through transistors M_{16} and M_{15}. The resistor R_3 performs two main tasks. It transforms the current supplied by the capacitor C_2 into a voltage, and provides dc bias voltages for both M_{16} and M_{19} transistors.

The three current mirror operational transconductance amplifier, $M_1 – M_3$, M_5, $M_{6,}$ $M_{8,}$ M_9, M_{11} - M_{13} forms the error amplifier. M_2, M_{12}, M_{15}, M_{18} are added to reduce the offsets due to drain to source voltage on M_6, M_9, $M_{13,}$ $M_{16,}$ and M_{19} and increase the current mirror accuracy when the V_{dd} is increased. The compensation capacitor C_1 is used to improve the AC stability of the voltage regulator. It uses the Miller effect to push the lowest frequency pole to higher frequencies, and placed in positive feedback.

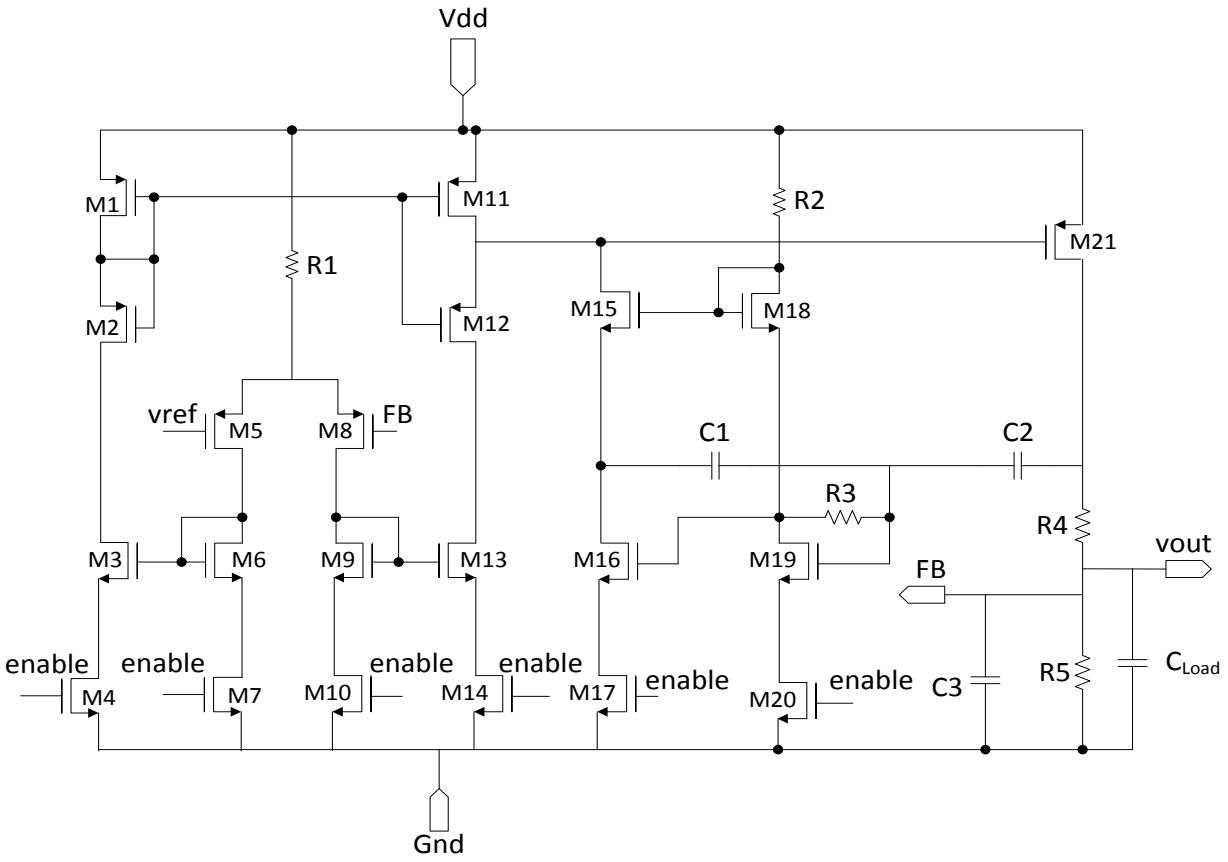


Figure 4.12 Voltage regulator

4.6 Constant G_m Bias Circuit

The constant g_m bias circuit is shown in Figure.4.13.

If $M_4 = M_8$ then, the current through $M_4 \approx$ The current through M_8.

However from the M_6-R_3 loop gives $V_{GS6} = V_{T6} + \sqrt{\frac{2I_6}{K_N'(W_6/L_6)}}$ (4.11)

Solving these two equations gives $I_8 = \frac{V_{T_6}}{R_3} + \left(\frac{1}{R_3}\right)\sqrt{\frac{2I_6}{K_N'(W_6/L_6)}}$ (4.12)

Therefore the output current $I_{out} \approx I_4 \approx I_8$ can be solved as

$$I_{out} = \frac{V_{T_6}}{R_3} + \frac{1}{\beta_6 {R_3}^2} + \frac{1}{R_3}\sqrt{\frac{2V_{T6}}{\beta_6 R_3}} + \frac{1}{(\beta_6 R_3)^2} \quad (4.13)$$

If the reference voltages and currents are process, voltage and temperature (PVT) independent then those voltages can be used as a master bias voltages on a large analog chip. Constant g_m bias circuit transistor sizes are given in Table 4.7.

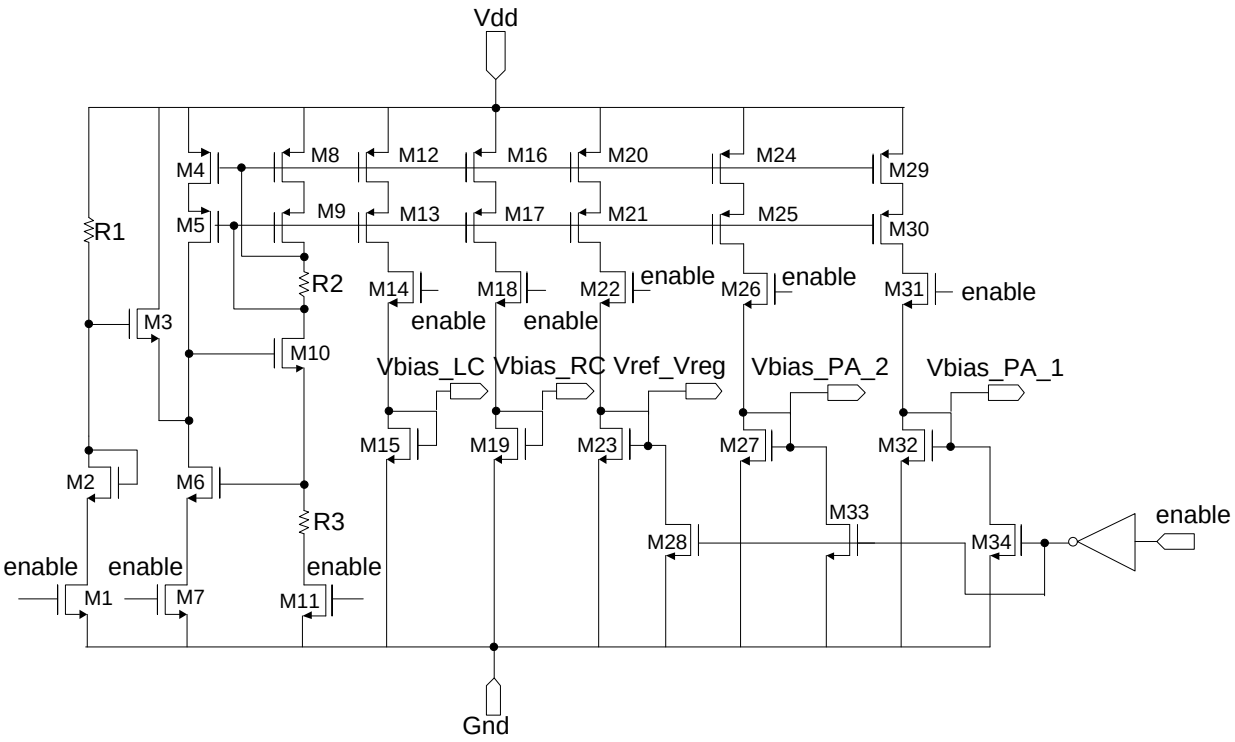


Figure 4.13 Constant g_m bias circuit

Therefore in the RFID tag design, the constant g_m bias circuit was used to provide the stable bias voltages for the RC oscillator, injection lock LC oscillator, Power amplifier and the voltage regulator circuits. The circuit provides stable bias for supply voltages between 1V and 3V.

Table 4.7 Constant g_m bias circuit transistor sizes

Component name	**Size**
M1	20 µm / 0.18 µm
M2	2 µm / 20 µm
M3	8 µm / 1 µm
M4 = M8 = M12 = M16 = M20 = M24 = M29	30 µm / 1 µm
M5 = M9 = M13 = M17 = M21 = M25 = M30	20 µm / 1 µm
M6	40 µm / 1 µm
M7	20 µm / 0.18 µm
M10	30 µm / 1 µm
M11	40 µum / 0.18 µm
M10	30 µm / 1 µm
M14	40 µm / 0.18 µm
M15	1 µm / 4 µm
M18	40 µm / 0.18 µm
M19	1 µm / 4 µm
M22	40 µm / 0.18 µm
M23	1.8 µm / 6 µm
M26	40 µm / 0.18 µm
M27	2.2 µm / 12 µm
M28	40 µm / 0.18 µm
M31	40 µm / 0.18 µm
M32	2.2 µm / 8 µm

M33	40 µm / 0.18 µm
M34	40 µm / 0.18 µm

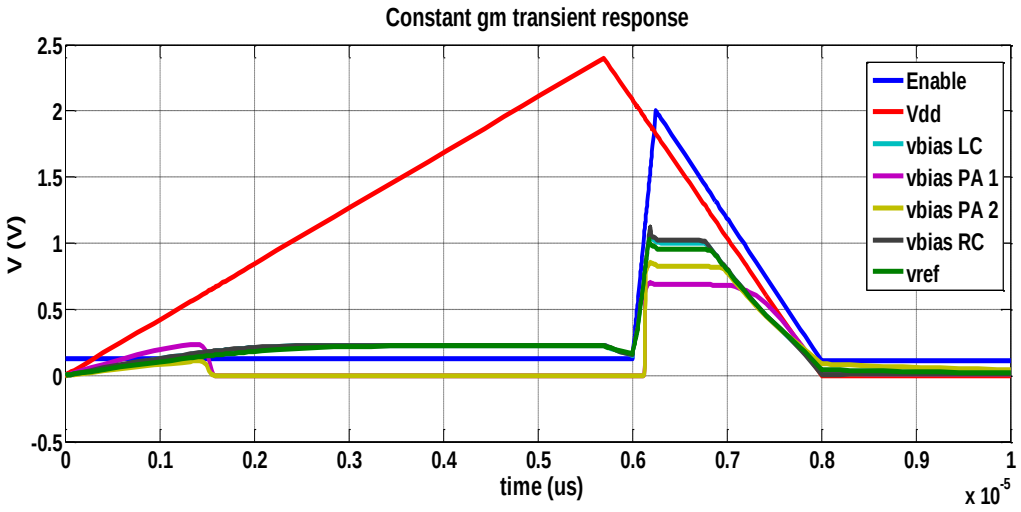


Figure 4.14 Constant g_m circuit transient response

Table 4.8 Constant g_m bias voltages

Variable name	**Voltage (V)**
vbias_LC	1.001
vbias_RC	1.022
vbias_PA_1	0.687
vbias_PA_2	0.826
Vref	0.956

Constant g_m current consumption = $(142.07nA + 100.678\mu A)/2 = 50.41\mu A$

4.7 RC Oscillator

In RF communication systems, in GHz frequency range, preferred type of oscillator is either LC oscillator or ring oscillator. LC oscillator is preferable because of its better phase noise performance compared to the ring oscillator[24]. However in CMOS process, an inductor is expensive because it is not a standard device and it takes a considerable chip area[25]. In many modern CMOS processes a thick copper metal is used for an inductor instead of aluminum to improve the quality factor (Q), which also increases the fabrication cost. The accuracy and the flexibility of a model can be problematic for the designer because design parameters are limited to ensure better model accuracy. Because the oscillation frequency is determined by a Band Pass Filter (BPF) made of passive resistors and capacitors the frequency is less susceptible to power supply noise[26].

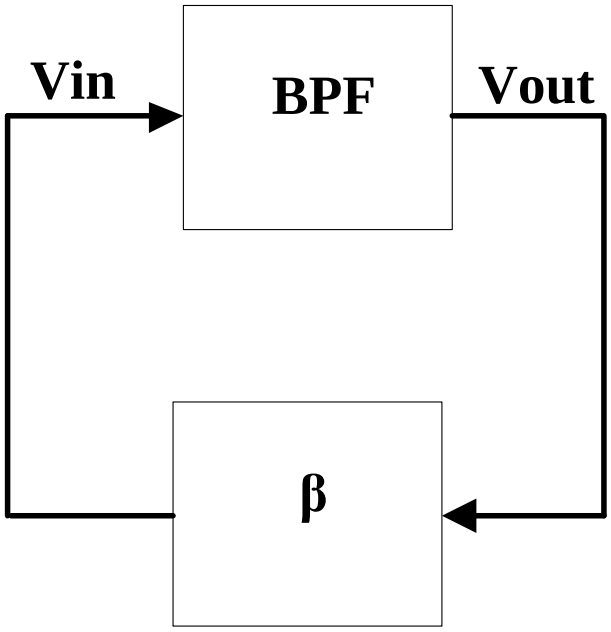


Figure 4.15 Block diagram of the BPF based oscillator

The open loop transfer function of a BPF in Figure 4.15 is

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{C_1}s}{s^2 + \frac{1 + C_1/C_2 + R_2/R_1}{R_2 C_1}s + \frac{1}{R_1 C_1 R_2 C_2}} \tag{4.14}$$

The oscillation frequency f_0 and minimum requirement g_m are given by

$$\omega_0 = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \tag{4.15}$$

$$g_m \geq \frac{1 + C_1/C_2 + R_2/R_1}{R_2} \tag{4.16}$$

The Q factor, is an important design parameter for the BPF based oscillator is given by

$$Q = \frac{\sqrt{(C_1/C_2)}.(R_2/R_1)}{1 + (C_1/C_2) + (R_2/R_1)} \tag{4.17}$$

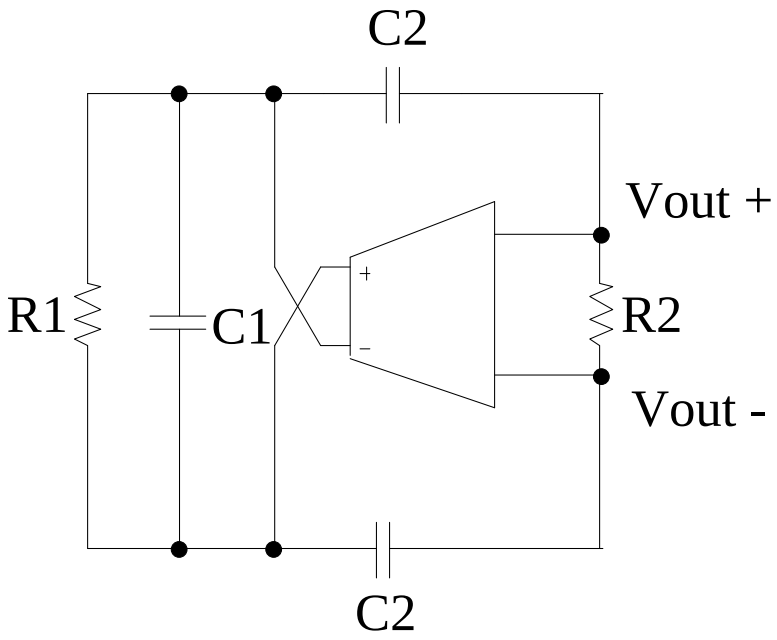


Figure 4.16 Block diagram of the BPF oscillator differential version

R_1, R_2, C_1, and C_2 form the BPF, and transistors M_1 and M_3 in Figure 4.16 take the voltage at the output of the BPF and transform these voltages to currents which are fed back to the BPF. For the positive feedback, a fully differential circuit is used. Transistor M_5 is used to bias the transistors M_1, M_2, M_3, and M_4. The common mode voltages of V^+_{out} and V_{out} (V_1) in Figure 4.17 is sensed by R_1 and used to bias the gate voltages of M_1, M_2, M_3, and M_4. When the g_m of M_1, M_2, M_3, and M_4 are set higher than the minimum requirement the oscillation starts and the oscillation frequency is set to ω_0.

The passive RC bandpass filter (BPF) based RC oscillator circuit was designed to avoid using an expensive inductor[27]. The oscillation frequency was determined by resistors and capacitors, the frequency is less susceptible to power supply noise[28]. The RC oscillator was designed to operate around 500MHz (Figure 4.19). This frequency was selected to transmit more bits before the system goes back to the standby mode.

If resistors and capacitors are chosen as $R_1 = R_2 = R$ and $C_1 = C_2 = C$ and f_0 = 500MHz, R = 4.586KΩ and C = 48.62fF

The bias voltage, vbias_RC was generated from the constant g_m bias circuit. In the passive RFID tag design, the RC oscillator circuit generates the clock signal for the 4-bit shift register block.

RC oscillator transistor sizes are given in Table 4.9.

Table 4.9 RC oscillator circuit transistor sizes

Component name	**Size**
M1	W = 10 µm L = 0.18 µm
M2	W = 10 µm L = 0.18 µm
M3	W = 20 µm L = 0.18 µm
M4	W = 20 µm L = 0.18 µm

M5	W = 6 µm L = 0.18 µm
R1	4.586 KΩ
R2	4.586 KΩ
R3	4.586 KΩ
R4	4.586 KΩ
C1	48.615 fF
C2	48.615 fF
C3	48.607 fF
C4	48.607 fF

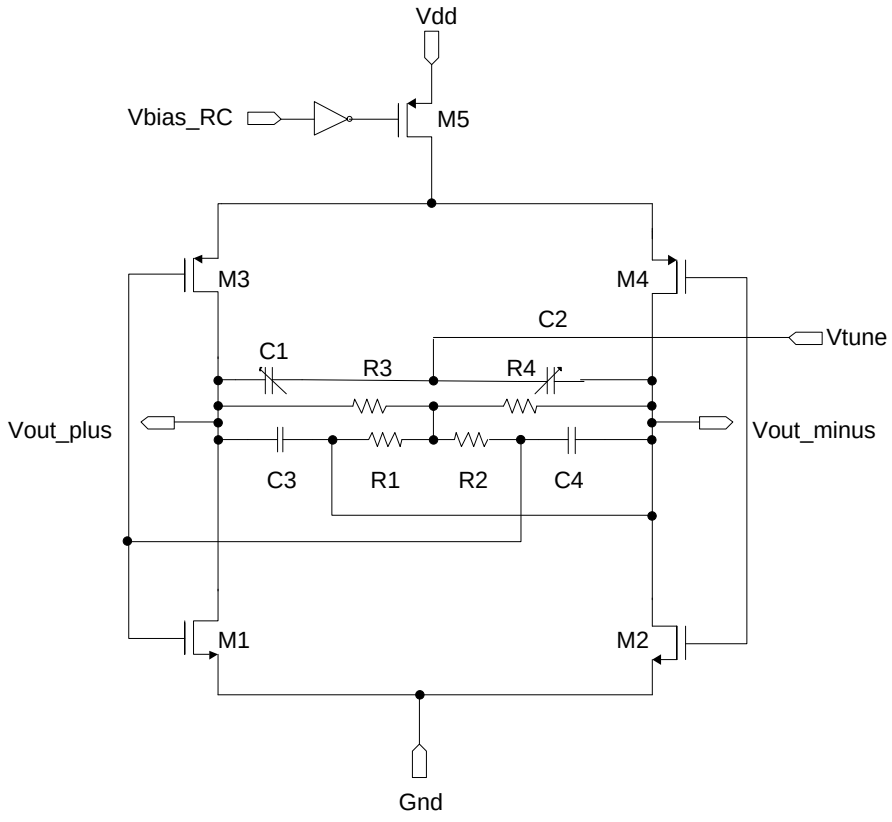


Figure 4.17 RC oscillator circuit

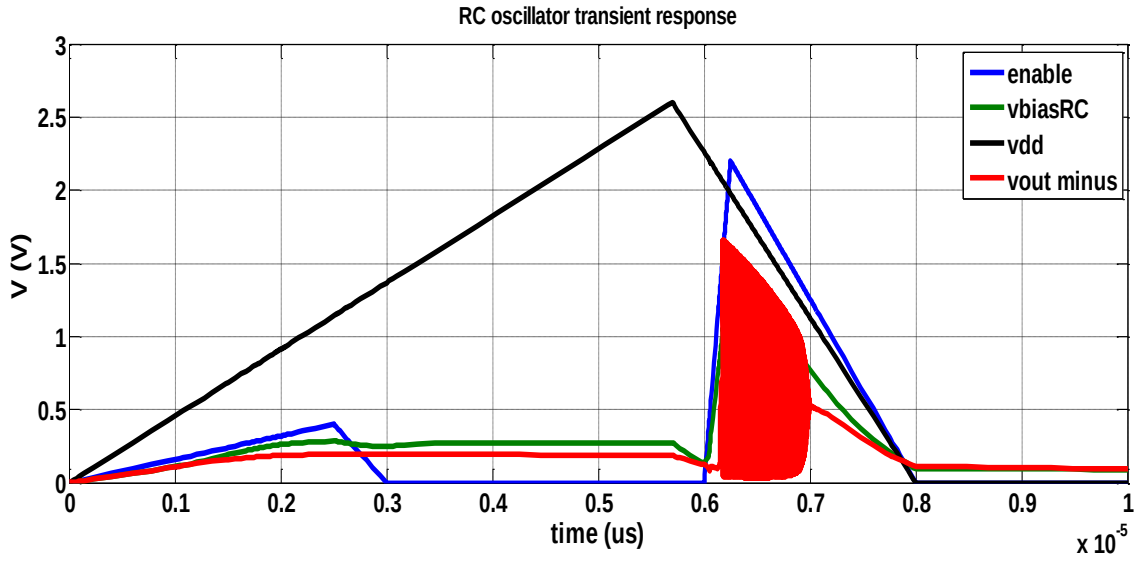


Figure 4.18 RC oscillator transient response with enable, vdd, and vbias_RC signals

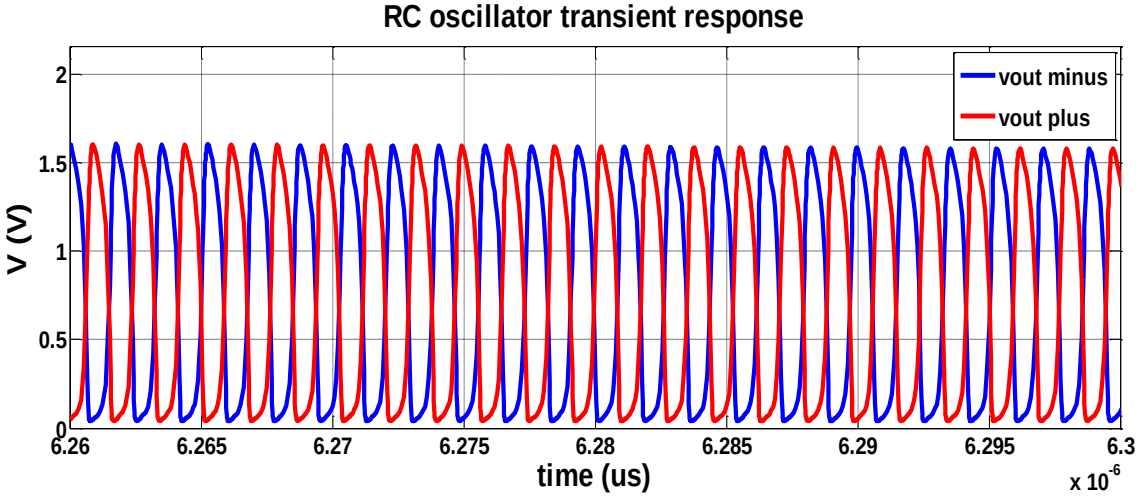


Figure 4.19 RC oscillator transient response

RC oscillator frequency = 499.8MHz

RC oscillator current consumption = $\frac{(1.0382mA+637.92\mu A)}{2}$ = 0.838*mA*

4.8 Delay Circuit

Delay circuit is a monostable device (Figure 4.20). Monostable element is a circuit that generates a pulse of predetermined width every time the quiescent circuit is triggered by a pulse or transition event. This is called monostable because it has only one stable state. A trigger event, which is either a signal transition or a pulse, causes the circuit to go temporary into another quasi-stable state. Therefore it will come to its original state after a time period determined by the circuit parameters. This circuit is called one-shot because it is useful in generating pulse of a known length. Delay element to control the duration of the pulse is one application of a one-shot circuit. In the XOR gate when both inputs are identical, the output is low. A transition on the input causes the XOR inputs to differ temporarily (Figure 4.20), and the output goes high. After the delay (t_d) is removed the output of the one shot trigger circuit becomes low. The pulse length of the t_d is created using chain of inverters or a RC network.

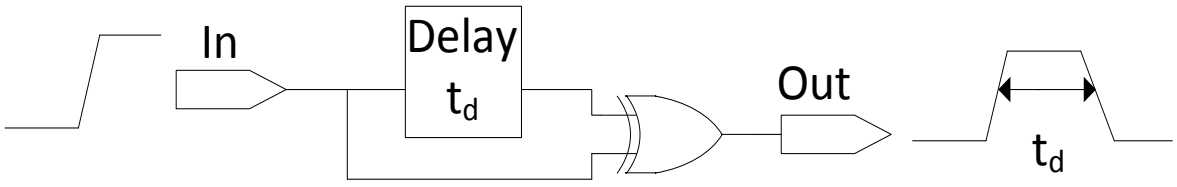


Figure 4.20 Transition triggered one-shot circuit

4.9 Injection Lock LC Oscillator

4.9.1 Theory of LC oscillator

A tank created by an ideal (lossless) inductor, L_t and ideal capacitor, C_t, will oscillate indefinitely after an external excitation is applied. The frequency of the oscillation is given by the natural frequency of the tank as

$$f_0 = \frac{1}{2\pi\sqrt{L_t C_t}} \tag{4.1}$$

Real inductors and capacitors are lossy. When an impulse is applied to the tank the oscillation will die after some time.

The negative resistance of the LC oscillator can be generated by a cross couple pair of active elements such as transistors as shown in Figure 4.21. Here the PMOS transistors are connected to a current source providing the tail current.

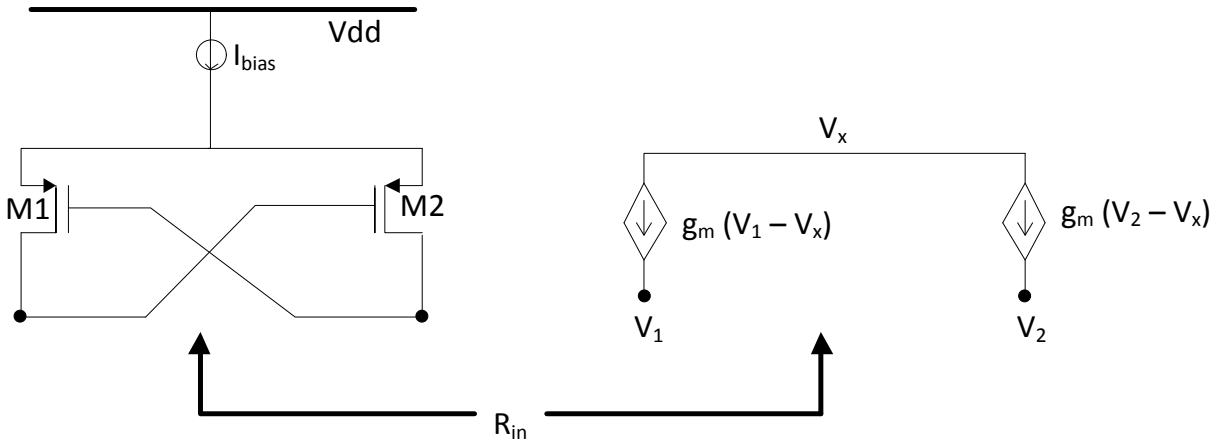


Figure 4.21 Schematic and small signal model of cross coupled pair

The input impedance R_{in} of the circuit

$$R_{in} = \frac{V_2 - V_1}{I_{in}} \tag{4.2}$$

$$I_{in} = g_m(V_1 - V_x) - g_m(V_2 - V_x) \quad (4.3)$$

$$I_{in} = g_m(V_1 - V_2) \quad (4.4)$$

Therefore $R_{in} = -\frac{1}{g_m}$ (4.5)

Therefore the cross coupled transistor pair has a input resistance of $1/g_m$. In order to sustain the oscillation the negative resistance generated by the cross coupled pair should be equal to the negative resistance of the tank. As a result it is common practice to have the small signal negative resistance at least two or three times higher than the parallel resistance value to guarantee the start of the oscillation. Therefore the LC oscillator oscillates if

$$-\frac{1}{g_m} > R_p \Rightarrow \frac{1}{g_m} < R_p \quad (4.6)$$

To start up the oscillation $R_p > 3\frac{1}{g_m}$ (4.7)

4.9.2 Injection locking of LC oscillators

The Dutch scientist Christiaan Huygenns, observed that pendulums of the two clocks hung on the same wall oscillated in phase, if the clocks were brought close enough, but oscillated independently, oscillated independently when they were placed part.

The proposed architecture employs a negative resistance LC oscillator (Figure 4.22). The injection of a weak periodic signal into a more powerful free-running oscillator may give rise to a variety of injection locking phenomena. Free-running oscillator (also name slave oscillator) leaves its natural frequency to synchronize with the external signal; it then gets phase locked to the injected signal from the master oscillator. Depending on the ratio of the injection frequency to the free-running frequency, injection locking can be categorized into three distinct types: first-harmonic, subharmonic, and superharmonic.

When a free running LC oscillator is injected with a harmonic signal f_i, as shown in Figure 4.22, the oscillator will lock to and track the injected signal over a certain frequency locking range. The locking range depends on the amplitude of the locking signal and the value of the tank inductor. Locking range can be increased by either increasing the amplitude of the injection signal or increasing the value of the inductance. The injection lock LC oscillator circuit is indicated in Figure 4.23. LC oscillator free running transient response and LC oscillator transient response with RF signal at 5.8 GHz are indicated in Figures 4.24 and 4.25. LC oscillator transistor sizes are mentioned in Table 4.11.

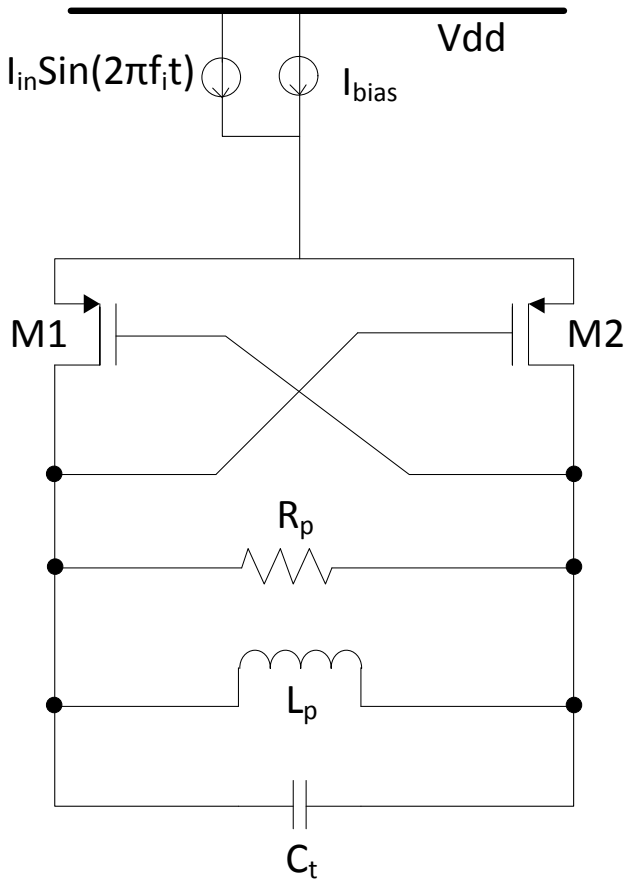


Figure 4.22 Schematic of an injection lock LC oscillator circuit

Table 4.10 LC oscillator circuit transistor sizes

Component name	**Size**
M1	W = 10 µm L = 0.18µm
M2	W = 10 µm L = 0.18µm
M3	W = 180 µm L = 0.18µm
C1	300 fF
C2	52.11 fF
C3	52.11 fF
L1	1.763 nH
L2	1.763 nH
R1	50 Ω

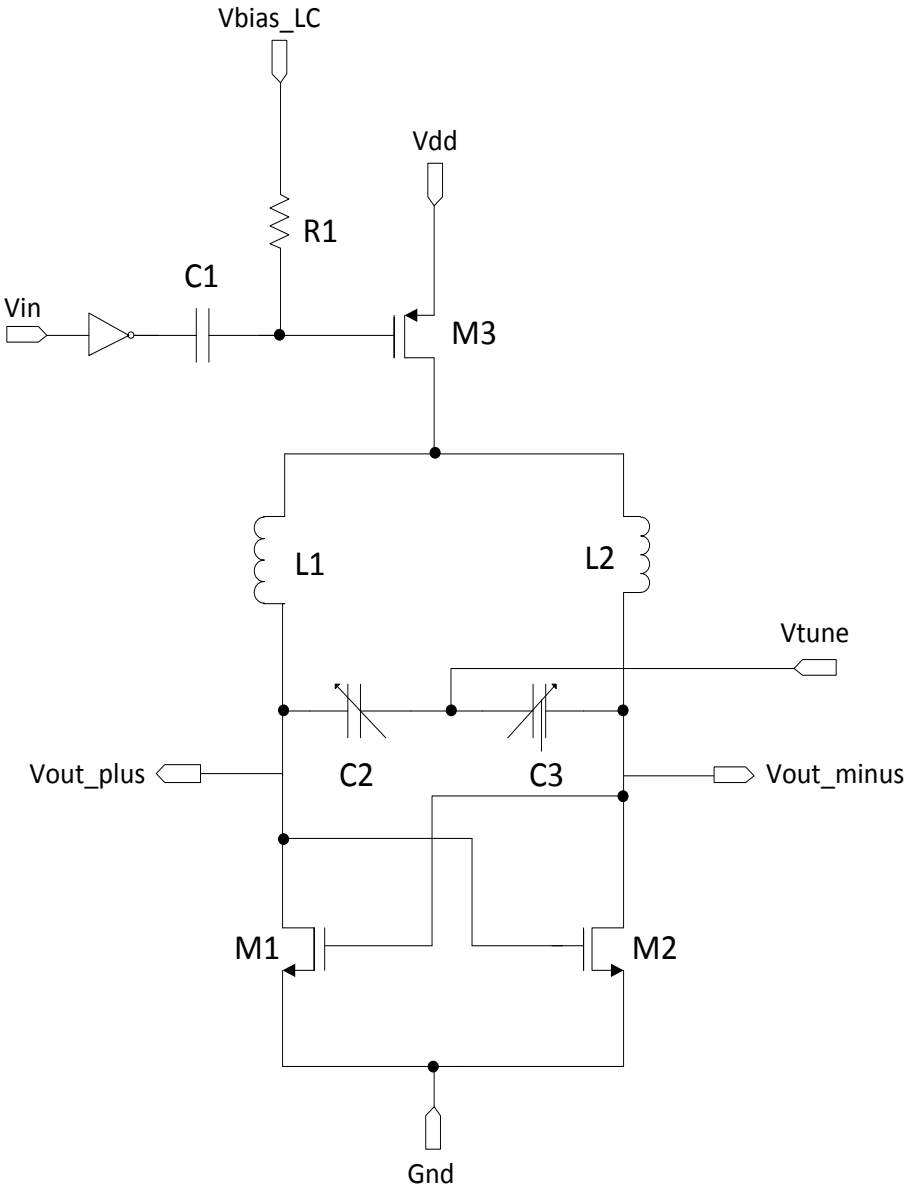


Figure 4.23 Injection lock LC oscillator circuit

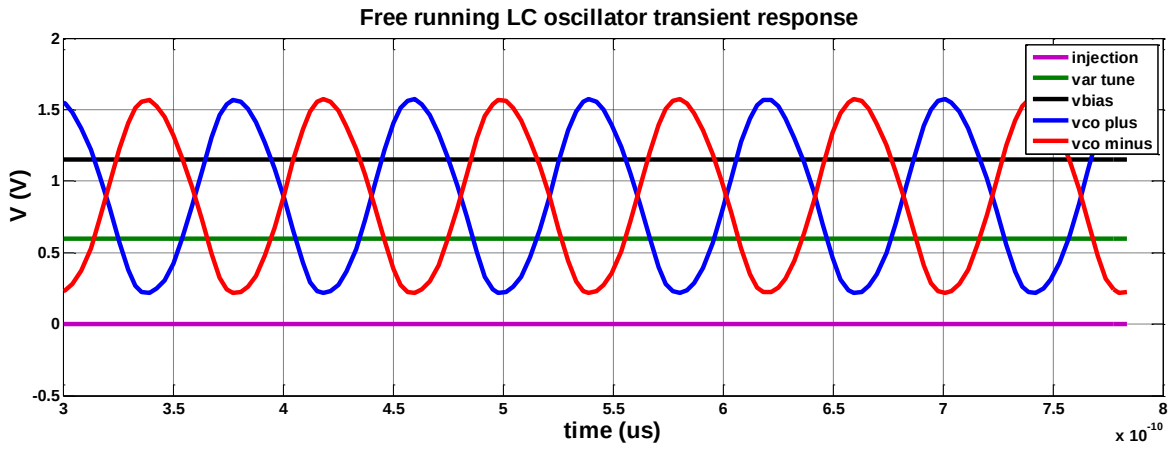


Figure 4.24 LC oscillator free running transient response

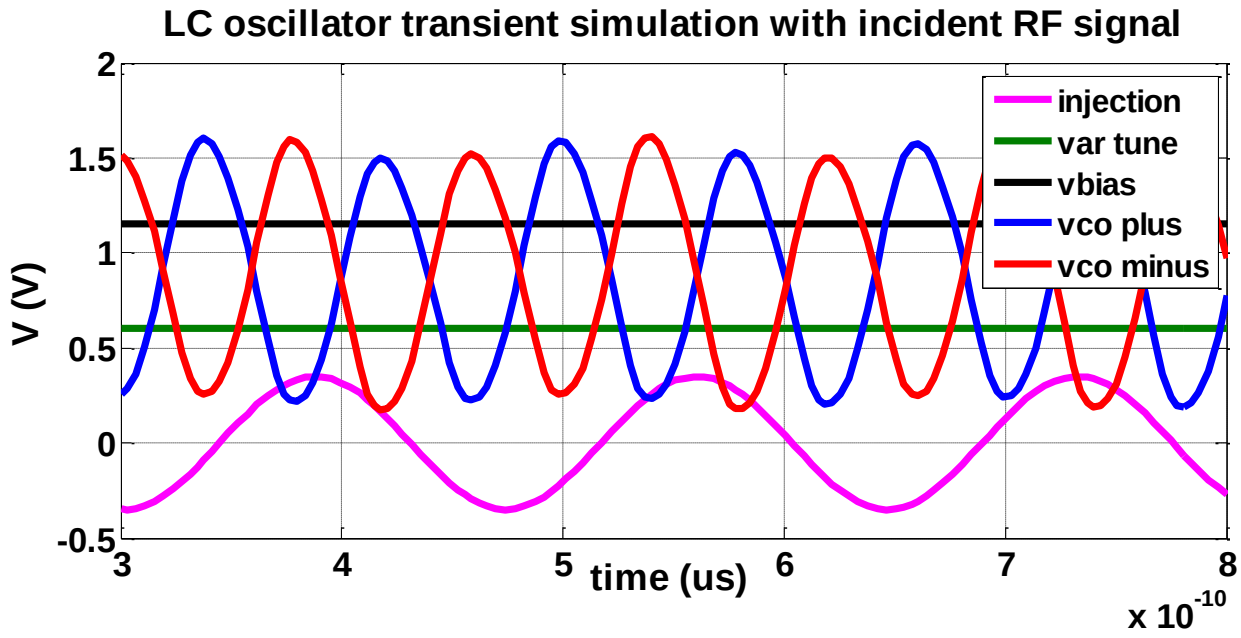


Figure 4.25 LC oscillator transient response with RF signal at 5.8GHz

Table 4.11 LC oscillator circuit transistor sizes

	Case 1	**Case 2**	**Case3**
V_{dd} (V)	1.2	1.5	2
Injection_Amplitide	450mV	450mV	450mV
V_{in} (GHz)	5.8	5.8	5.8
V_{bias}_LC	450mV	463.2mV	455.61mV
Frequency (GHz)	11.47	11.36	11.34

The bias voltage (vbias_LC) was generated from the constant g_m bias circuit. The capacitor is used to block DC. Injection lock oscillator circuit works in the active mode. Therefore it oscillates when the enable signal is high.

4.10 Power Amplifier

Power amplifier (PA) is a two stage amplifier with both driver and output stages having class A operation was designed to resonate at 11.6GHz (Figure 4.26). The power amplifier was used to drive the 50Ω antenna. A single CMOS transistor was used and loaded with a RF choke, which acted like an ideal current source [29]. The bias voltages of the first and second stages of the power amplifier were generated from the constant g_m bias generator circuit. The resistors of each stage of the power amplifier isolate the AC from DC. The power amplifier goes into standby mode with the rest of the system, during the charging mode. When the enable signal is high constant g_m bias generator circuit provides the bias voltages to the PA and is in the active mode. When the enable signal is low it doesn't provide the correct bias voltages to turn on the CMOS transistors of the PA. Therefore the PA goes into standby mode.

In the passive RFID tag design, the power amplifier amplifies the signal received from the LC oscillator and matches the load to a 50Ω antenna. The 11.6 GHz sinusoidal signal from the injection lock LC oscillator was fed into the gate of the lower transistor. The pulsed digital data was fed into the gate of the other transistor. The modulation depends on both the bias condition of the two gates and the device dimensions. The modulation occurs when the device operates in the saturation or in the cut-off region, that is when there is '1' or '0' coming from the digital data [28]. The top transistor acts as a switch and is turned on the high state of the digital data and remains off at the low state, maintaining the OOK modulation scheme

In low frequencies the multiplexers were used in the literature. In this proposed, novel approach a CMOS switch is used to provide the OOK modulation for the bits of the RFID tag.

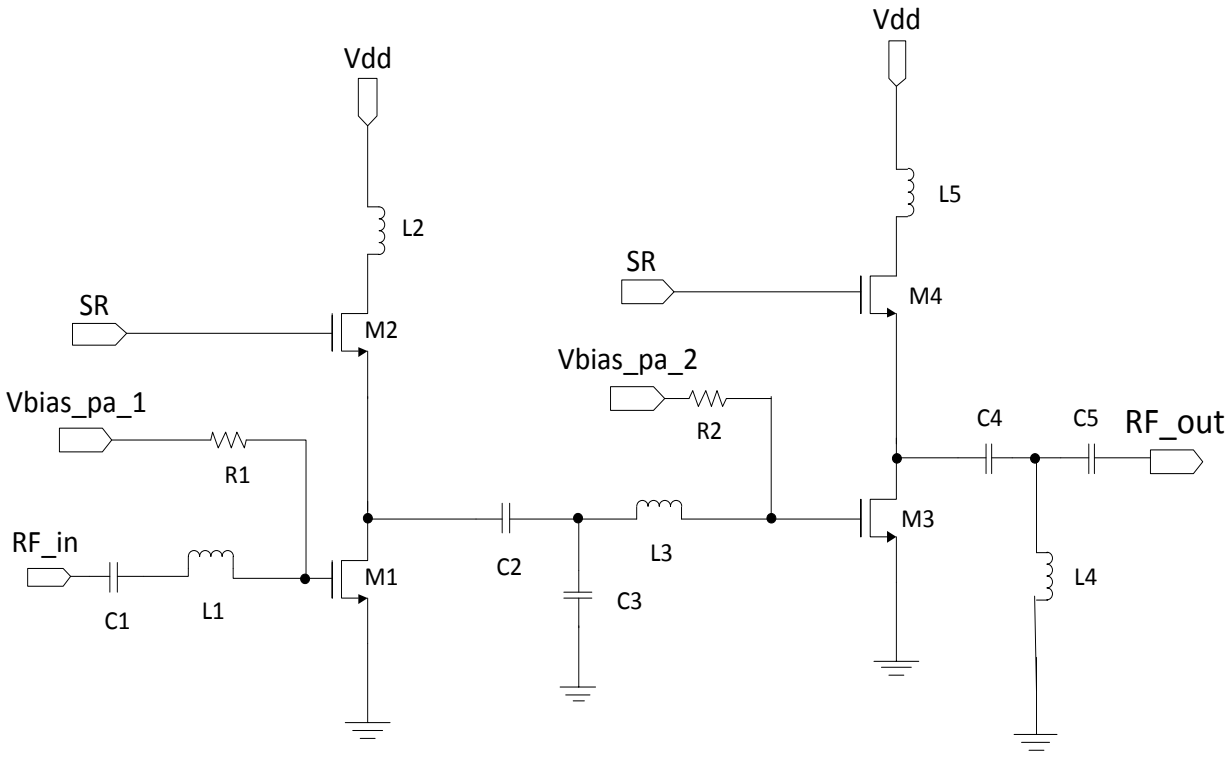


Figure 4.26 Two stage class A PA circuit with output of the shift register

4.10.1 Output power

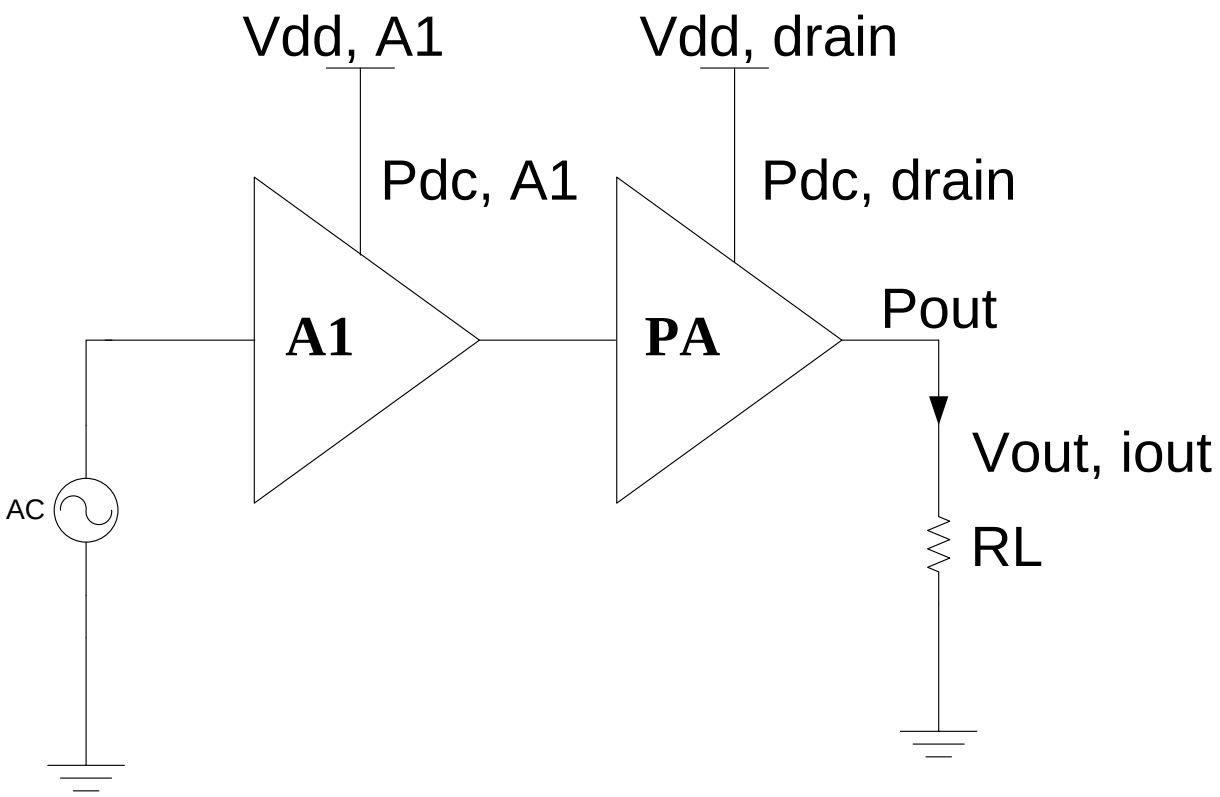


Figure 4.27 PA with driver stage A_1 connected to an antenna

PA with driver stage A_1 connected to an antenna is shown in Figure 4.27. The power generated at the fundamental frequency is called P_{out}.

$$P_{out} = \frac{A^2}{2R_L} = \frac{V^2_{out,max}}{2R_L} = \frac{V^2_{out,rms}}{R_L} \tag{4.2}$$

4.10.2 Gain and efficiency

Gain (G) of the PA can be defined as the ratio of the output power (P_{out}) and the input power (P_{in}) which is expressed in dB

$$G_{dB} = 10log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (4.3)$$

The Drain Efficiency (DE), which is defined as the ratio between the average output power at the fundamental (P_{out}), and the DC power consumption ($P_{DC,drain}$) of the very last stage of the PA. Therfore

$$DE = \frac{P_{out}}{P_{DC,drain}} \quad (4.4)$$

$$PAE = \frac{P_{out}-P_{in}}{P_{dc,tot}} \quad (4.5)$$

X band power amplifier transistor sizes are given in Table 4.12 and X band Power amplifier transient sizes optimization are shown in Table 4.13.

Table 4.12 X band Power amplifier transient sizes

Transistor name	**Sizes**
M1	50/0.18 µm
M2	30/0.18 µm
M3	60/0.18 µm
M4	90/0.18 µm
L1	1.323nH
L2	1.621nH
L3	411pH
L4	1.303nH
L5	1.284nH
C1	200fF

C2	200fF
C3	10.3fF
C4	120fF
C5	400fF
R1	10KΩ
R2	5KΩ

Table 4.13 X band Power amplifier transient sizes optimization

M1 (W/L) µm	**M2 (W/L) µm**	**M3 (W/L) µm**	**M4 (W/L) µm**	**RF_out (V)**	**RF_freq. (GHz)**	**Delay (ns)**
50/0.18	9/0.18	60/0.18	30/0.18	0.433	10.48	0.9576
50/0.18	9/0.18	60/0.18	60/0.18	0.624	10.49	0.903
50/0.18	9/0.18	60/0.18	90/0.18	0.721	10.48	0.901
50/0.18	9/0.18	60/0.18	120/0.18	0.702	10.48	0.934
50/0.18	12/0.18	60/0.18	90/0.18	0.748	10.48	0.789
50/0.18	18/0.18	60/0.18	90/0.18	0.764	10.48	0.785
50/0.18	22/0.18	60/0.18	90/0.18	0.77	10.48	0.857
50/0.18	24/0.18	60/0.18	90/0.18	0.778	10.86	0.852
50/0.18	30/0.18	60/0.18	90/0.18	0.76	10.83	0.856

Transistor sizes were optimized to get the maximum RF_out voltage from the power amplifier. More RF_out voltage betters the voltage gain of the power amplifier. When the transistor sizes were optimized, consideration was made that the power amplifier frequency was

still at the X-band frequency, and the delay between RF_out and Q (Figure 4.28) signal was minimum. Less delay between the RF_out and Q signal betters the switching of the power amplifier. The delay between RF_out and Q signal is important for the On-off_keying amplitude modulation (Figure 4.28) performance of the power amplifier.

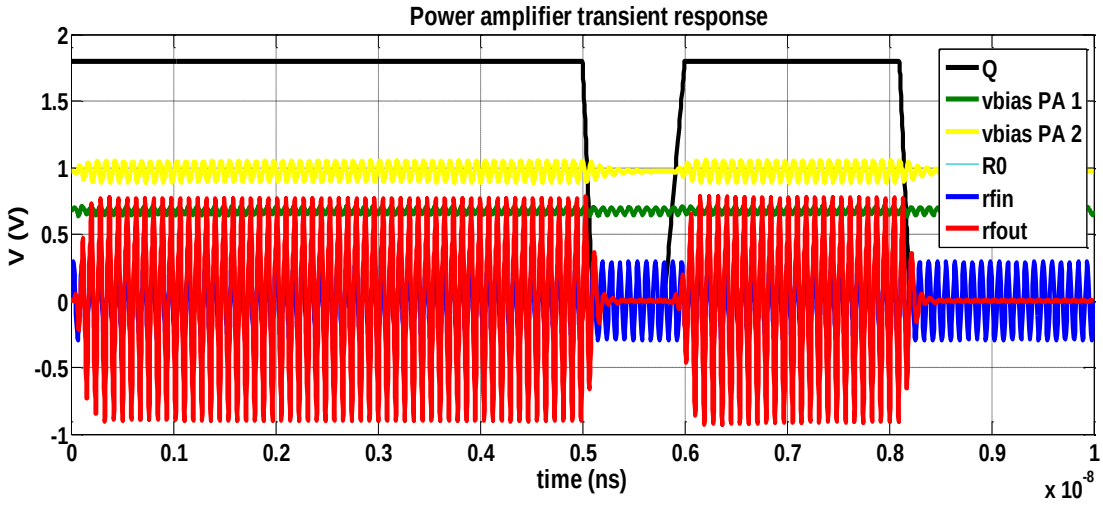


Figure 4.28 Power Amplifier transient response

4.11 5-bit Parallel In Serial Out Shift Register

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

More generally, a shift register may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). In the PISO configuration has the data input lines D1 through D5 in parallel format, where D5 is the MSB. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the Write/Shift control line is set to high and the registers are clocked in a synchronize clock.

In the RFID tag design, it is assumed tag id is a 5 bit static id. The number of bits a tag transfers depends on the discharging time of the capacitor and the clock frequency. We have designed 5-bit Parallel in Serial out shift register for sending the 5 bits of the RFID tag. Each bit of the shift register corresponds to a bit in the RFID tag. The final output of the shift register is the serial version of the 5 bit parallel tag id. At least 5 clock cycles are needed to shift a 5 bit tag id from parallel to serial. Each stage of the five bit shift register consists of an edge triggered dynamic D flip-flop. The 5-bit parallel in Serial out shift register is given in (Figure 4.29).

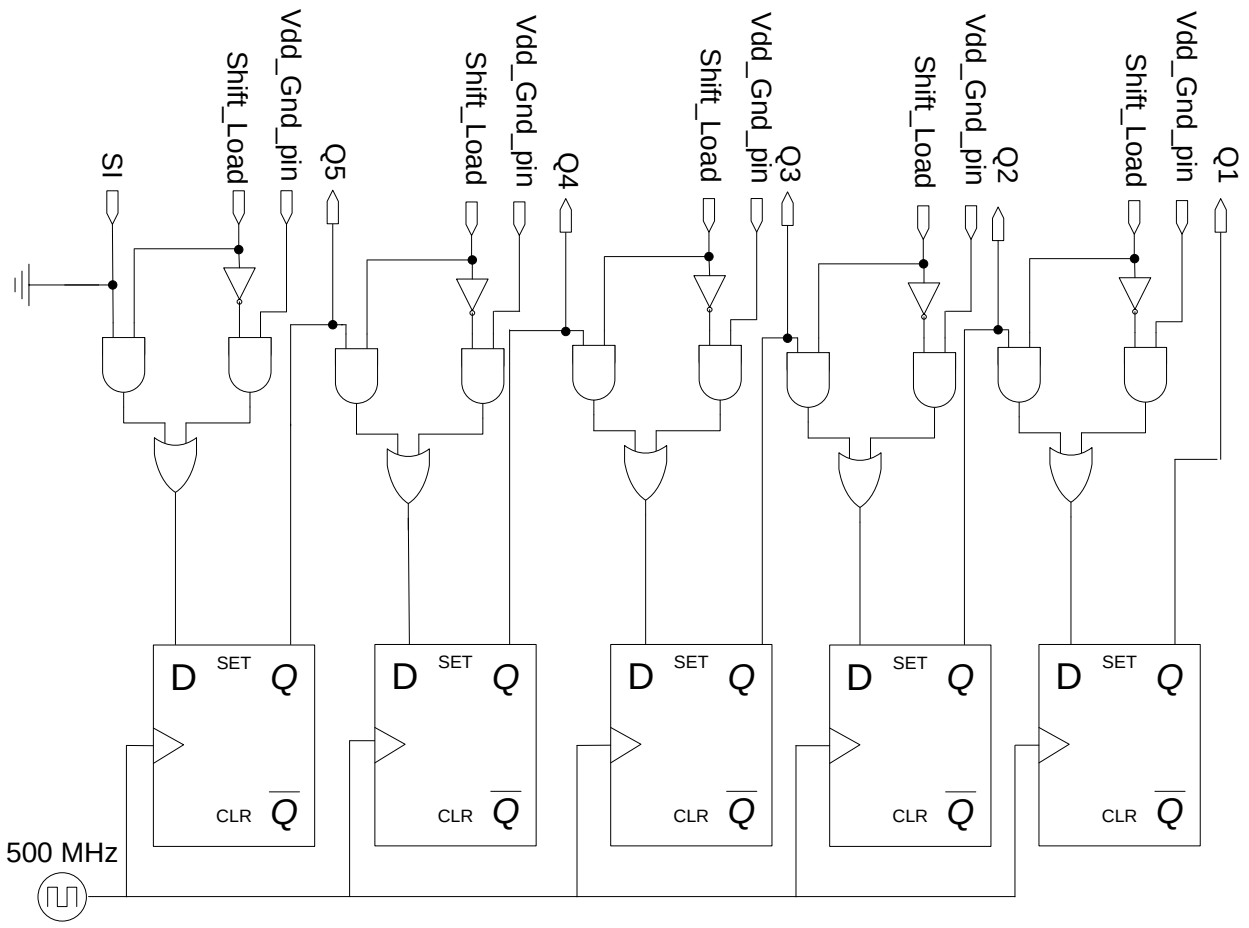


Figure 4.29 5-bit Parallel in Serial out shift register

4.11.1. Edge-triggered dynamic D flip-flop

An efficient functional alternative to a D flip-flop can be made with dynamic circuits (where information is stored in a capacitance) as long as it is clocked often enough; while not a true flip-flop, it is still called a flip-flop for its functional role. While the master–slave D element is triggered on the edge of a clock, its components are each triggered by clock levels. The "edge-triggered D flip-flop", as it is called even though it is not a true flip-flop, does not have the master–slave properties.

Edge-triggered D flip-flops are often implemented in integrated high-speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. A common dynamic flip-flop variety is the True Single-Phase Clock (TSPC) type (Figure 4.30) which performs the flip-flop operation with little power and at high speeds. A common dynamic flip-flop variety is the true single-phase clock (TSPC) type which performs the flip-flop operation with little power and at high speeds. However, dynamic flip-flops will typically not work at static or low clock speeds: given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states. D flip flop circuit transistor sizes are given in Table 4.14 and TSP D-FF transient simulation is indicated in Figure 4.31.

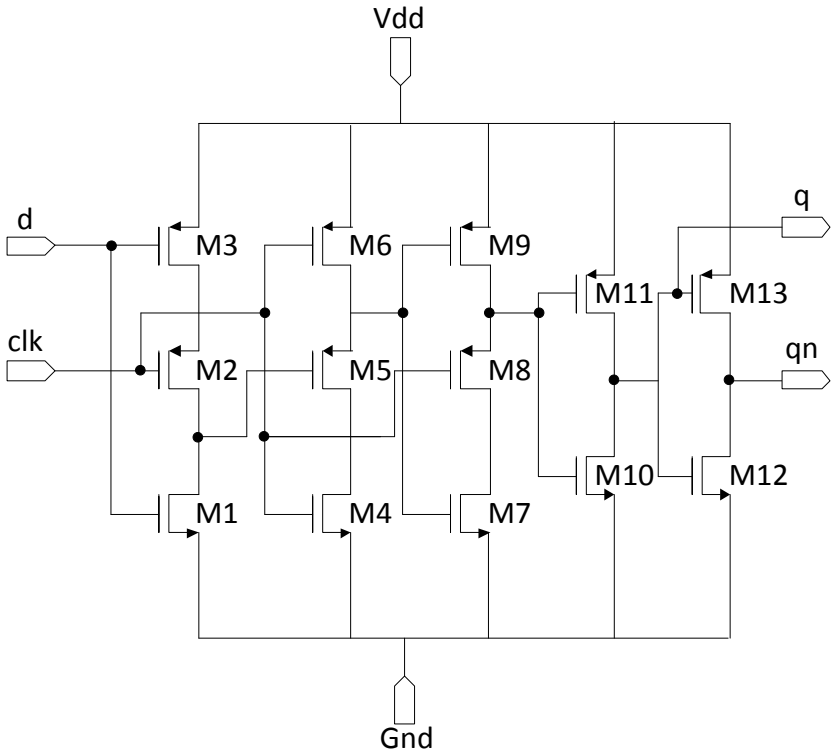


Figure 4.30 TSP D-FF schematic

Table 4.14 TSP D flip flop circuit transistor sizes

Transistor name	**W/L (µm)**
M1	2/0.18
M2	4/0.18
M3	4/0.18
M4	2/0.18
M5	2/0.18
M6	4/0.18
M7	2/0.18
M8	2/0.18
M9	4/0.18
M10	2/0.18
M11	4/0.18
M12	2/0.18
M13	4/0.18

TSP D-FF current consumption = $(675.306\mu A + 477.47\mu A)/2 = 576.38\mu A$.

When the input ‘D’ is 1V, in the rising clock edge ‘q’ is 1.3V and ‘qbar’ is 0Vs.

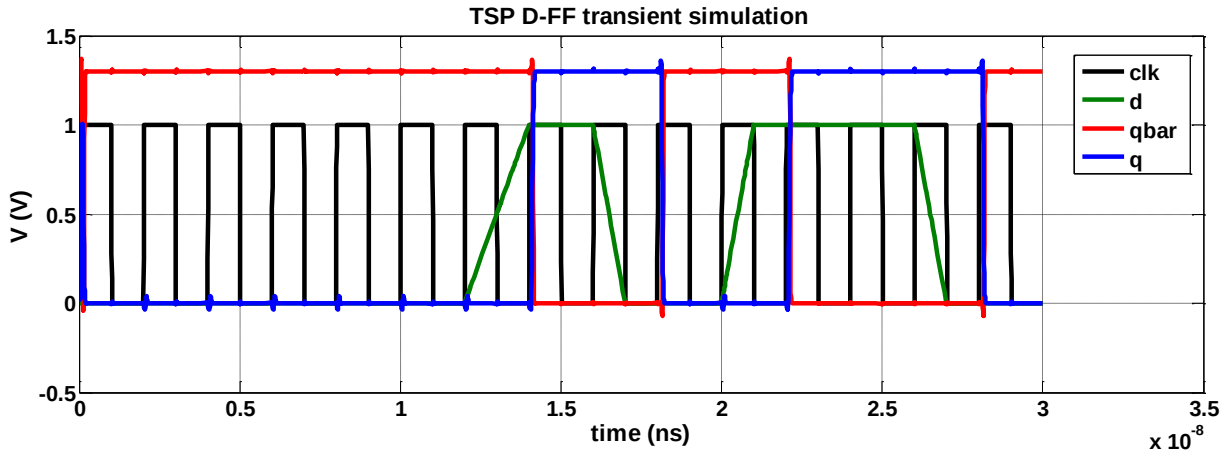


Figure 4.31 TSP D-FF transient simulation

4.12 RFID Final Simulation

The final overall simulation of the RFID tag for the bit pattern 10110 is given below. This is the final output (Figure 4.32) after connecting RF-DC rectifier, mode selector, Schmitt trigger circuit, 5 bit shift register, RC oscillator, LC oscillator, and X-band PA. RF-DC rectifier generates a power supply voltage of 2.2 V.

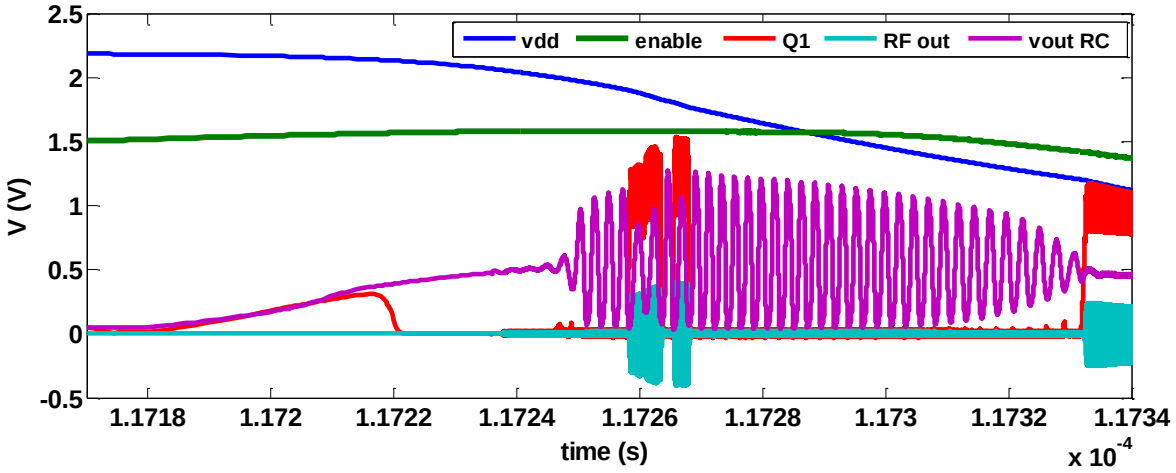


Figure 4.32 RFID final simul

CHAPTER 5

X-band Antenna

X-band antenna is the most important building block of the RFID tag design. Its characteristics affect the overall efficiency of the WPT systems in many ways. In general an antenna has a complex input impedance which can be written in the form $Z_{ant} = R_A + jX_{ant}$ and $R_A = R_{loss} + R_s$. R_s is the radiation resistance of the antenna, R_{loss} is the lost resistance of the antenna and X_{ant} is the imaginary part of the antenna input impedance.

A typical WPT system is given in Figure 5.1. The Effective Isotropically Radiated Power P_{EIRP} equal to $P_{RF}G_{PA}G_{t,}$ is radiated in the direction of the battery less device situated at a distance *d*.

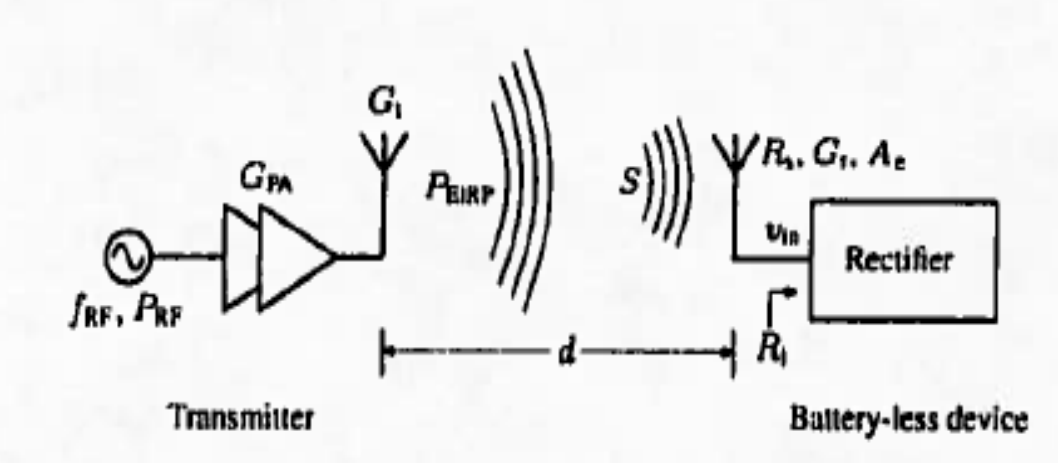


Figure 5.1 Typical WPT system [15]

$$S = P_{EIRP}\ \frac{1}{4\pi d^2} \tag{5.1}$$

Power collected P_r collected by the device antenna and transferred to the load is

$$P_r = A_e S \tag{5.2}$$

Where A_e is the effective aperture of the antenna. The maximum aperture related to the antenna gain G_r and wavelength λ_{RF} is given by

$$A_e = \frac{\lambda^2_{RF}}{4\pi} G_r \quad (5.3)$$

Therefore

$$P_r = S\frac{\lambda_{RF}{}^2}{4\pi} G_r = P_{EIRP} G_r \frac{\lambda_{RF}{}^2}{(4\pi d)^2} \quad (5.4)$$

Equation 5.4 is known as the Friss relation.

The voltage source amplitude (v_s) is equal to

$$v_s = 2\sqrt{2R_s} P_{av} \quad (5.5)$$

If the rectifier is modeled as a Resistive load (R_i), the input voltage v_{in} is equal to

$$v_{in} = v_s \frac{R_i}{R_i + R_s} = 2\sqrt{2R_s} P_{av} \cdot \frac{R_i}{R_i + R_s} \quad (5.6)$$

Now by using (5.6) the input voltage of the rectifier is

$$v_{in} = 2\sqrt{2R_s} P_{av} \cdot \frac{R_i}{R_i + R_s} = 2\sqrt{2R_s} \frac{R_i}{R_i + R_s} \sqrt{P_{EIRP}} \frac{\lambda_{RF}}{4\pi d} \sqrt{G_r} \quad \text{where } P_{av} = P_r \quad (5.7)$$

From equation (5.7) v_{in} is inversely proportional to the distance (d), where d is the distance between the transmitting antenna and the passive rfid tag.

Antenna design and placement play a significant factor in coverage zone, range, and accuracy of communication of a tag, because the antenna both draws the energy from the reader's signal to energize the tag and sends the data that are received from the reader [30]. Antennas in the RFID front end have been designed to match 50Ω load. A RFID tag antenna has to be directly matched to the IC chip, which primarily exhibits complex input impedance. Maximum power must be delivered from the antenna to the IC to maximize the performance of the transponder.

Fully integrated passive RFID tag is the ideal solution to dramatically reduce the costs and sizes of RFID tags. In order to achieve this goal, three basic requirements are necessary: high gain on- chip antenna, high efficiency RF-DC converter and ultra-low power mixed

signal circuitry.

Out of three types of RFID tags (active, passive and semi-passive), passive tags attract broad interests due to its low cost and long life time. Passive tags utilize antennas to harvest RF energy for all their operations, so the antenna design for passive tags are critical for their performance[6]. The type of antenna used by RFID tags is closely related to the target applications. For example, patch antennas are well suited for metallic objects since it is possible to make use of their bodies as a ground plane [7-8].

The integration of the antenna with the RFID tag is the final hurdle to achieve a fully integrated single-chip wireless system with largely reduced cost and form factor. Low radiation efficiency is the main problem of the previous studies involved in developing on-chip antennas [9]. In this paper, we propose an on-chip antenna structure operating in the X-band frequency and compare it with the existing antenna designs. The proposed antenna, the patch antenna, and the symmetric dipole antenna with balun were designed, simulated and optimized in Sonnet software.

5.1 On-Chip Asymmetric Dipole Antenna Design

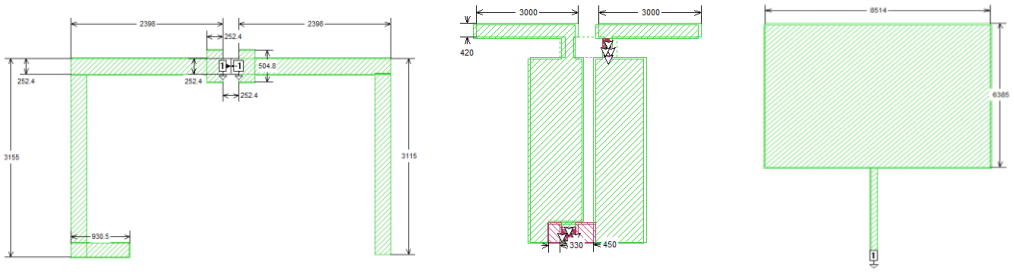
The layout of the proposed antenna is shown in Figure 5.2(a) with differential port. It is an asymmetric dipole antenna. Its overall electrical length from the feed point to end of the long section is about a quarter wavelength ($\lambda_0/4$) at the resonance frequency of operation. The final electrical dimensions of the antenna are $0.17\lambda_0$ by $0.1\lambda_0$. Throughout the antenna design process, asymmetric dipole antenna exhibits superior performance over symmetric dipole and patch antennas. The IBM 0.18μm six-metal layer CMOS process is used for electromagnetic analysis of the antennas. The dielectric stack starts with 700μm silicon with a loss tangent of

0.004, and conductivity of 7.41S/m. The conductive layer is defined as 5μm thick aluminum film. The complete IBM PDK 0.18μm dielectric stack is given in Table 5.1.

Table 5.1 Substrate stack description for Sonnet simulation

Thickness	**Mat. Name**	**Erel**	**Dielectric**	**Diel Cond.**
10000.0	Air	1.0	0.0	0.0
4.3	AM	3.8	0.0	0.0
4.0	SiO_2	4.1	0.0	0.0
6.7	SiO_2	4.1	0.0	0.0
700.0	Silicon	11.9	0.004	7.41

Symmetric dipole antenna mentioned [10] in Figure 5.2(b) consists of a via-hole balun acts as an unbalanced to balanced transformer between the feed coaxial line and the two printed dipole strips. The structure is resized to fit 10GHz application. The length of the dipole strips is approximately 1/4 of the wavelength. The ground plane of the microstrip line and the dipole strips are in the same plane. The widths of the dipole arm strips are chosen to be approximately one-tenth of the wavelength. The patch antenna in Figure 5.2(c) is designed so that one side is half wavelength [31]. When building it on a substrate it can be fed through a microstrip line.



(a) (b) (c)

Figure 5.2 Antenna layouts for (a) asymmetric dipole antenna with differential port, (b) Symmetric dipole antenna with balun, and (c) patch antenna.

5.2 On-chip Slot Antenna Design

Integration of antenna with the rest of the transceiver on a single IC is the last barrier in achieving a totally integrated single chip wireless system. This antenna has much higher gain and efficiency compared to other on-chip antennas operating in the same frequency.

CHAPTER 6

Experimental Results

Experimental results were taken according to the following test plan.

Test plan for chip 1

1. Antenna circuit

1. Set the synthesized sweeper frequency to 10GHz
2. Generate EM waves from the horn antenna that is connected to RF_OUTPUT of the synthesized sweeper
3. Power amplifier between synthesized sweeper and horn antenna may be needed to increase the signal strength at the antenna
4. Set the power level to result determined by Friis Equation.
5. Set antenna height to result determined by Friis Equation.
6. The DC_OUT will be connected to a pin connector and that will be connected to the parameter analyzer to measure the voltage

2. RF-DC rectifier circuit without matching

1. The DC_OUT will be connected to a pin connector and that will be connected to the parameter analyzer to measure the voltage
2. Set the synthesized sweeper frequency to 10GHz
3. Set the power level to -8.1dBm
4. The Synthesized sweeper RF OUTPUT is connected to The RF_IN through the sma connector.

3. ZVT transistor

1. The Vout will be connected to a pin connector and that will be connected to the SMU3 triaxial cable of the parameter analyzer to measure the voltage.
2. The Vin will be connected to a pin connector and that will be connected to the SMU2 triaxial cable of the parameter analyzer to measure the voltage
3. Channel definition screen will be set as follows.

   SMU3(VNAME→ Vd, INAME→ Id, MODE→V, FCTN→ VARI).

   SMU2(VNAME→ Vg, INAME→ Ig, MODE→V, FCTN→ VARI).

   SMU1(VNAME→ Vs, INAME→ Is, MODE→COMMON, FCTN→ CONST).

3. Gate voltage Vin will be swept from 0 V to 1.8 V is assigned to the X axis.

4. Shunt inductor with antenna

1. Set the synthesized sweeper frequency to 10GHz
2. Set the power level to -8.1dBm
3. The Synthesized sweeper RF OUTPUT is connected to The RF_IN through sma connector.
4. The DC_OUT will be connected to a pin connector and that will be connected to the parameter analyzer to measure the voltage

6.1 RF-DC Rectifier

The energy harvester and its building blocks were successfully fabricated in 0.18-µm CMOS process. The fabricated circuit building blocks include; (i) 6-stage RF-DC rectifier, (ii) 6-stage RF-DC rectifier with different matching circuits, (iii) slot antenna, and (iv) Integrated 6-

stage RF-DC rectifier with slot antenna.

6.1.1 Rectifier with and without matching circuits

Figure 6.1 shows the layout of the RF-DC rectifier with series inductive matching and the probe setup for measurement [32]. The RF signal was generated by Agilent 8341A vector signal generator. Figure 6.2 shows the output voltage of the RF-DC rectifier as a function of input RF frequency. The rectifier with series inductor matching shows the highest output voltage in the frequency range from 9.0 GHz to 9.6 GHz. The rectifier with parallel inductor and series capacitor matching also shows conversion peak at about 9.5 GHz, but with significantly lower output voltage. Meanwhile, the rectifier without any matching produces significantly lower output voltage in the X band as expected.

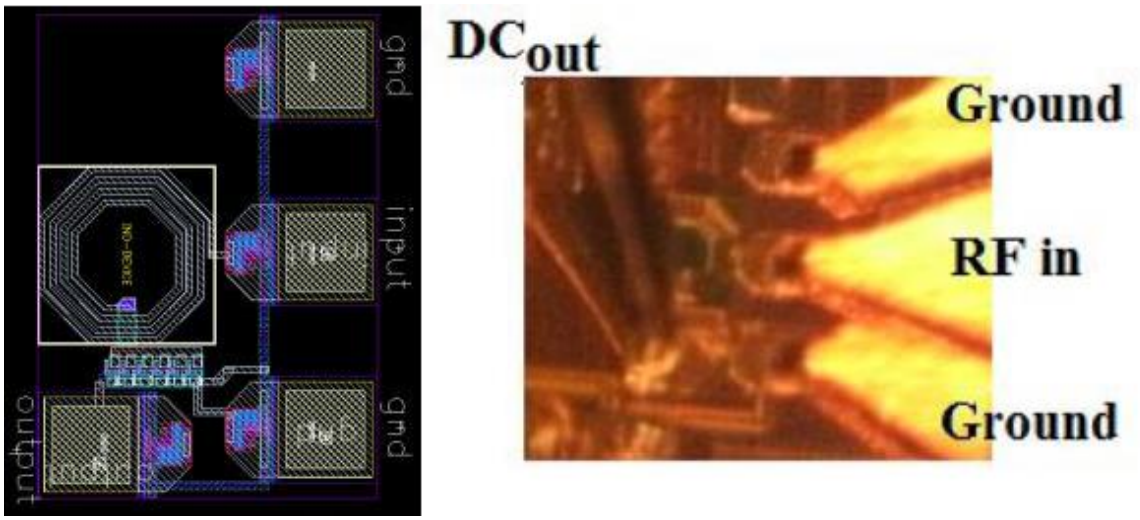


Figure 6.1 Layout and probing setup of series inductive matched RF-DC Rectifier

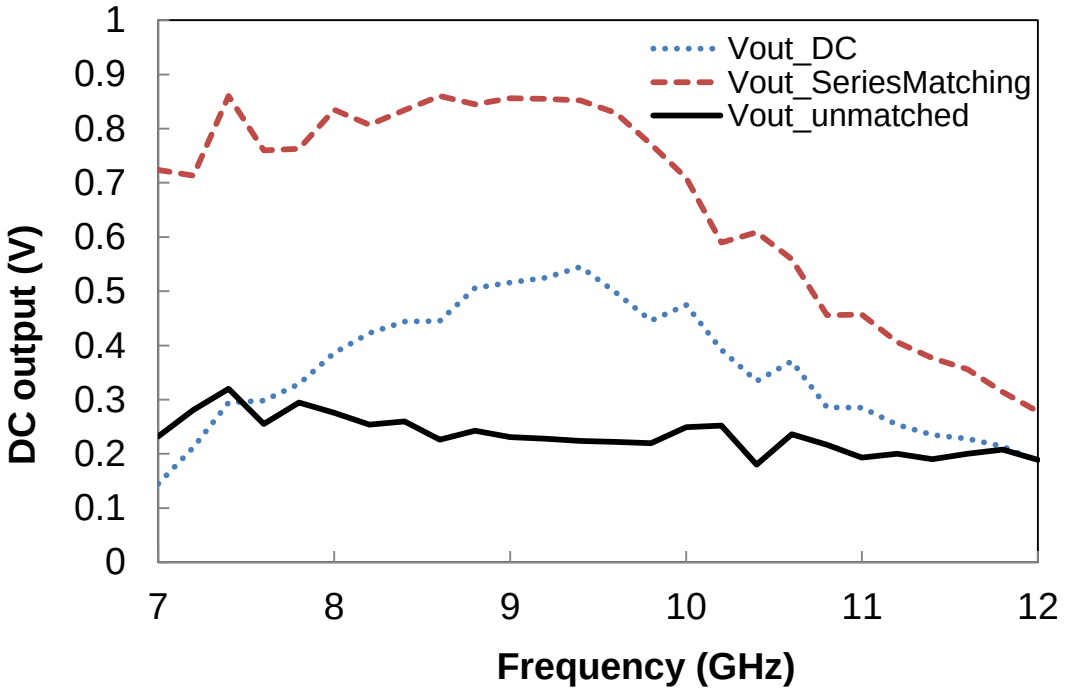


Figure 6.2 Rectifier output voltage versus RF frequency for -10 dBm input power and 304 KΩ load impedance

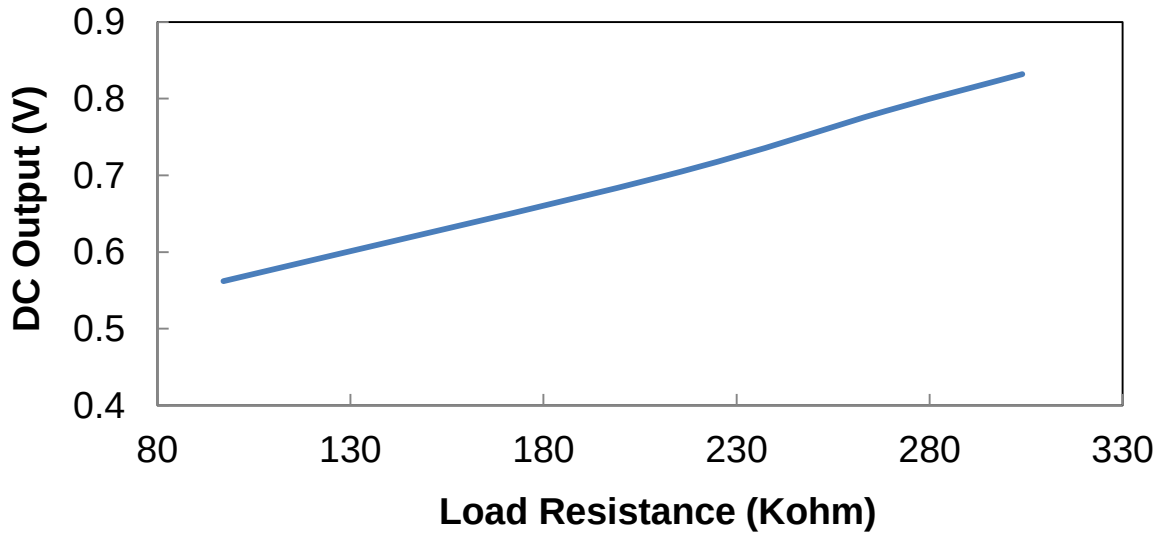


Figure 6.3 DC output voltage with different load resistance, RF input at 9.2 GHz and power of -10 dBm

Figure 6.3 shows the dependence of DC output voltage on load impedance. The extracted

equivalent internal source resistance at P_{in} = -10 dBm is 85.8 KΩ, which is close to the value extracted from simulation results (100 KΩ). Compared with Cadence Spectre simulation result, the measurement data shows lower optimum frequency, 9.0~9.6 GHz versus 10 GHz in simulation and lower DC output, which is largely attributed to the circuit parasitics.

Figure 6.4 shows the DC voltage generated by the power harvester circuit for different levels of the input signal power at 9.2 GHz. The circuit exhibits 3.1% power conversion efficiency for -8 dBm input power.

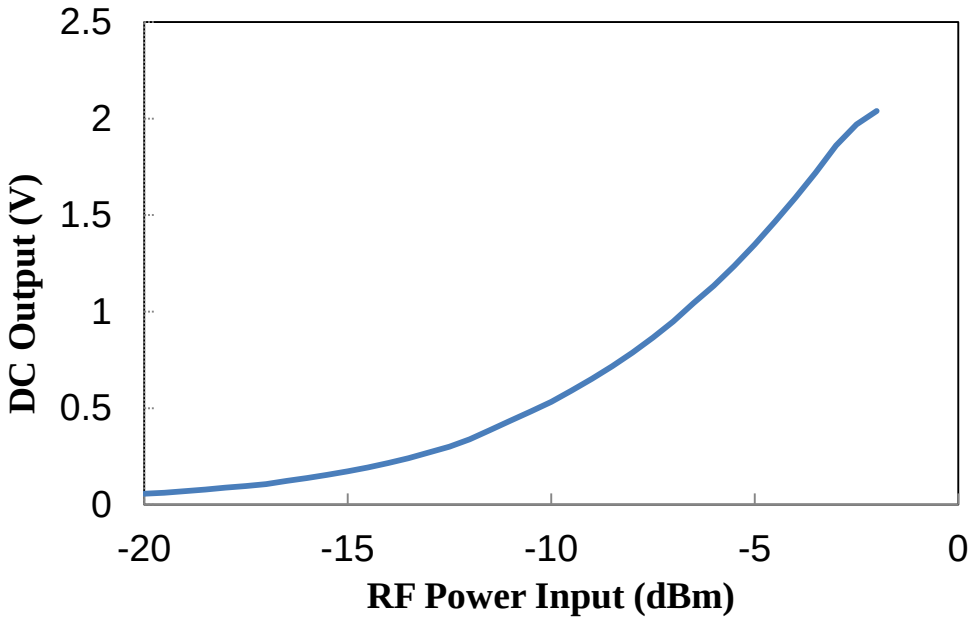


Figure 6.4 DC output voltage versus RF input power at 9.2 GHz with load impedance of 304 KΩ

6.2 X-band Antenna

6.2.1 Slot antenna

Figure 6.5 shows the fully integrated RF-DC rectifier with miniaturized slot antenna. We

used the rectifier with series inductive matching since it produced the highest DC output voltage to integrate with the slot antenna [31, 32]. To characterize the antenna itself, separate antenna with GSG pad was also included in the final layout. The measurement setups for both structures are shown in Figure 6.5.

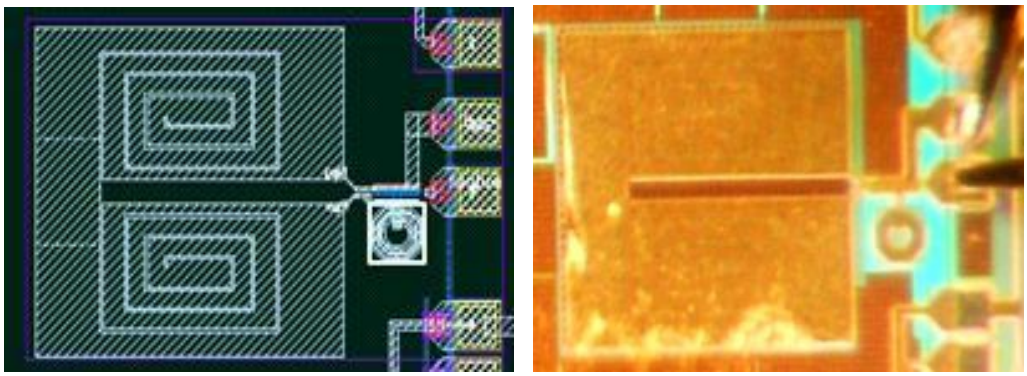


Figure 6.5 Layout and microphotograph of the RF-DC Rectifier with slot antenna

The RFOUT of the Agilent 8341A vector signal generator was connected to the WR-90 horn antenna which has the frequency band of 8.2 GHz to 12.4 GHz and nominal gain of 15 dB. The electromagnetic waves from the horn antenna were received by the slot antenna.

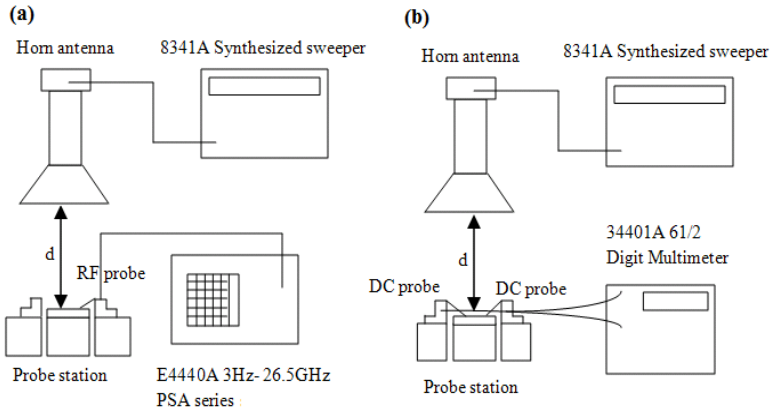


Figure 6.6 (a) on-chip probing setup used to measure slot antenna; (b) on-chip measurement setup used to measure the rectified voltage of the RF-DC rectifier with slot antenna

To measure the received power spectrum, the antenna was probed directly by Cascade Microtech GSG probe connected to the E4440A (3 Hz – 26.5 GHz) series spectrum analyzer. Fig. 9 shows the received power versus antenna range for 10 dBm source power at 10 GHz.

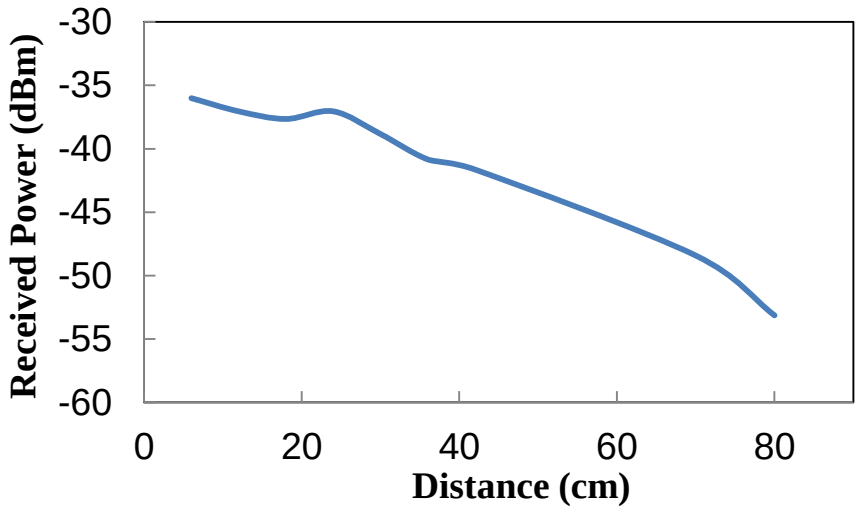


Figure 6.7 Power received by slot antenna versus the distance between antennas with source power of 10 dBm

The power arrived at the slot antenna, P_r, can be calculated using the Friss free-space equation. The Friss free-space equation in dBm is as follows:

$$P_r = P_t + G_t + G_r - 20log_{10}\left(\frac{4\pi d}{\lambda}\right) \quad (6.1)$$

where, P_t is the power transmitted by the transmitting antenna, G_t is the gain of the transmitting antenna, G_r is the gain of the receiving antenna, λ is the wavelength, and d is the distance between the receiving and transmitting antenna.

Figure 6.8 shows the slot antenna gain versus the distance calculated from the Friss equation (6.1). The best gain of the slot antenna was achieved when the distance between the two antennas was from 24 cm to 60 cm.

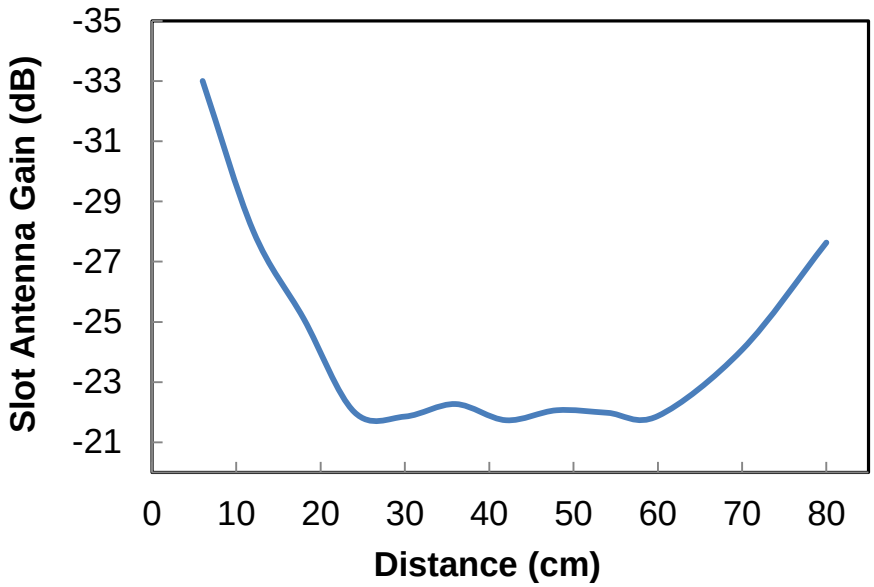


Figure 6.8 Receiver antenna gain versus the distance between antennas with source power of 10 dBm

Our model uses the following parameters: For a one data set

d = 0.24 m

λ = 0.03 m (f = 10 GHz)

P_t = 10 dBm (8341 synthesized sweeper power)

G_t = 15 dB (WR-90 horn antenna 8.2 – 12.4 GHz power)

P_r = -37.05 dBm (Received power of EM4440A spectrum analyzer)

From (5) => G_r = -22.0 dB

With all the data points the receiver antenna gain (G_r) can be obtained as -22 dB.

The fully integrated energy harvester was implemented as a 6 stage RF-DC rectifier connected to the slot antenna. Figure 6.10 shows the generated DC output of the X-band energy harvester with different levels of source power. When the source power increased from 0 dBm to 10 dBm the DC output increase gradually from 0 mV to 40 mV. When the source power was increased beyond 10 dBm there was a rapid increase of the DC output from 40 mV to 100 mV.

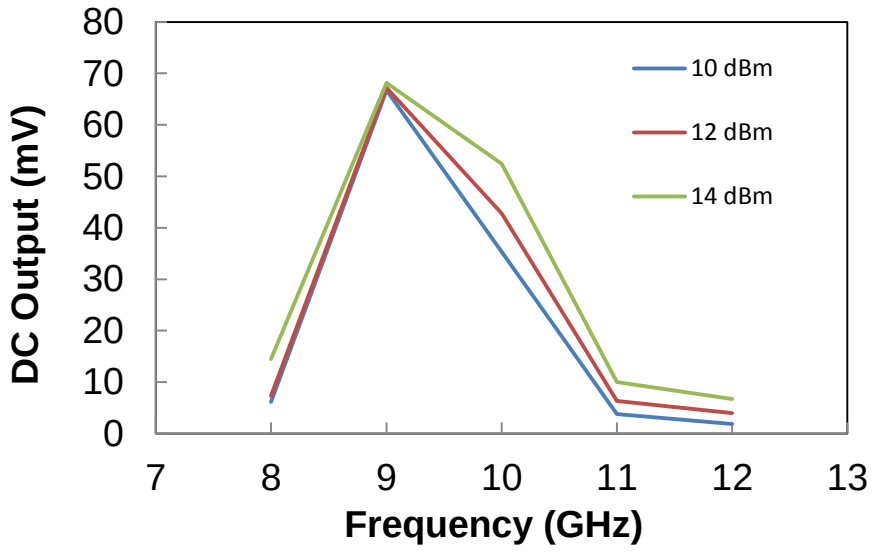


Figure 6.9 DC output voltage versus input signal power at 10 GHz at the antenna range of 6cm

We have implemented a novel fully integrated X-band energy harvester in IBM 0.18-µm RF CMOS technology with on-chip antenna which is smaller than the previously reported antennas. The novel on-chip miniaturized slot antenna occupies less space compared to the traditional off-chip antennas. The proposed antenna covers an area of 0.55mm^2. The smaller size and the cost of the RFID tag are critical for widespread adoption of the technology. The cost of the RFID tag can be lowered by implementing an on-chip antenna.

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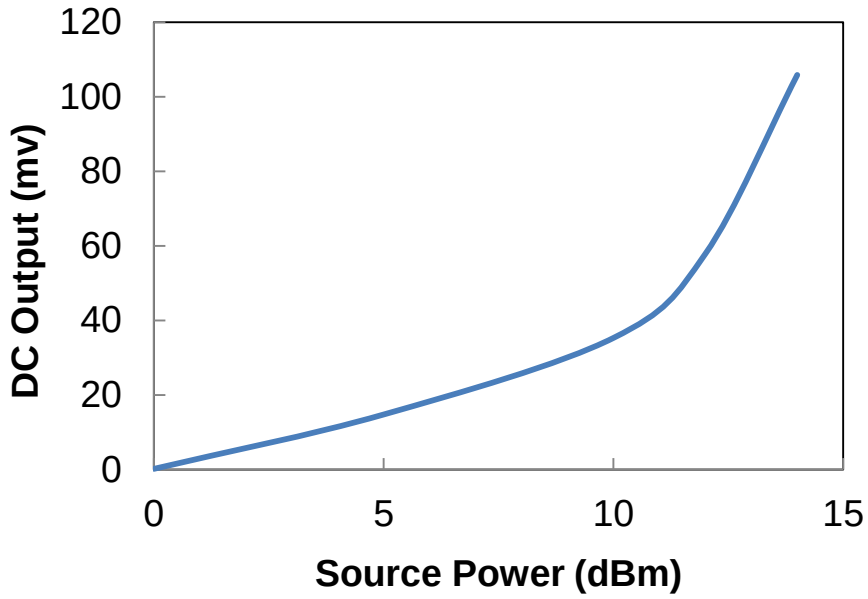
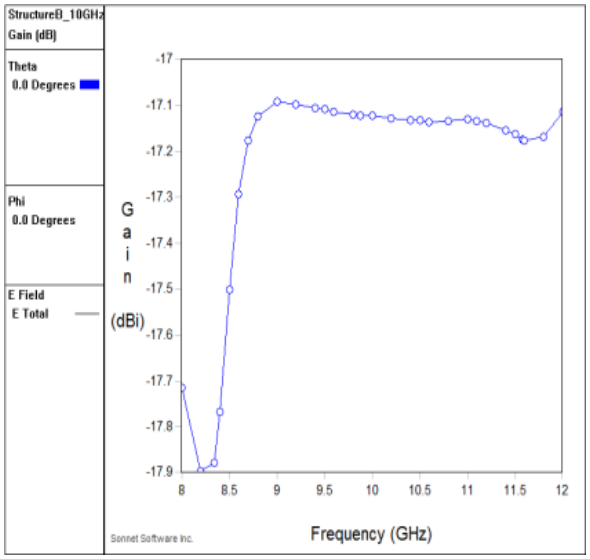


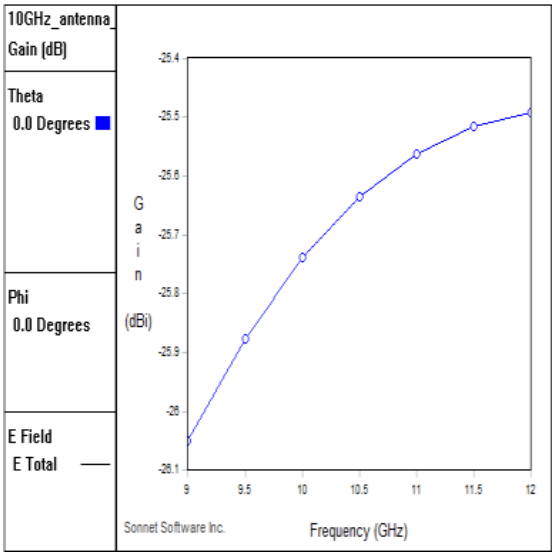
Figure 6.10 DC output voltage versus input signal power at 10 GHz at the antenna range of 6cm

6.2.2 Asymmetric dipole antenna with differential port

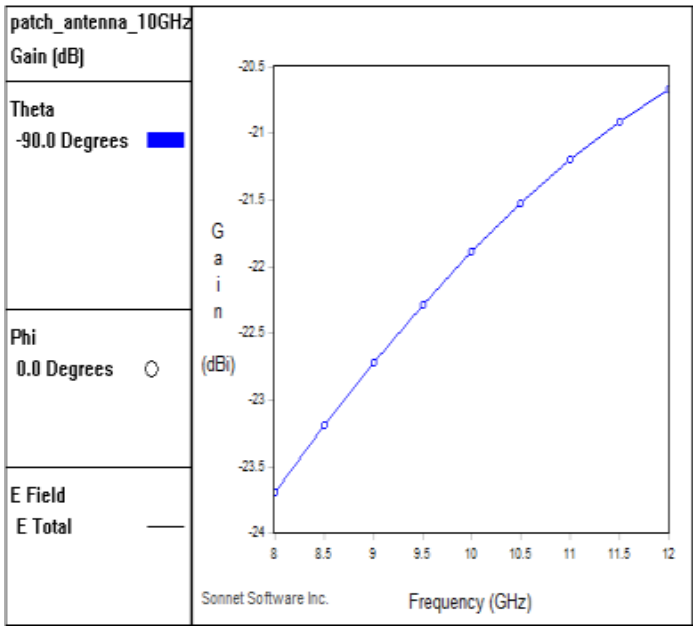
The simulated antenna gains vs. frequency are shown in Figure 6.11(a) The proposed antenna with differential port (Figure 6.11) has a gain of -17.1dBi. In contrast, symmetric dipole antenna with balun in the same dielectric environment shows a modest gain of -25.7dBi and the Patch antenna has a gain of -21.5dBi. The gain vs. theta of the proposed antenna was compared with the symmetric dipole antenna with balun and the patch antenna (Figure 6.12). The simulated antenna pattern plots of gain are shown in Figure 6.12.



(a)

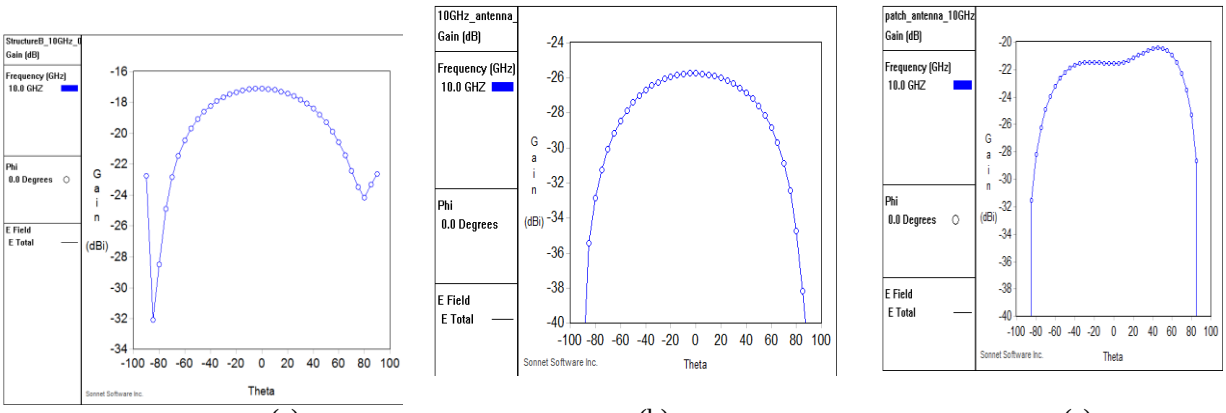


(b)



(c)

Figure 6.11 Directive gain at (φ=θ=0) vs. frequency of (a) asymmetric dipole antenna differential port, (b) Symmetric dipole antenna, and (c) patch antenna



(a) (b) (c)

Figure 6.12 Antenna pattern plots of gain (φ=θ=0) vs. theta of (a) asymmetric dipole antenna differential port, (b) Symmetric dipole antenna, and (c) patch antenna

Table 6.1 Layout dimension and gain

Antenna	**Gain**	***fr***	**Maximum Linear Dimenasion**
Asymmetric Dipole Antenna	-17.1	10.2	504
Symmetric dipole antenna with balun	-25.7	10.0	660
Patch Antenna	-21.5	10.0	851

Table 6.1 shows the comparison of the proposed antenna with the symmetric dipole antenna with balun and patch antenna. The asymmetric dipole antenna with differential port has the highest gain of -17.12dBi with similar maximum linear dimension to the other two structures. During the antenna design process, we noticed the asymmetric dipole antenna shows much higher resonant frequency (>20GHz) than above antennas with similar sizes. To compare with other state-of-the-art small antennas, the next step will be fabricating and

measuring the proposed antenna structure in IBM 0.18 CMOS technology.

Test plan for chip 2

RFID chip is shown in Figure 6.13. Wirebonded rfid chip of the PCB board is given in Figure 6.14. RFID chip contain entire RFID tag and the individual test blocks.

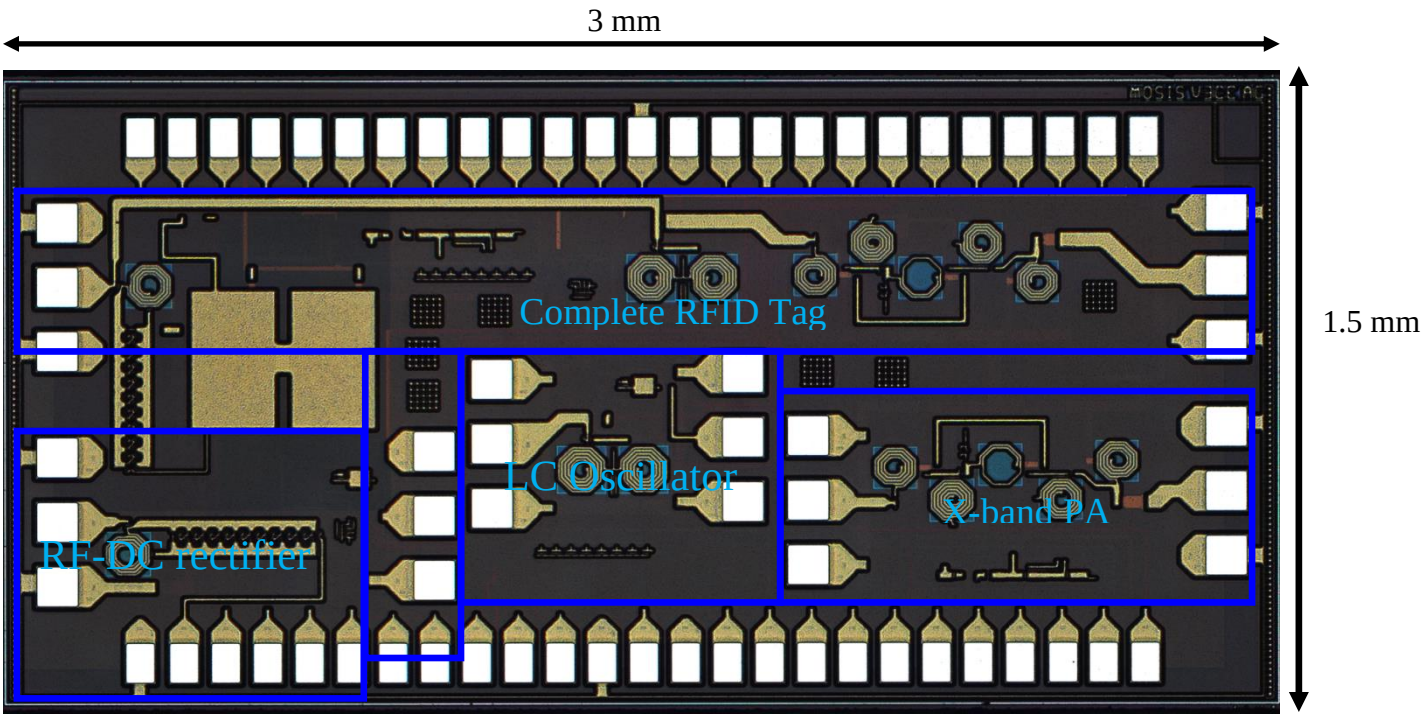


Figure 6.13 Microphotograph of the RFID tag (3 mm X 1.5 mm) with test blocks

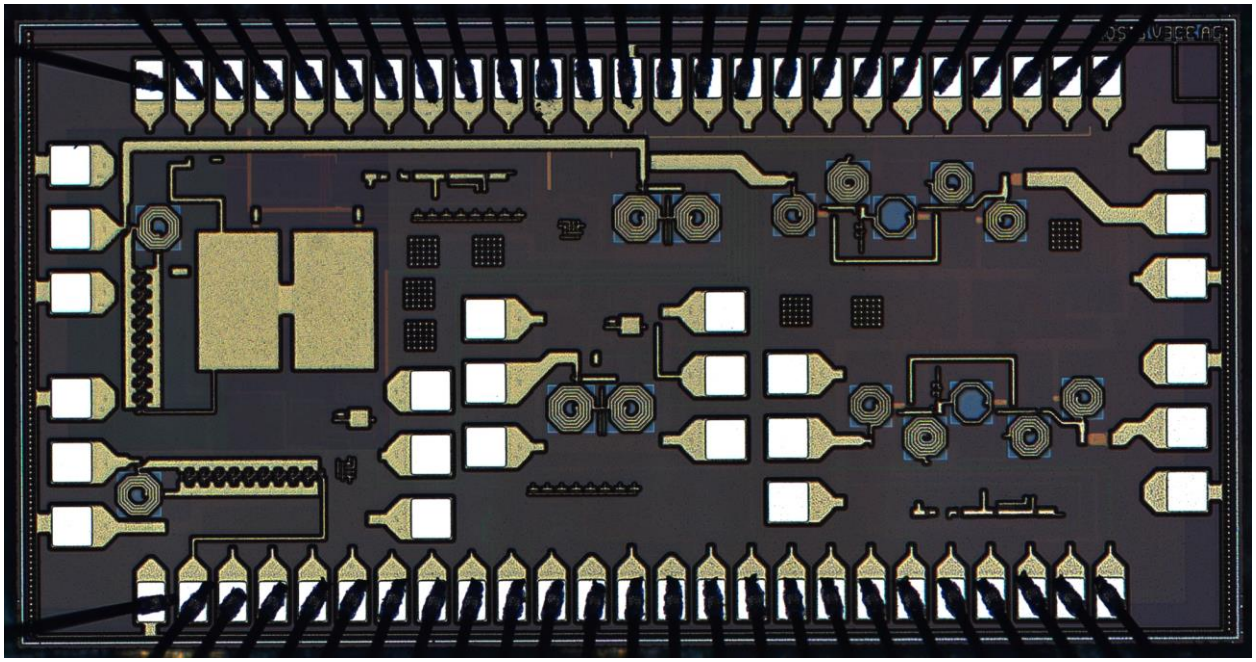


Figure 6.14 Microphotograph of the wirebonded RFID tag with test blocks

1. **Complete RFID tag**

   - Vout_DC : Ouput of the RF-DC rectifier. The output of the rectifier is connected to extl-cap used as the load of the rectifier. Output of the rectifier will be displayed in the oscilloscope through “Vout_DC_sma”
   - Vout_DC_test : Vout_DC_test signal for the RF-DC rectifier. If the DC output of the rectifier is not enough “Vout_DC_test” will be given externally through jumper J2. If the rectified output and the test output voltage is the same it will be shorted
   - enable : The output of the voltage sensor will be displayed from this signal. This is connected to oscilloscope through “enable_sma”

- vcontrol_lc : Control voltage for the injection lock LC oscillator will be provided from the jumper J1 (line 2 of jumper J1)
- vcontrol_rc : Control voltage for the RC oscillator will be provided from the jumper J1 (line 1 of jumper J1)
- rfid_tag_add5, rfid_tag_add4, rfid_tag_add3, rfid_tag_add2, rfid_tag_add1: The combination of the 5 bit addresses will be provided from this dip switch
- Q1: The output of the 5 bit shift register will be connected to a oscilloscope through "Q1_out" sma. This will display the final output of the 5 bit shift register in the entire RFID tag. If the Q1 output is not correct it will provided from a function generator connected through "Q1_out" sma.

2. X-band PA

- Vbias pa_2_PA :" vbias_pa_2_PA" and "vbias_pa_2_cons_gm" from constant g_m circuit are connected to" J_PA" jumper. If both voltages are the same it will shorted through the jumper
- Vbias pa_1_PA :" vbias_pa_1_PA" and "vbias_pa_1_cons_gm" from constant g_m circuit are connected to "Jf" jumper. If both voltages are the same it will shorted through the jumper
- Q1_PA : Is the output from the 4 bit shift register. This signal will be provided externally from the function generator connected through sma "Q1_PA"
- vdd_pa : The power to power amplifier will be provided through the Header2 (Jd)

3. RF-DC Rectifier

- rec_dc_out : Output of the rectifier block
- rec_dc_out_sma: Ouput of the rectifier is connec ted through "rec_dc_out_sma" to display the output of the rectifier from E440A oscilloscope. The waveform will be used to see the ripples of the RF-DC rectifier output.
- rec_out_extcap : This is the external capacitor used as the load of the rectifier. This will be used to see the capacitor loading of the rectifier circuit.
- R12: This resistor will be used to calculate the output power of the rectifier circuit. This will be also used to see the resistive loading of the rectifier circuit.

4. 4 bit shift register circuit

- Vout_: This will be used to provide the clock signal to the shift register.
- Q1_SR: The final output of the shift register .
- Tagid_SR_5: This id will provided from the 4th position of the dip switch.
- Tagid_SR_4: This id will provided from the 3rd position of the dip switch.
- Tagid_SR_3: This id will provided from the 2nd position of the dip switch.
- Tagid_SR_2: This id will provided from the 1st position of the dip switch.
- Shift_load_SR : This will be used to load or shift the bits of the shift register.
- vdd_shift_reg: The power of the 4 bit shift register through the Header2(Jl)

5. **Schmitt trigger circuit**

- vout_sch_trig : “vout_sch_trig” is connected through “vout_sch_tr_sma” to see the output of the Schmitt trigger circuit.
- vin_sch_trig: “ vin_sch_trig” is connected through “vin_sch_tr_sma” to provide the input from function generator to the Schmitt trigger circuit.
- vdd_sch_trig: The power of the 4 bit shift register through the Header2(Jn)

6. **Voltage sensor**

- **vout_volt_sensor** : Output of the voltage sensor is connected to “vout_volt_sensor” to see the output voltage.
- **vdd_volt_sensor**: The vdd waveform of the voltage sensor will be given from the function generator connected through the **sma “vdd_sensor_sma”**.

7. **Voltage regulator**

- vbias_reg : Bias voltage for the voltage regulator will be given externally from the jumper” Ji”.
- vout_reg: Voltage regulator output will be displayed through a oscilloscope connected through “vout_reg_sma”.
- vdd_volt_reg: The vdd waveform for the voltage regulator will be given from a function generator connected through the sma “vdd_volt_reg”

8. RC oscillator

- vcontrol_rc_osc : The control voltage of the RC oscillator will be provided through the jumper J5 (line 2 of Jumper J5).
- vbias_rc_osc: The bias voltage of the RC oscillator will be provided through jumper J6. If the "v bias_rc_cons_gm" voltage of the constant gm bias circuit and "vbias_rc_osc" of the RC oscillator are the same it will shorted in jumper J6.
- vdd_rc_osc: The power of the rc oscillator will be provided through jumper J4.

9. LC oscillator

- vcontrol_lc_osc : The control voltage of the LC oscillator will be provided through the jumper J5 (line 1 of Jumper J5).
- vbias_lc_osc: The bias voltage of the LC oscillator will be provided through jumper Ja. If the "vbias_lc_cons_gm" voltage of the constant gm bias circuit and "vbias_lc_osc" of the LC oscillator are the same it will shorted in jumper Ja.
- vdd_lc_osc: The power of the lc oscillator will be provided through jumper J7.

6.3 X-band PA Results

X- band PA result setup is shown in Figure 6.14.

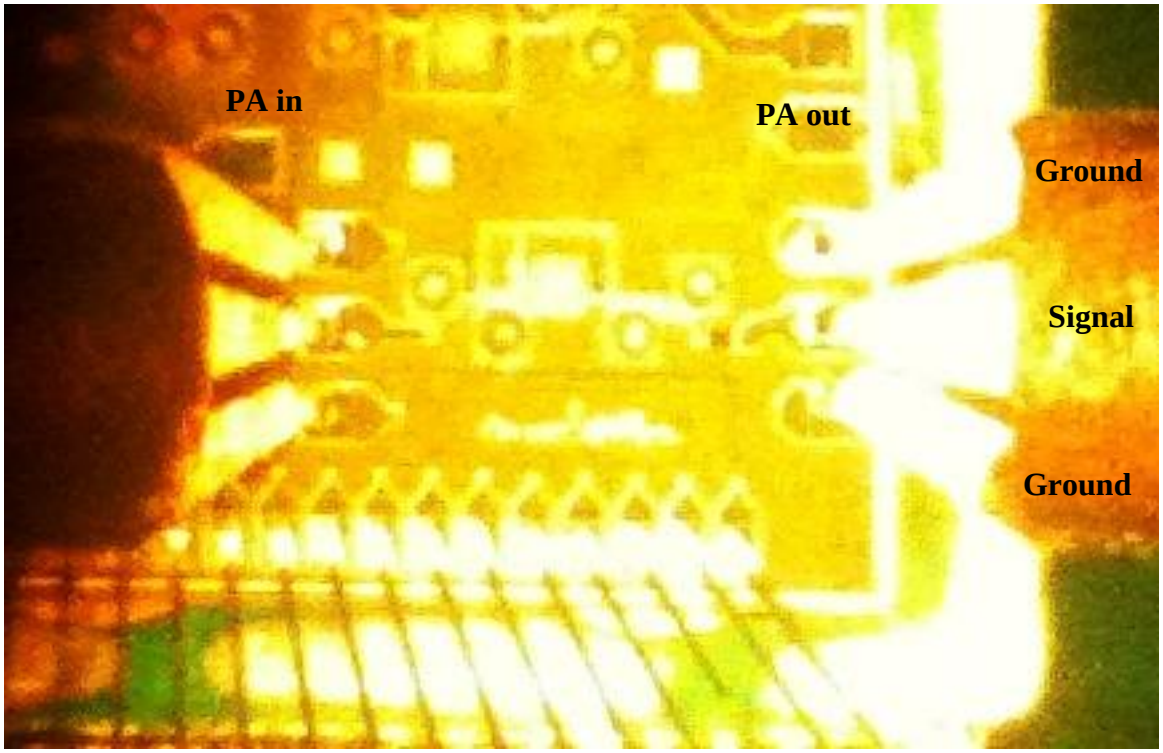


Figure 6.14 Microphotograph of the X-band PA test structure probe setup

PCB board was manufactured in Saturn PCB and wirebonding was carried out by Amtech microelectronics. The RF signal was generated by Agilent 8341A vector signal generator. RF signal was connected to PA in Figure 6.14. The output of the PA, PA out was connected to Agilent E4440 A spectrum analyzer. X- band PA test structure pcb board setup is shown in Figure 6.15. When the modulation of the PA is on the magnitude of the output signal is shown in Figure 6.16. It has a output power magnitude of -29.21dBm at 11.58GHz frequency. This magnitude was shown in Spectrum analyzer after 20dBm attenuator and a 6.41dBm cable loss.

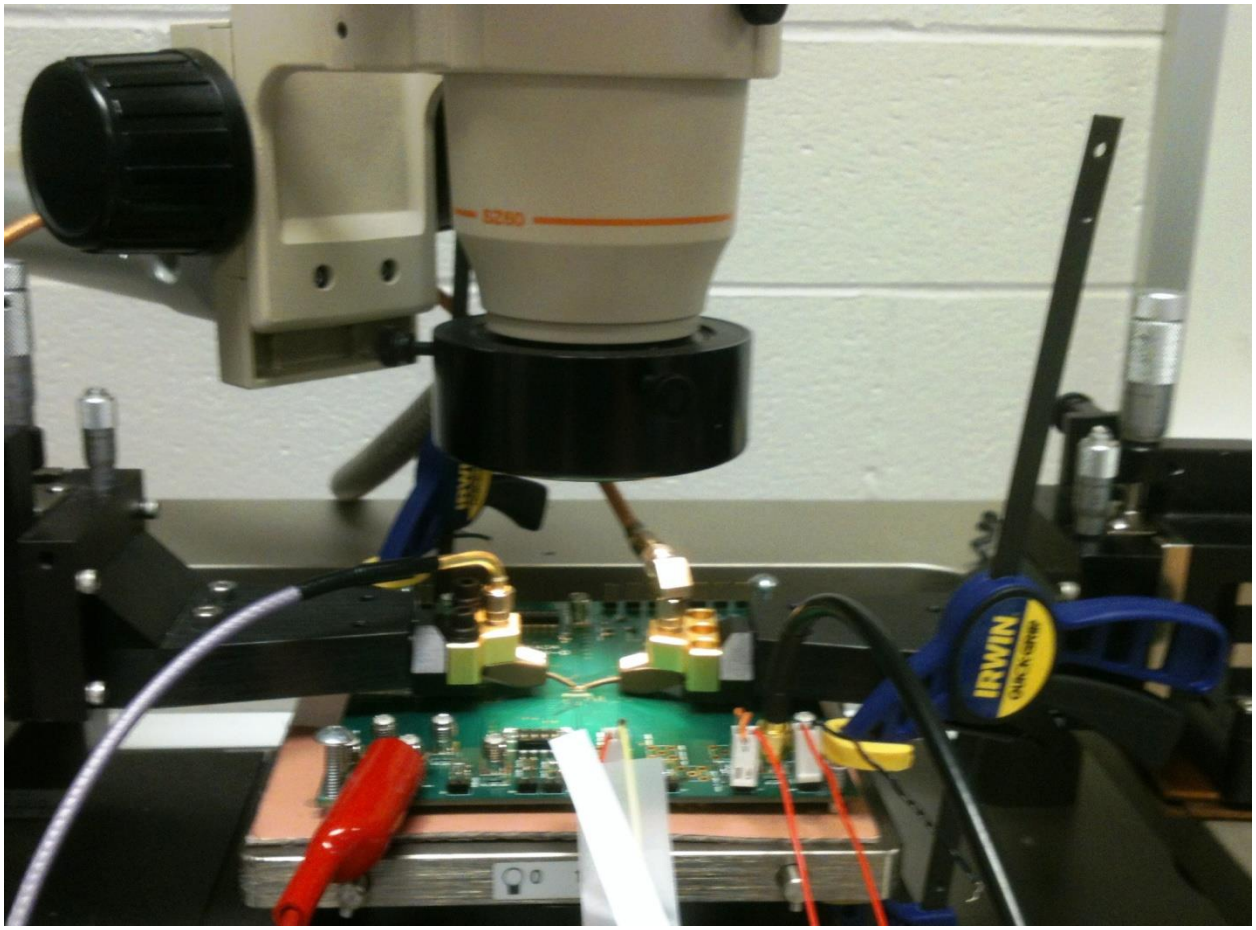


Figure 6.15 X-band PA board setup

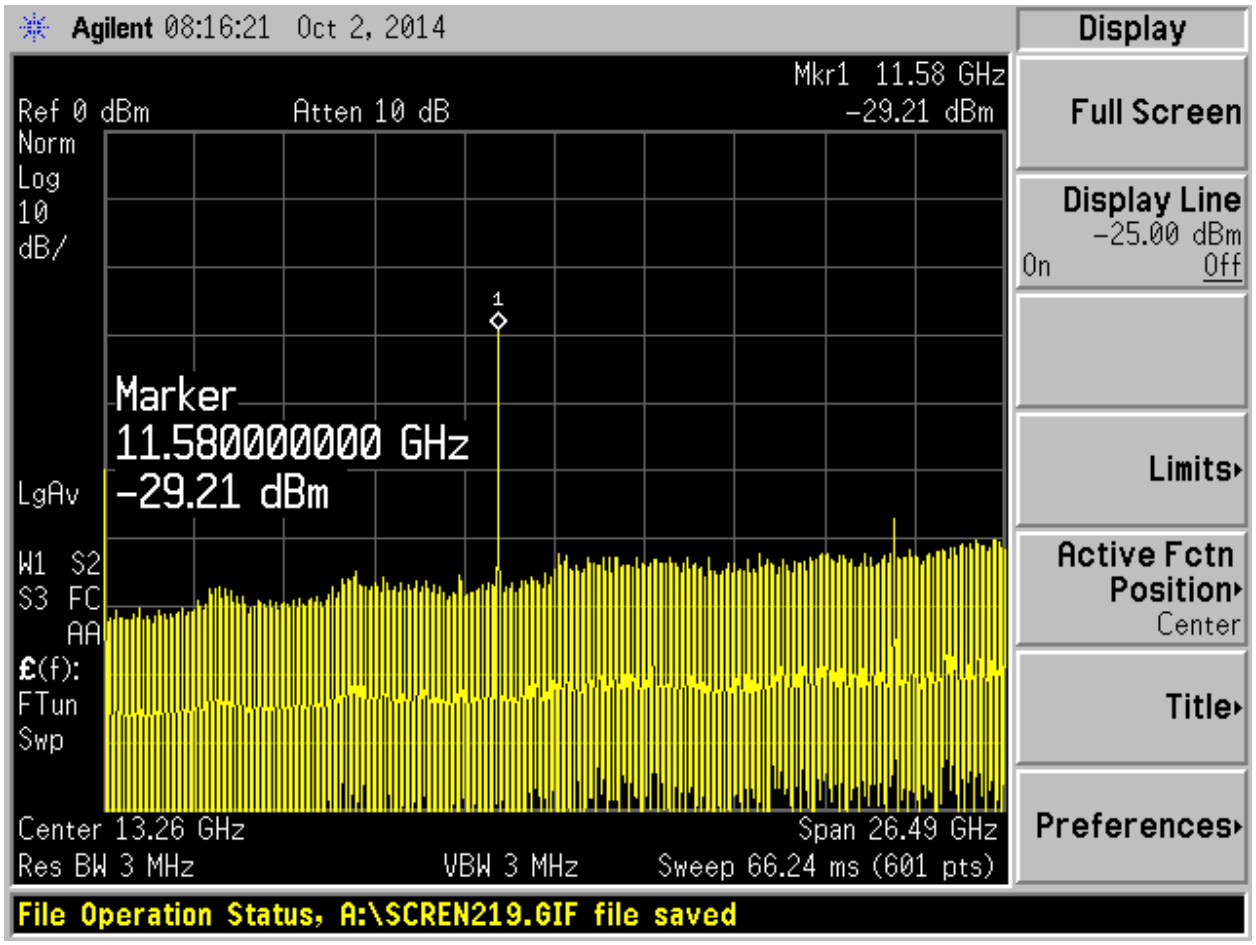


Figure 6.16 X-band PA output power spectrum when the modulation is on

When the modulation of the PA is off the magnitude of the output signal is shown in Figure 6.17. It has a output power magnitude of -60.46dBm at 11.58GHz frequency. This magnitude was shown in Spectrum analyzer after 20dBm attenuator and a 6.41dBm cable loss. The PA was designed to transmit the bits of the RFID tag. The bits were transmitted using On-Off_Keying (OOK).

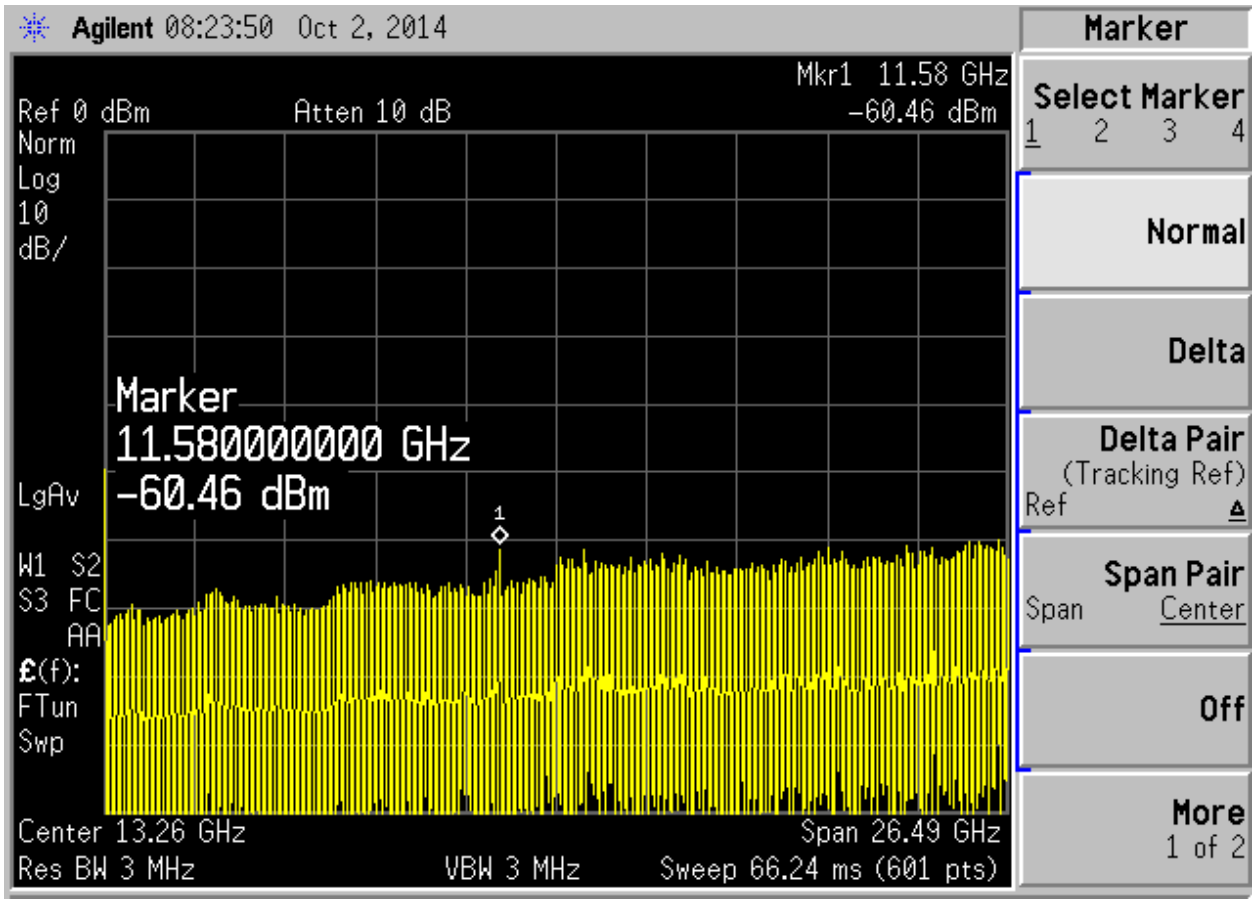


Figure 6.17 X-band PA output power spectrum when the modulation is off

X band PA test condition for output power vs frequency

- vdd = 1.83 V
- current = 9 mA
- vbias_pa_1 = 0.84 V
- vbias_pa_2 = 0.82 V
- input power = -1 dBm
- Attenuation = 20 dBm
- Cable loss = 6.41 dBm

X-band PA has a maximum output power of 5.19dBm at 9.3GHz (Figure 6.18). This frequency can be increased to 11GHz with a post layout simulation in cadence tool.

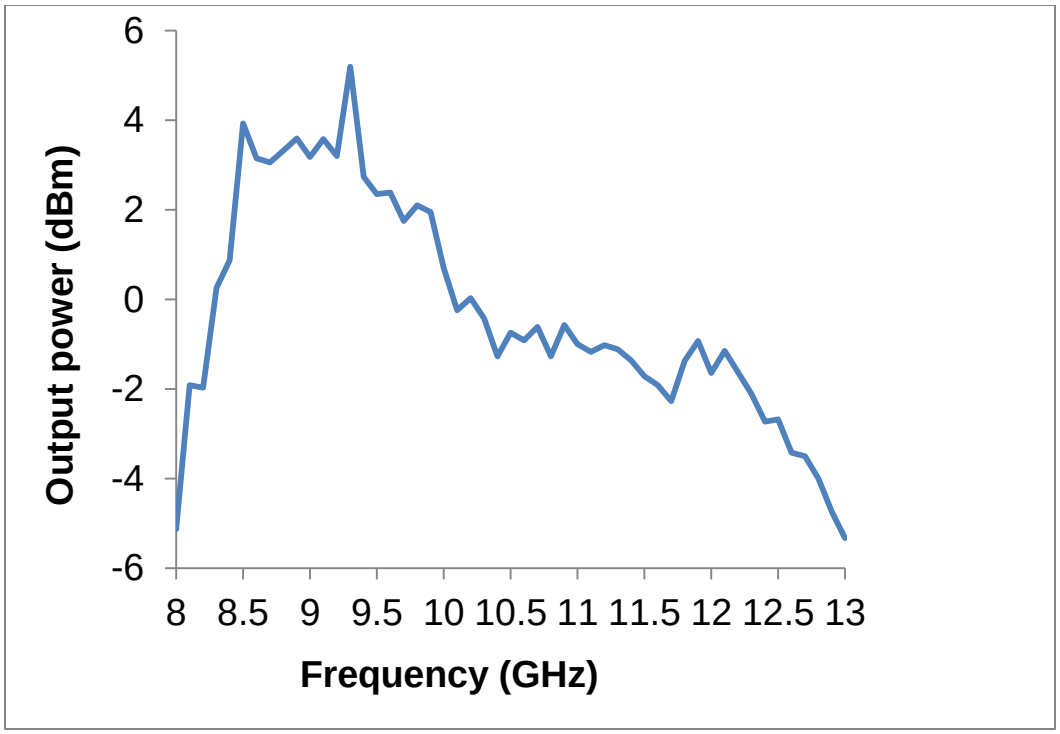


Figure 6.18 X-band PA output power vs. frequency

X band PA test condition for output power vs input power

vdd = 1.83 V

current = 7 mA

vbias_pa_1 = 0.84 V

vbias_pa_2 = 0.82 V

input power = -1 dBm

Attenuation = 20 dBm

Cable loss = 6.41 dBm

The input power vs. output power of the fabricated X-band PA is shown in Fig. 6.19. The output power saturates after 1 dBm

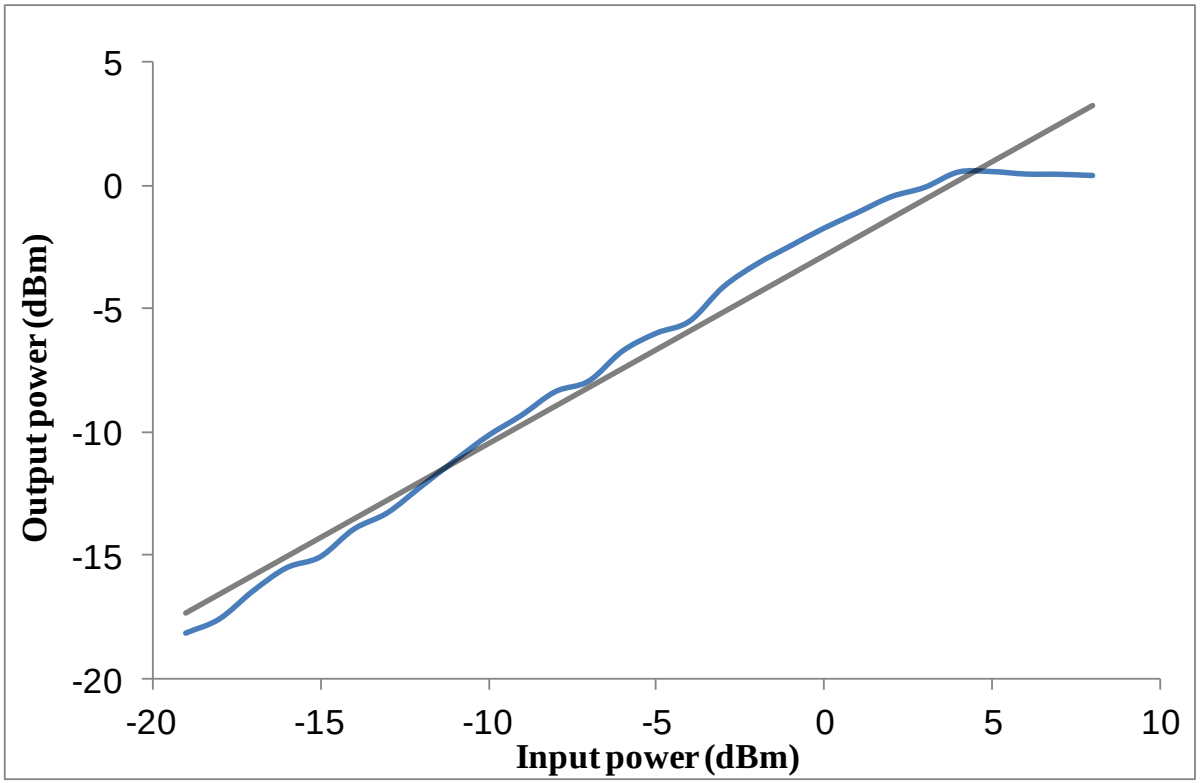


Figure 6.19 X-band PA output power vs. input power fabricated results

The input power vs. output power simulated X-band PA is shown in Figure 6.20. The output power saturates after 5 dBm

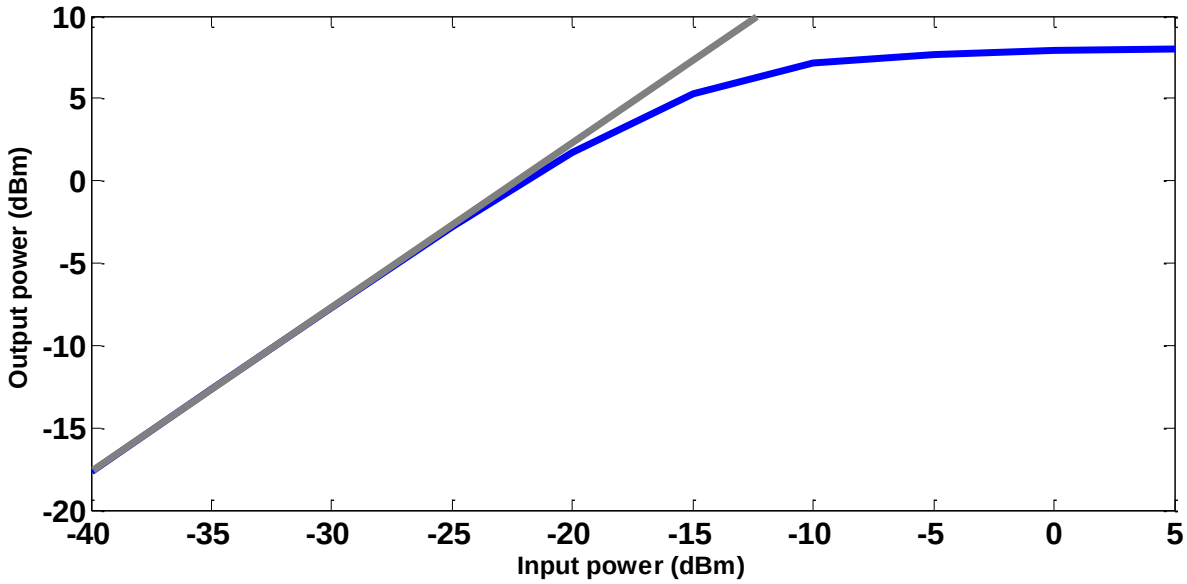


Figure 6.20 X-band PA output power vs. input power measured results

X band PA test condition for output power vs input power

vdd = 1.83 V

current = 7 mA

Frequency = 9.3 GHz

vbias_pa_1 = 0.69 V

input power = -1 dBm

Attenuation = 20 dBm

Cable loss = 6.41 dBm

The output power vs. bias voltage1 of X-band PA is shown in Figure 6.21. The output power of the PA reaches the maximum value when the bias voltage is 0.82 V.

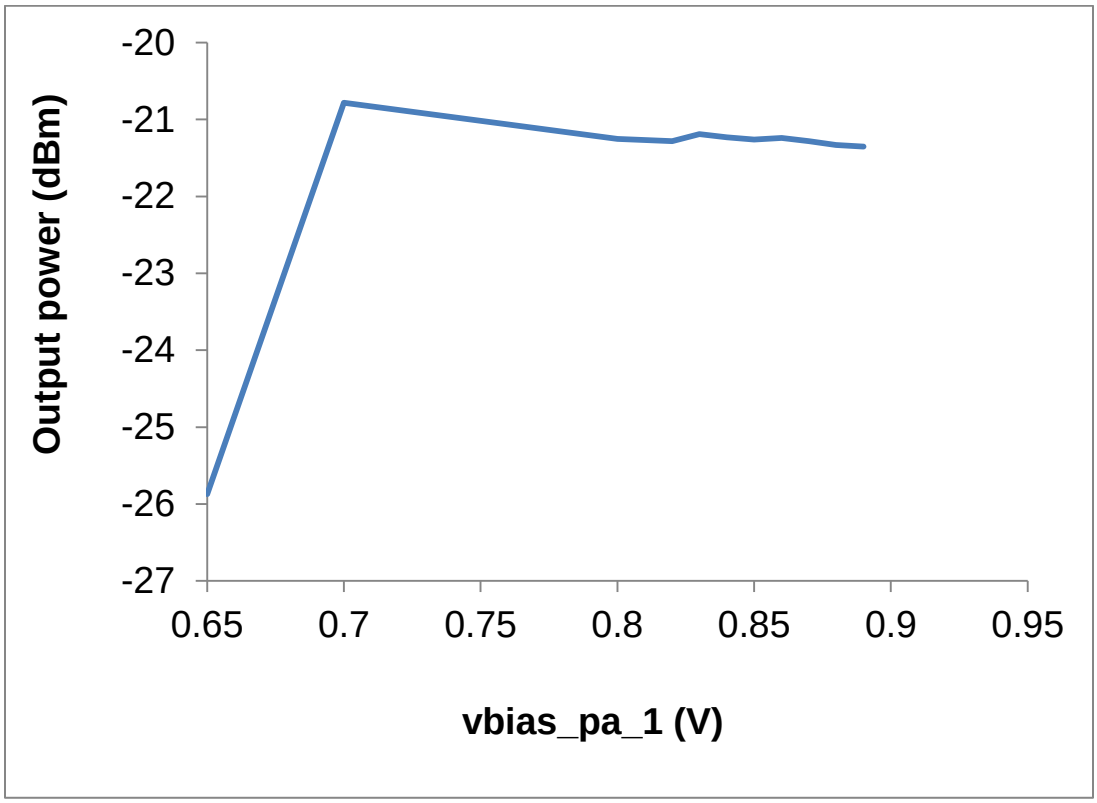


Figure 6.21 X-band PA output power vs. power amplifier bias voltage1

vdd = 1.83 V

current = 7 mA

Frequency = 9.3 GHz

vbias_pa_1 = 0.82 V

input power = -1 dBm

Attenuation = 20 dBm

Cable loss = 6.41 dBm

The output power vs. bias voltage2 of X-band PA is shown in Figure 6.22. The output power of the PA reaches the maximum value when the bias voltage is 0.73 V.

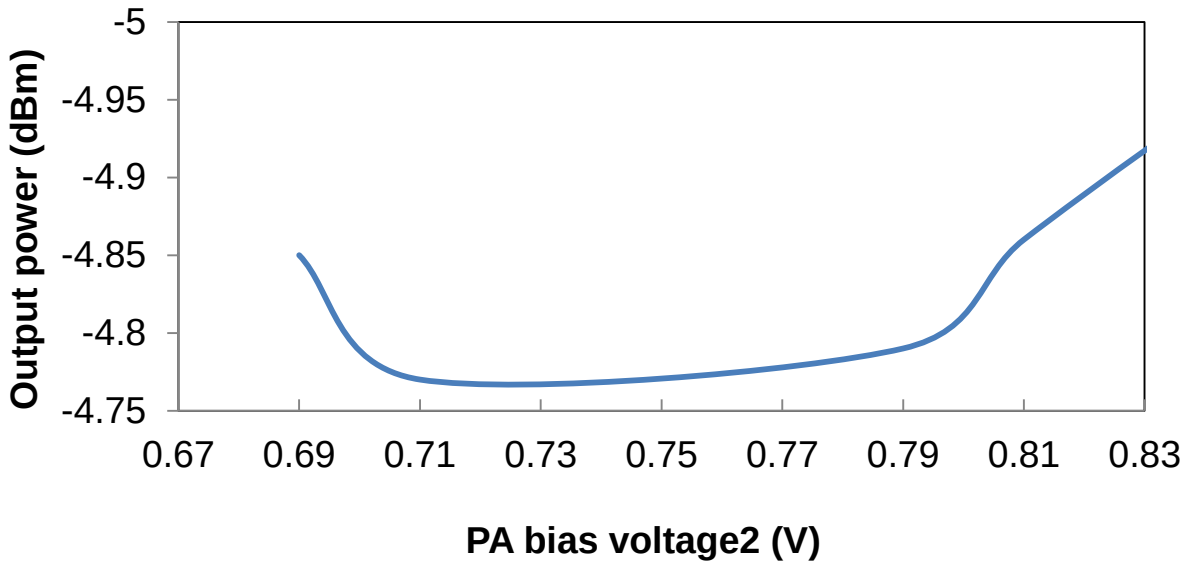


Figure 6.22 X-band PA output power vs. power amplifier bias voltage2

CHAPTER 7

Conclusions And Suggestions For Future Work

7.1 RF –DC Rectifier

One of the most promising components of the proposed architecture is the RF-DC rectifier. It is fully CMOS compatible and can be fabricated in foundry offering low threshold devices. After obtaining the simulation results, we used a 10 stage rectifier which generates 1.83 V with the minimum RF power needed to operate the rectifier.

7.2 X-band Power Amplifier

One of the most power hungry components of the proposed architecture is the Power amplifier circuit. Currently the power amplifier gives the maximum output power of 0.23dBm at 9.1GHz. Cadence spectre post layout simulation of the power amplifier will be needed to have a maximum output power at 11.6GHz.

7.3 LC Oscillator

The proposed architecture uses two separate inductors in the resonant tank of the LC oscillator. These inductors can be replaced by a transformer which achieves high quality factor with a smaller area.

7.4 General Comments

We implemented a novel fully integrated X-band energy harvester in IBM 0.18-µm RF CMOS technology with on-chip antenna which is smaller than the previously reported antennas. The novel on-chip miniaturized slot antenna occupies less space compared to the traditional off-chip antennas.

The lower price and miniaturization of the antenna allow new RFID technology applications such as insects tracking. These tiny tags can be attached to moving insects such as

honey bees, butterflies, and ants to track their movements and habitats. The other key design issues addressed in this research include the roles of coupling and load capacitors in a multistage rectifier, different matching networks for voltage boosting and efficient power transfer from a source.

Our simulation and measurement results show that the single series inductor provides the best matching for the multi-stage rectifier. The matched rectifier generated 1.23V DC output voltage with 304 KΩ load at 9.2 GHz for -8 dBm direct X-band input through the GSG probe. Our results show the feasibility of a fully integrated passive RFID transponder with on-chip antenna in X-band frequency.

The entire RFID tag circuit was designed to operate in low power consumption. Voltage sensor circuit which generates the enable signal was designed to operate in very low current. In the active mode RF-DC rectifier current is about 3μA. All the test blocks of the RFID tag were tested.

The smaller size and the cost of the RFID tag are critical for widespread adoption of the technology. The cost of the RFID tag can be lowered by implementing an on-chip antenna. It was possible to develop, fabricate, and implement a fully integrated RFID tag in a size which is smaller (3 mm X 1.5 mm) than the existing tags. With further modifications, this could be used as a commercial low cost RFID tag.

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