2010

Nano-Scaled Fet Device For Cmos Technology

Prabhat Ranjan Pathak
North Carolina Agricultural and Technical State University

NANO-SCALED FET DEVICE FOR CMOS TECHNOLOGY

by

Prabhat Ranjan Pathak

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

Department: Electrical Engineering
Major: Electrical Engineering
Major Professor: Dr. Alvernon Walker

North Carolina A&T State University
Greensboro, North Carolina
2010

ABSTRACT

Pathak, Prabhat Ranjan. NANO-SCALED FET DEVICE FOR CMOS TECHNOLOGY. **(Major Advisor: Alvernon Walker)**, North Carolina Agricultural and Technical State University.

In this work the 3-D structure of the Accumulation mode (ACM) and Enhance mode (ECM) FinFET was developed by the Taurus-Device Editor. The design of both ACM and ECM FinFET was optimized for high-performance IC applications to meet ITRS specification for I_{off} current, for 9nm gate length. The design of ACM and ECM FinFET is optimized, analyzed and compared against each other with respect to Darin Induced Barrier Lower (DIBL), Sub-threshold Swing(SS), operation and performance characteristics with varying electrical and physical parameters Silicon thickness (T_{si}), Source/Drain doping gradient (σ_{sd}), electrical channel length (L_{eff}), lacer spacer width (L_{sp}) and Source/Drain Contact Resistance (r_{sd}). Finally, both designs were optimized for 9nm gate length for on current (I_{on}) to meet ITRS specifications for I_{off}. The simulation solves and includes Poisson, drift-diffusion transport equation and 3D-Schrodinger equation self-consistently.

School of Graduate Studies
North Carolina Agricultural and Technical State University

This is to certify that the Doctoral Dissertation of

Prabhat Ranjan Pathak

has met the dissertation requirements of
North Carolina Agricultural and Technical State University

Greensboro, North Carolina
2010

Major Professor Dr. Alvernon Walker	Research Professor Professor Tsu-Jae King Liu
Committee Member Dr. Clinton B. Lee	Committee Member Dr. Ward J. Collis
Committee Member Dr. Corey A. Graves	Department Chairperson Dr. John Kelly

Interim Associate Vice Chancellor
of Research and Graduate Dean
Dr. Alan Letton

DEDICATION

To My Family

BIOGRAPHICAL SKETCH

Prabhat Ranjan Pathak was born in Hazaribagh, India on January 2, 1974. He received his B.E (Bachelor of Engineering) degree in Electronics Engineering in the year 1996 at the Nagpur University, India. He received the Master of Science degree from the Department of Electrical Engineering at the University of North Carolina A & T State University, Greensboro, North Carolina in 2003. He is currently a Ph.D. candidate in the Department of Electrical and Computer Engineering at the University of North Carolina A & T State University, Greensboro.

ACKNOWLEDGEMENTS

First of all, I thank my parents and my family for their support and encouragement. I appreciate very much the support of Aunt and Uncle Narmada and Manu for all the support extended to me throughout all the years during my Ph.D.

It is a great time to express my many thanks to Professor Tsu-Jae king Liu for providing me all the resources and extraordinary guidance in my Ph.D. research. It is a great honor for me to have her as research advisor/co-chair. Also, I am very grateful to all the members of Device Group, including industrial research fellows from Hitachi, Toshiba and Samsung at University of California Berkeley for providing me important insight and information in my research and helping me to finish my research on time.

I am very thankful to the Department of Electrical Engineering and School of Graduate Studies at North Carolina A & T State University for providing me the opportunity to finish my Ph.D. and M.S Degree. I also would like to thank my major advisor Dr. Alvernon Walker and Committee member Dr. W. J. Collies, Dr. Clinton B. Lee and Dr. Corey Graves for their valuable time serving as my research committee, and for their valuable classroom instruction. I would also like to thank Dr. Numan Dogan for his instruction, his suggestions, and for being my advisor for my M. S. Degree.

I would also like to thank my friend and fellow PhD student Serap Karagol for her help in the scientific workplace and with mat lab code in plotting my research results. Lastly, I would like to thank Cecilia Wright, Debora DeNaro and J.P. Chauhan for proofing my dissertation and proposals, and for helping with editing and formatting.

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES **PAGE**

LIST OF TABLES

TABLES **PAGE**

CHAPTER 1
INTRODUCTION

1.1 Motivation

Over the last three decades, the electronic industry has shown both monetary and business growth that has exponentially outpaced comparative industries such as automotive and steel with its value reaching more than one trillion dollars in the world economy every year. This multi-trillion dollar electronic industry is fundamentally based on the success of semiconductor devices. In that regard, the Complementary-Metal-Oxide-Semiconductor (CMOS) transistor technology has also strengthened over the last several decades and is potentially one of the most implemented technologies to make silicon based semiconductor devices using electronic chips.

Every year over the past fifty years, CMOS transistor technology has undergone a factor of two reductions in size resulting in increased performance, increased density of transistors, and reduced power dissipation of electronic chips. This trend was predicted by Gordon Moore in the late 1970's and has been proven true for the past several decades. For Moore's Law to continue below 65nm gate lengths, it was very important to suppress the High Short Channel Effect (HSCE) and Off State Leakage Current (OSLC), which are unimportant at higher gate lengths. Initially, emaciated gate dielectric materials, reduced junction depths, and advanced channel engineering which compressed the scaling trend of planner bulk silicon CMOS transistors just near gate lengths of 45nm. However, this

scaling trend cannot continue endlessly as reductions past the 45nm gate length suffer from severe physical and material limitations. As thickness of SiO_2 will be reaching the atomic scale layer in a few years.

A possible alternative solution to keep the scaling trend of CMOS technology on pace with Moore's Law would require a search for novel device structures and new channel materials with a higher dielectric constant 'k'. Two new promising nano-scale devices that are proposed for CMOS technology over the Planer bulk MOSFET are Ultra-Thin-Body MOSFET (UTB-MOSFET) and Double-Gate MOSFET (DG-MOSFET).

Both devices use an Ultra-Thin-Body (UTB) to suppress the HSCE, which has further advanced the scale down of CMOS technology to a sub-20nm technology node; however, UTB-MOSFET has the drawback of a serious series resistance between the extended source and drain region, which results in performance degradation of the device. In other words, the trade-off with using the UTB in CMOS technology is that lowering the HSCE is accompanied by a large parasitic series resistance in-between the extended source and drain region of UTB-MOSFET.

As the DG-MOSFET is an improved extension of UTB-MOSFET, the conducting channel being surrounded by a gate electrode on either side (a double gate) offers better control of over channel i.e. HSCE. Also, a self-aligned raised source and drain in DG-MOSFET has been able to lower the parasitic series resistance. Moreover, lithography technology improved in printing the smaller gate length while the ability to grow the perfect insulator in ever reducing thickness has made the DG-MOSFET gate length reach scales near 22nm technology node. At this level and below 22nm gate length DG-MOSFET

faces a fundamental physics barrier including processing challenges. Also the case of DG-MOSFET alignment of Double Gate MOSFET is very challenging.

There are several multigate devices which have been introduced for below 22nm technology node. In 1998, research efforts of Device Characterizations Lab (DCL), at the University of California at Berkeley, produced another device structure called SOI-FinFET which is the leading device of DG-MOSFET and also fabrication of FinFET which is compatible with CMOS technology. The most unique quality of this device is the conducting channel wrapped around the silicon film (called fin) provides better control over the channel compared with UTB-MOSFET and DG-MOSFET which made it possible to scale down the gate lengths up to 10nm at the research level. This device has been fabricated in industrial research production as well as in university settings. SOI-FinFET is a potential device for CMOS scaling below 22nm technology node.

The purpose of my research work is to verify through numerical simulation that the future scaling trend of CMOS technology using SOI-FinFET will continue below 10nm gate length and that scaling will continue for a few more decades.

CHAPTER 2
CMOS SCALING AND ITS IMPLICATIONS

2.1 Introduction

Metal Oxide Semiconductor Integrated Circuits have fulfilled the world major requirement of electronic devices for hardware computation, communication, automotive, entertainment and other applications. All these requirements have been successively achieved over the past- half century by steady improvement in cost, performance and power consumption. Such a trend of steady improvement has always been the major factor for the growth of the IC industry as well as for invention of new applications. Now, there is skepticism about future growth for the IC industry and if this trend will continue in the future. Since there is no definite direction for IC Industry the million dollar question remains. How will the growth of the trillion dollar microchip industry continue in coming years? As subthreshold leakage, controlling of threshold voltage, oxide thickness and lithography are the major limiting factors for the chip industry to overcome.

2.2 History of Microelectronics

All these major breakthroughs started in 1965 when [1-4] the Noble Prize in physics was shared by three people William Bradford Shockely, John Bardeen and Walter Houser Braittian for their research in semiconductors and their discovery of transistor effects. Afterwards, transistors became the basic buildings blocks of integrated circuits. It is now the

most widely used semiconductor device in CMOS technology for the manufacture of integrated circuits. All these milestones or advancements in integrated circuits [5] started with series of inventions as shown in Figure 1 [6].

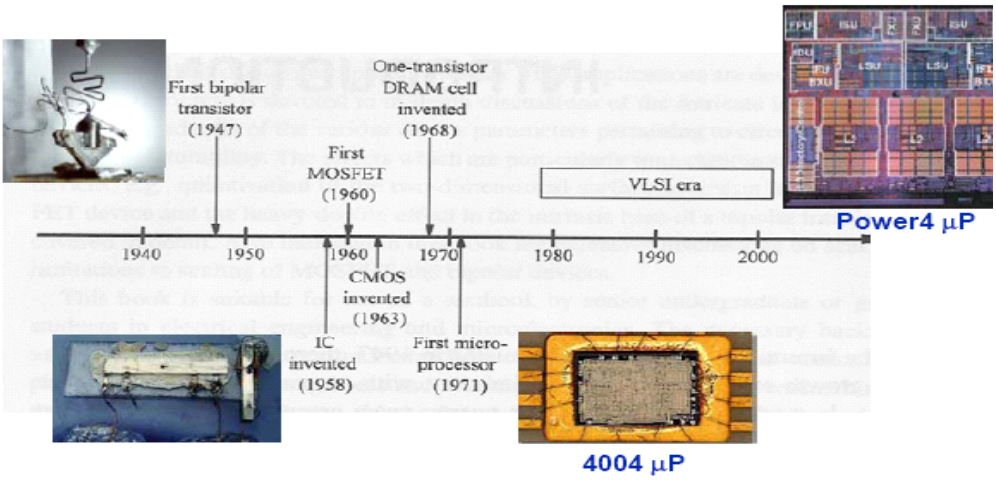

Figure 1. History of Integrated-Circuit

The first invention occurred 1945, when Bell Labs arranged a group to develop a semiconductor replacement for the vacuum tube [7-8]. Later in 1947 this group was able to develop an amplifying circuit utilizing point-contact known as the transistor Bipolar Junction Transistor (BJT) of [1-4] as shown in Figure 2. Jack Killby from Texas Instrumentations and Robert Noyce of Fairchild Semiconductor unbeknownst to each other and before they filed the US patent for similar work in 1959, followed with the integrated circuit invention [9]. First patent was issued to Robert Noyce and later after a legal battle it was shared with Jack Killby. The invention of Jack Kilby and Robert Noyce, also known

as "the chip", has been recognized as one of the most important innovations and significant achievements in the history of humankind [10-13].

Figure 2. First transistor invented at Bell Lab

Just a year after in 1960, the Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) was invented to replace the BJT in integrated circuit. The next invention was reported by Kahng and Sze [14] for first floating gate MOSFET in 1967. All these inventions led to a milestone in the semiconductor industry with the invention of the Complementary-Metal-Oxide-Semiconductor called CMOS by Frank Wanlass in 1967 [15] which is widely used in Microprocessor, Microcontroller, Static RAM and many other digital logic circuits. It is also used widely in analog circuits as an image sensor and data converter and also as

transreceivers. CMOS technology was predominately used in VLSI circuits in the 1980's as well as today because of high noise immunity as well as low static power dissipations. All these inventions starting from the first Bipolar Junctions Transistor to the invention of the CMOS device as shown in Figure 1 has fueled the growth IC industry making it a trillion dollar business every year in the world economy. Also, it has changed human life socially and technologically over the past several decades. Furthermore these changes account as one of biggest achievements in human life as it has changed the way people think and also the way they communicate and carry information among themselves.

2.3 Moore's Law and Technology Scaling

The semiconductor industry has grown every year for the last four decades and will continue for several more decades [16] and CMOS is one of major technologies used to manufacture the integrated circuit. The growth of the semiconductor industry was predicated by the founder of Intel Corporation Gordon Moore in 1965 [17] who published a paper predicting the growth of semiconductor industry and providing a roadmap of the integrated circuit which is still in use today. The paper was submitted to Electronics Magazine which further referred to it as "Moore's Law". This law has become the instrument for improvement of hardware computing as well as for the growth of the semiconductor industry. Gordon Moore [17] devised an empirical formula that every one and half years the number of the transistor will be double in the integrated circuit as shown in Figure 3, [16]. According to Moore's Law, there will be a new technology node or the length of metal line width will reduce every two years. Examples of technology node are 250nm, 180nm,

90nm, 65nm and 45nm, etc. The number indicates the distance between the two metal lines which reduces along with the poly silicon width with every new technology node and the periodic size reduction is called scaling.

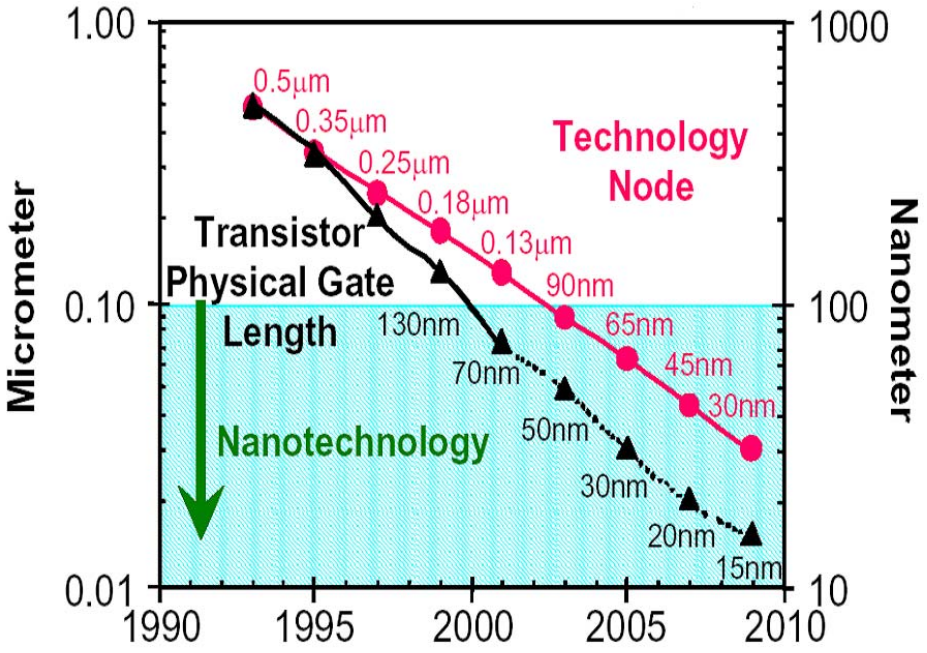

Figure 3. Moore's Law and technology scaling

Table 1 presents the ITRS roadmap for 90nm to 22nm technology node for High Performance (HP) and Low Standby Power (LSTP) for physical gate length (L_g), Equivalent Oxide Thickness (EOT), Power Supply Voltage (V_{dd}), On current (I_{on}) and I_{off}.

2.3.1 Advantages of technology scaling and Moore's Law. The main advantages of technology scaling or reducing new metal line width is to reduce the circuit size by 2. This means at every new generation twice the number of circuits can be fabricated on the

same wafer. Which is the primary engine for driving the cost of IC lower at every new generation since the empirical formula was developed by Gordon Moore in 1960 [17]. This has made possible a drop in price of memory devices 1 million times and has increased the packaging density exponentially and has made the IC inexpensive. Moore's Law has changed the shape of the semiconductor industry and has helped the IC industry to reach more than a trillion dollars business worth world-wide which is more than any other industry. Moore's Law has changed the capability of digital electronics devices in the area of processing speed, memory capacity, sensor speed and even number size of pixels in digital cameras [18].

Table 1. ITRS Roadmap for Technology Node from 90nm to 22nm

Year of Productions	**2004**	**2007**	**2010**	**2013**	**2016**
Technology Node (nm)	90	65	45	32	22
Physical Length L_g (nm)	37	25	18	13	9
EOT (nm) (HP/LSTP)	1.2/1.2	0.9/1.6	0.7/1.3	0.6/1.1	0.5/1.0
Vdd (HP/LSTP)	1.2/1.2	1.1/1.1	1.1/1.0	1.0/0.9	0.9/0.8
I_{on}/W,HP (mA/mm)	1100	1510	1900	2050	2400
I_{OFF}/W,HP (mA/mm)	0.05	0.07	0.1	0.3	0.5
I_{on}/W,LSTP (mA/mm)	440	510	760	880	860
I_{OFF}/W,LSTP (mA/mm)	1e-5	1e-5	6e-5	8e-5	1e-4

Moore's Law is the driving force in the 20^{th} and early 21^{st} centuries for technology and social change. This achievement is unmatched and will continue for at least a few more decades. In 2008 Pat Gelsingerso, [19] from Intel Corporation made the comment that "we see no end in sight of Moore's Law until 2029". Since 1965 Moore's Law has been used in long term planning for research and development [20]. Several countries like the United States, including Europe and Japan have been using revised versions of Moore's

Law as indicators for the growth of semiconductor industry. They continually invest money in researching to upgrade Moore's Law to facilitate future growth of the IC industry.

2.3.2 Scaling: small is beautiful. Since the 1960's the price of a one bit memory device and logic gate has dropped more than a million times at the same time the performance of electronic devices and their packaging density has increased exponentially. This has worked for more than a half-century. This is all possible due to scaling of lateral dimension of the Semiconductor device along with power supply, oxide thickness and threshold voltage and several other parameters within each new technology node as shown in Table 2 where α is a scaling factor and always $\alpha > 1$. Basically all electronic devices become more attractive in high performance with less power dissipations and they became less expensive. "Small is beautiful" appears to be true for semiconductor devices for the last several decades because smaller devices have the fueled growth of the IC industry. Also, "small is beautiful" has created a race among researchers and IC manufacturers who are looking for newer ways to make the semiconductor device smaller. Also, smaller device has created the cycle of investment and research impacting world economics, social and technologies.

Table 2. Generalized Field Scaling

Year of Productions	Constant-field Scaling	Generalized-field scaling
Physical dimension	$1/\alpha$	$1/\alpha$
L, W, T_{ox} wire pitch	α	E/α
Body Doping Concentrations	$1/\alpha$	E/α
Voltage	$1/\alpha$	E/α
Circuit Density	$1/\alpha^2$	$1/\alpha^2$
Capacitance Per Circuit	$1/\alpha$	α (goal)
Circuit Power	$1/\alpha^2$	E/α^2
Power Density	1	E^2
Power- Delay Product (energy per operations)	$1/\alpha^2$	E^2/α^3

2.4 Generalized-Field and Constant-Field Scaling

According to Moore's Law every one-and-half years the number of transistors will double in microprocessors and performance will increase 35% at the same time costs will be lower from the previous technology. All this becomes possible by CMOS scaling of power supply, oxide thickness and threshold voltage along the lateral dimension of MOSFET as shown in Figure 4. At each technology node power supply voltage, threshold voltage, and oxide thickness are scaled aggressively. However, now it is becoming more difficult to continue scaling as scaling of these parameters are reaching material and fundamental limitations. Table 2 shows the relationship between constant-field scaling and generalized-field scaling.

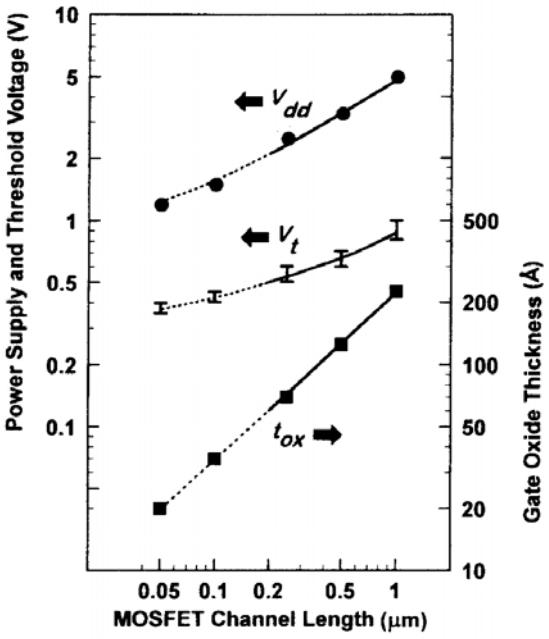

Figure 4. Generalized scaling of V_{dd}, V_t and t_{ox}

2.4.1 Controlling of subthreshold current. Transistor lateral dimension has been scaled vertically and horizontally since 1965 following the empirical formula developed by Gordon Moore. Along the lateral dimensions power supply voltage, threshold voltage and oxide thickness have scaled with respect to CMOS channel length as shown in Figure 4.

The threshold voltage is the minimum gate voltage required to start conduction between source and drain region. The current which flows below threshold voltage is subthreshold current or leakage current. In MOSFET when $V_{gs} < V_t$, practically the current between source and drain should be zero but there is leakage current which flows between the source and drain called subthreshold current as shown in Figure 5 [21]. As the smaller V_t is desirable for higher I_{on} current which means higher performance, but we cannot just arbitrarily set V_t very low for example 0.1V.

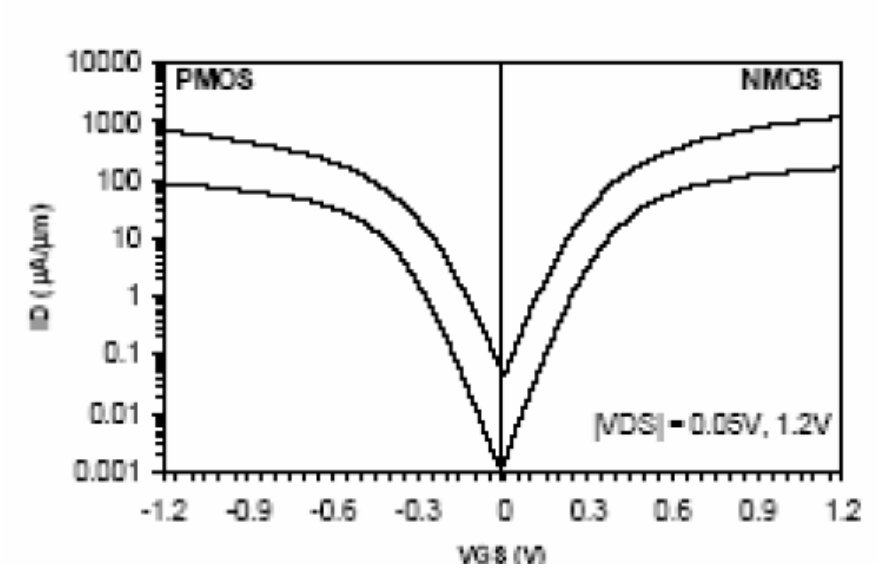

Figure 5. NMOS and PMOS subthreshold curves

As subthreshold current I_{off} is the measure of drain current I_d is $V_{gs} < V_t$ and $V_{gs} = V_{dd}$. It is not possible to control I_{off} current down to zero even if the transistor is OFF or in standby mode. The source-drain leakage has risen tremendously since 2003 as shown in Figure 6 in case of high performance and low performance devices. Subthreshold leakage is one of biggest challenges for CMOS technology today and will be more challenging in the future. For example, there will be a small amount of current flow between the source and drain perhaps 100nA per transistor. As today's microprocessor has one billion transistors [22] and a cell phone has 200 million transistors.

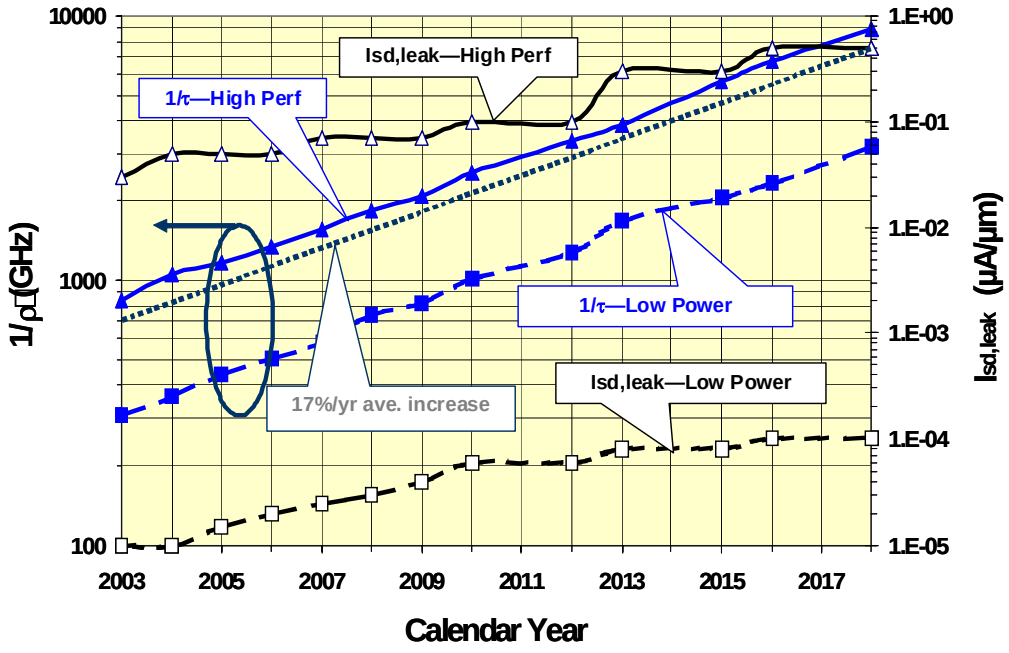

Figure 6. Scaling for high-performance and low-power logic

This will lead to higher static power consumptions as shown in Figure 7 and total power will be dominated by static power instead of dynamic power in the coming few years. This is one of the major challenges of CMOS scaling in the sub-45nm range, as there is insufficient cooling capacity to handle subthreshold leakage (i.e. static power).

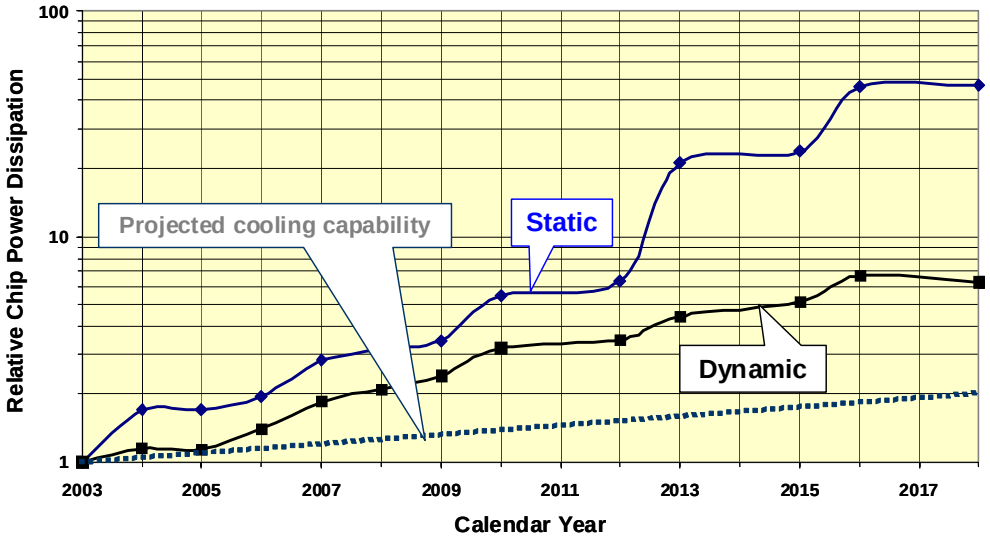

Figure 7. Potential problems with chip power dissipation scaling

2.4.2 Supply voltage scaling. Today's design of power supply voltage is one of biggest challenges for high performance digital circuits which is comparatively less challenging in the case of Low Power Devices, Low Standby Power devices (LSTP) and analog circuits. Reduction of Power supply voltage is one of biggest challenges for CMOS scaling and it will become more challenging in the future as power supply voltage has reached below 1V. It will be reaching 0.6V which will be very close to threshold voltage. $I_{on}\alpha(V_{dd} - V_t) \sim$ very low which will degrade the device performance coming years.

As high performance devices count for more than 50% growth of the IC industry, it is one of the biggest challenges for CMOS scaling and for growth of the IC industry. It will continue to be more critically challenging in the future. Reduction of power supply voltage is one of the fringe behaviors of scaling. Reduction of power supply voltage is not proportional with channel length (L) as shown in Figure 4. The means electrical field in the channel is associated with 250nm to 45nm and has risen tremendously as channel length has become lower. Reduction of Power supply voltage (V_{dd}), threshold voltage (V_t) and gate oxide thickness (t_{ox}) is not proportional vs. channel length or electrical channel length (L_{eff}). Reduction of all these three electrical parameters is not proportional to rate with channel length, along the downscaling of CMOS the voltage level and gate oxide thickness are also reduced. As electron thermal voltage is constant at room temperature, the ratio between the operating voltage and thermal voltage shrinks at each new technology node. This leads to a higher leakage current streaming from thermal diffusion of electrons. At nanometer range along phenomenon such as reliability, power, noise and tunneling through source and drain became limiting factors. Threshold voltage has scaled more aggressively compared with oxide thickness and power supply voltage, and further oxide thickness has scaled more than power supply voltage. As the active power of the new Intel microprocessors is already $50-100$W in range, in the coming years it will require a major breakthrough in power management via architectural innovation, and expensive packaging solutions will be needed.

2.4.3 V_t **roll-off.** Threshold voltage is the minimum voltage required to start current flowing between source and drain. When V_t is set too low then I_{off} current will be very

high. So V_t should not be set too low. Also, V_t will depend on the channel length L of MOSFET. In other words V_t decreases as channel length decreases as shown in Figure 8 [23].

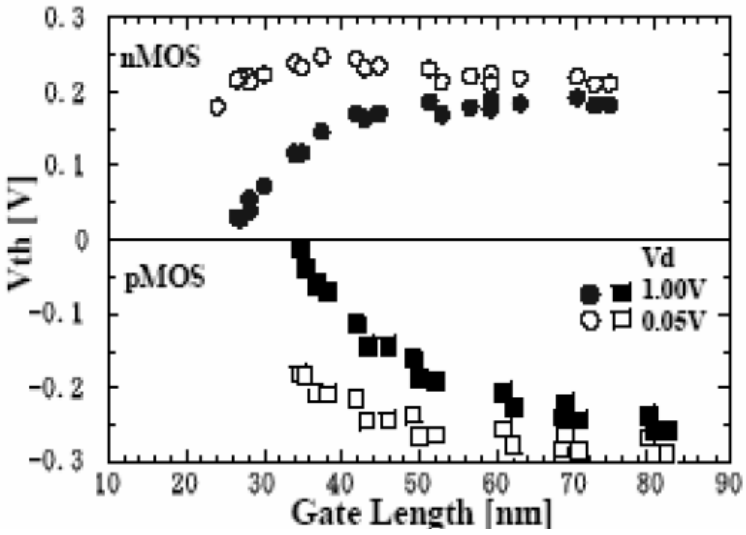

Figure 8. As V_t decreases with decreasing L_g is called V_t roll-off

If V_t is dropped too low then I_{off} current will be too high and that channel length is not acceptable and it called V_t roll-off. We can drop channel length too low then it will be hard to control V_t. The threshold voltage of MOSFET is defined as gate voltage at which significant current begins to flow between the source and drain region. Another big challenge associated with the V_t is that below the threshold voltage current the source and drain should drop immediately to zero. Rather it decreases exponentially, with a slope on logarithmic scale inversely proportional to thermal energy KT. This is due to some of the thermally distributed electrons which have enough energy to overcome the potential

barrier controlled by the gate voltage and flow to drain, even when the gate voltage is zero. Such subthreshold behavior is critical because electrons follow directly fundamental thermodynamics. In other words, it is independent of the power supply voltage and channel length.

2.4.4 Controlling of gate insulator thickness (SiO_2). SiO_2 has been used as the preferred gate oxide insulator in MOSFET since 1960. The thickness of oxide has been scaled from 300nm with technology node 250nm and 1.2nm with the technology node 65nm respectively, as shown in Figure 9 [16] and Figure 4. Thickness of Gate-oxide insulator has scaled along the gate length in the past in order to keep good control over the short-channel effect and also maintain good sub-threshold turn-off slope.

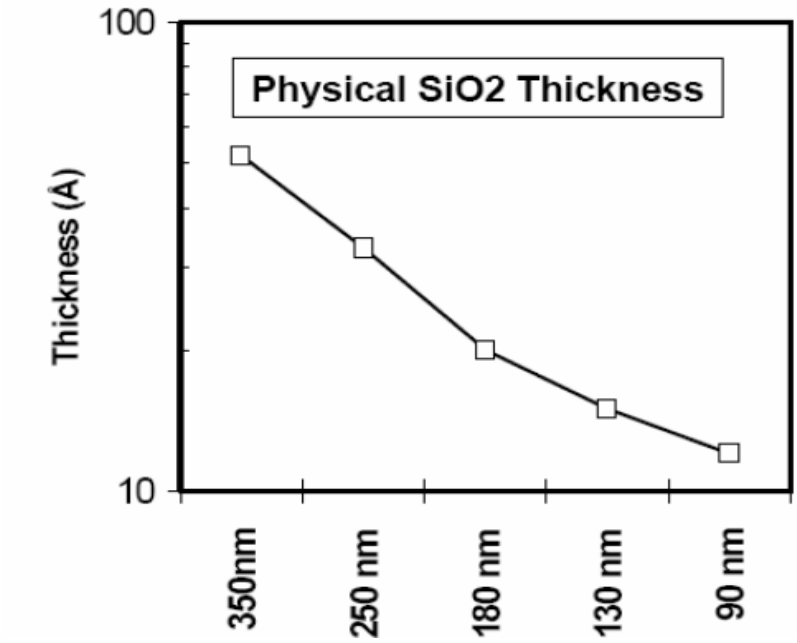

Figure 9. Thickness of SiO_2 scaled along the line width

By reducing the gate oxide insulator this will result in better control over the channel effect compared with the drain voltage. As the thickness of oxide reaches a lower atomic layer further scaling of oxide thickness means it is approaching fundamental limitations. In the past reducing gate oxide SiO_2 (thinner) was one way to control short channel effect. It is amazing that SiO_2 has carried so far without facing any extrinsic limitations, such as surface roughness, defects density, large-scale thickness, and uniformity control. As the thickness oxide film becomes too thin and is subjected to quantum mechanical tunneling shown in Figure 10 [24] there is exponential rise of gate leakage current.

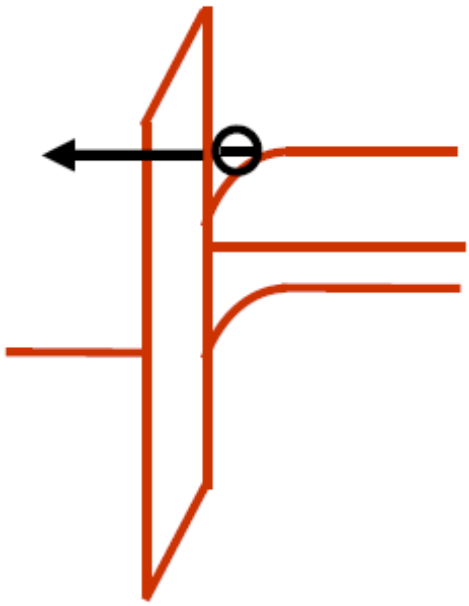

Figure 10. Electron tunneling path through the gate oxide

2.4.5 Discrete doping effects. Discreteness of dopant atoms is another type of physical effect or a statistical variation within the performance and leakage of a chip which is becoming more and more important within the scaling of transistors and may limit scaling in coming years [25-28]. These variations are the net outcome of variations such as: device parameters such as the threshold voltage [29], parasitic resistance and capacitances [30], geometric interconnects leading to variations in interconnects loading [31].

Discrete dopant effect is the average concentrations of doping. It is quite well controlled by the standard ion implantations, as the annealing process does not control exactly where each dopant will end up. Consequently, the process does not control exactly where each dopant will end up. (There is randomness at each atomic scale that do not control exactly where each dopant will end up). Consequently, there is randomness at each end of atomic scale, resulting in spatial fluctuations in local doping concentrations, and these in turn, cause device-to-device variations in MOSFET threshold voltage.

2.5 Scaling-Related Problems and Solutions

The real force behind the growth of the semiconductor industry is CMOS Scaling. Over the last half-century the CMOS device has been scaled aggressively, and it has become a challenging and an interesting research topic for Nanotechnology. As CMOS scaling and design is reaching nanometer range, its design complexity becomes more severe and leaves uncertainty over future CMOS technology scaling. As process downscale into the deep nanometer range [32-33], many new issues arise while old ones becomes more severe. Reliability, noise, power and lithography are the old problems associated with CMOS scaling,

but now as CMOS technology is heading into the nanometer regime, several new challenges like sub-threshold Leakage, oxide failure, dopant fluctuation, V_t roll-off and many other problems become more severe along the old issues. Now, CMOS technology is facing material fabrications as well as design limitations, and there is no definite direction for the microchip industry. Also, at this level basic fundamental device equation which when used in source, drain and channel to predict the electrical behavior of the device is in urgent need of new inventive equations for nanometer devices. The feasibility of Moore's Law is challenged which is considered to be the the main factor for growth of the IC industry over the last four decades. Also, the insulating properties material used in manufacturing of the CMOS devices is challenged. Microelectronics or Integrated circuit is now looking for new direction, or in other words, new inventions are needed for further advancement and/or to keep the growth of semiconductor industry moving upward.

CHAPTER 3

PLANAR, ULTRA THIN BODY AND DOUBLE GATE MOSFET FOR CMOS TECHNOLOGY

3.1 Introduction

In last half century, the rapid advances in microelectronics technology lead to a proliferation of semiconductor devices (MOSFET) and information technology. It has changed the way people transfer information globally. It is one of biggest achievements in human history and has impacted our lives socially and technologically. Transistors are basic building blocks of the integrated circuit. Figure 11 shows the basic structure of MOSFET and its operation.

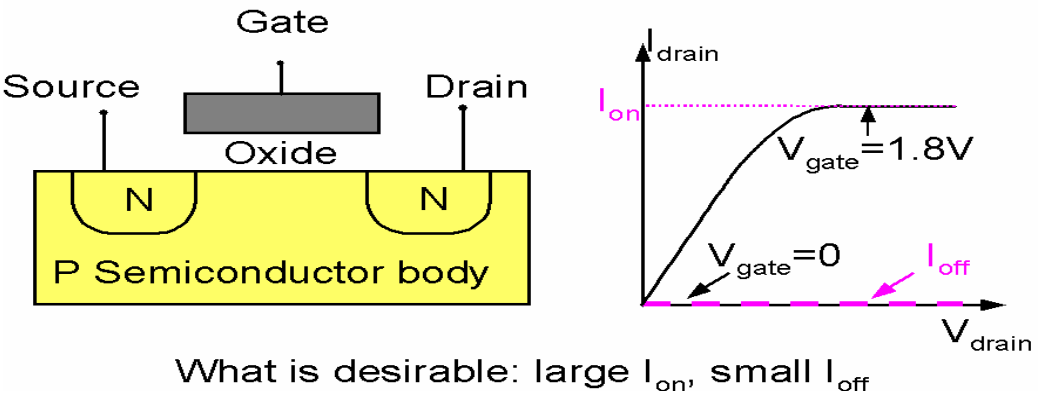

Figure 11. Bulk MOSFET having P-type body and N-type source and drain

The metallic gate electrode and semiconductor channel are electrically insulated from each other. When voltage applied to the metallic Gate terminal called gate voltage (V_g) is used to control the flow of electric charge between the source and drain terminal. It is always desirable for high I_{on} current with zero I_{off} current when Gate voltage is zero or transistor is off.

There are two types MOSFETs; "N-channel" (NMOS) which turns on when high voltage is applied to gate, and another "P-channel" (PMOS) P-channel device which turns-on when low voltage is applied to the gate. N-channel device has n-type in the source and drain and p-type doping in the channel while in the case of P-Channel has a p-type doping in the source and drain and an n-type doping in the channel. It is possible to grow an n-well inside a p-substrate and vice-versa to create a technology where both NMOS and PMOS can coexist. It is known as complementary metal oxide semiconductor as shown in Figure 12.

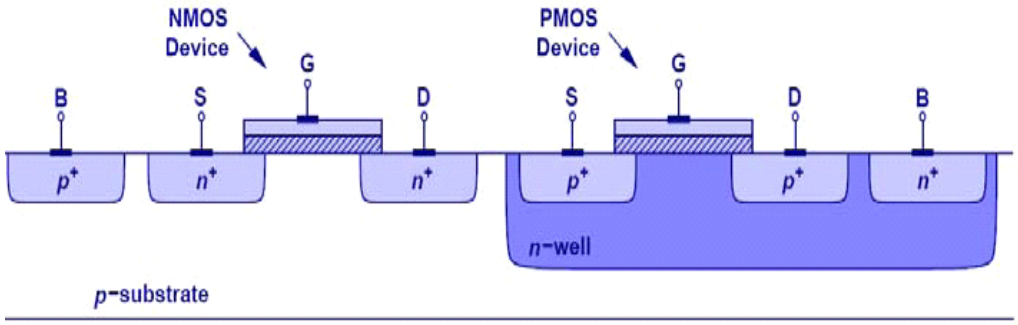

Figure 12. N-channel and P-channel devices operate in complementary

3.2 Planer Bulk MOSFET and Technology Challenges

Planer Bulk CMOS technology has predominately been used for very large scale integrated (VLSI) circuits in the past as now. Planar bulk MOSFET is predominantly used for semiconductor devices in CMOS technology. Transistors have been scaled down in dimension over the last half century and the reason for this scaling is to achieve improvements in speed with reduction in power and cost per function [17]. Results in, today the new Intel Dual Core Processor has a gate length that is below 45nm [21]. Scaling brings closer proximity of source and drain at each technology node results in reduction of the control of gate in channel compare with drain shown in Figure 13. Short channel effects means significant leakage current in the OFF state as shown in Figure 14. As the gate length (L_g) of a transistor is decreased (lateral scaling) below 35nm, source and drain regions become closer and the drain electrical field starts reducing the source channel potential barrier as shown in Figure 15 for different channel length.

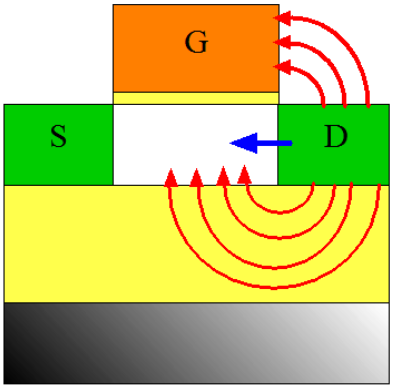

Figure 13. V_g **has less control over channel than** V_d

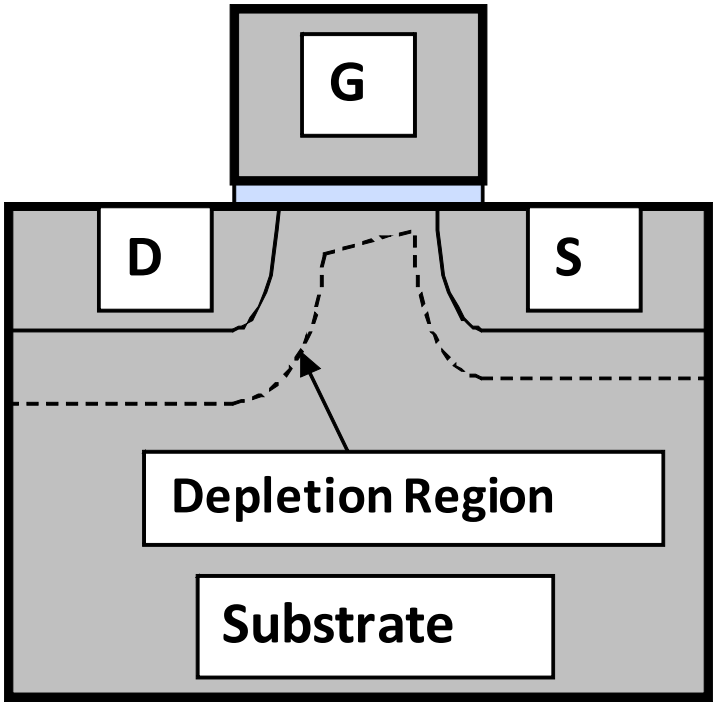

Figure 14. Planar-Bulk Device with depletion region

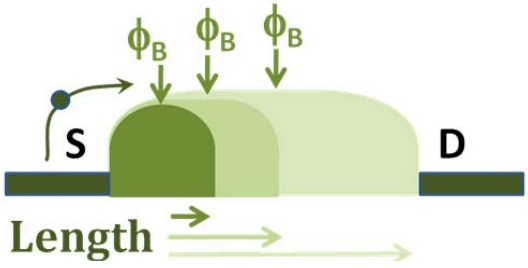

Figure 15. The drain electrical field reduces the source channel potential

The capacitive coupled gate tends to lose control over the channel, especially in the sub-surface region. As the chief outcome of this is an off-state leakage (I_{off}) of the transistor which contributes to the total stand-by power. This is one of biggest challenges for bulk CMOS device and it will become even more challenging in the future. As shown in Figure 16, since 1990 leakage power has sharply increased meaning processor power will be totally dominated by leakage power more than active power in future years.

This capacitive coupling can be improved by decreasing the gate-dielectric thickness (vertical scaling) as shown in Figure 17. The simple descriptions of the competition between the gate and the drain over the control of the channel barrier height. One way to reduce the control of the drain in the channel is to minimize the drain-to-channel capacitance and maximize the gate-to-channel capacitance. In order to increase the gate-to-channel capacitance the thickness of oxide t_{ox} should be reduced as much as possible. Another way to accomplish this by making the width of W_{dep} and X_j too small.

Now, it is very difficult to make these dimensions even smaller as thickness of oxide is reaching the atomic layer. As thickness of t_{ox} is infinitesimally small limited only by very little atomic layer, this provides perfect control over the potential barrier height the layer of silicon very close to the gate or right at the silicon surface of the planar bulk MOSFET. As shown in Figure 18, the drain potential has more control on the leakage current path which is some distance below the silicon surface than the gate voltage. The gate is far away from the submerged location and has less control than the drain. The resulting drain voltage pulls the potential barrier down and allows leakage current to flow through this submerged path as shown in Figure 18, [6].

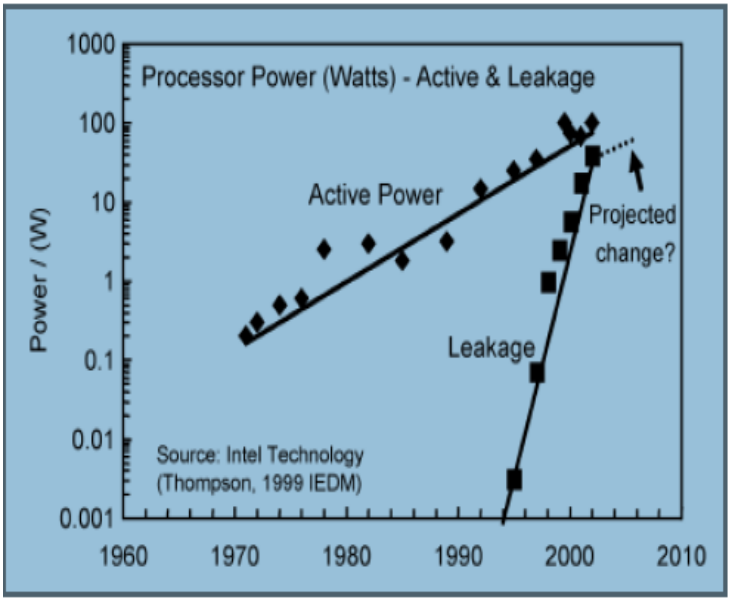

Figure 16. The leakage power is almost 50% of total power

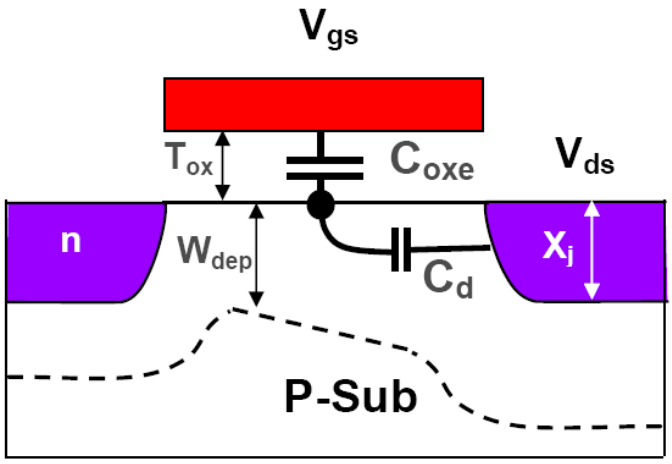

Figure 17. Schematic two-capacitor network in MOSFET

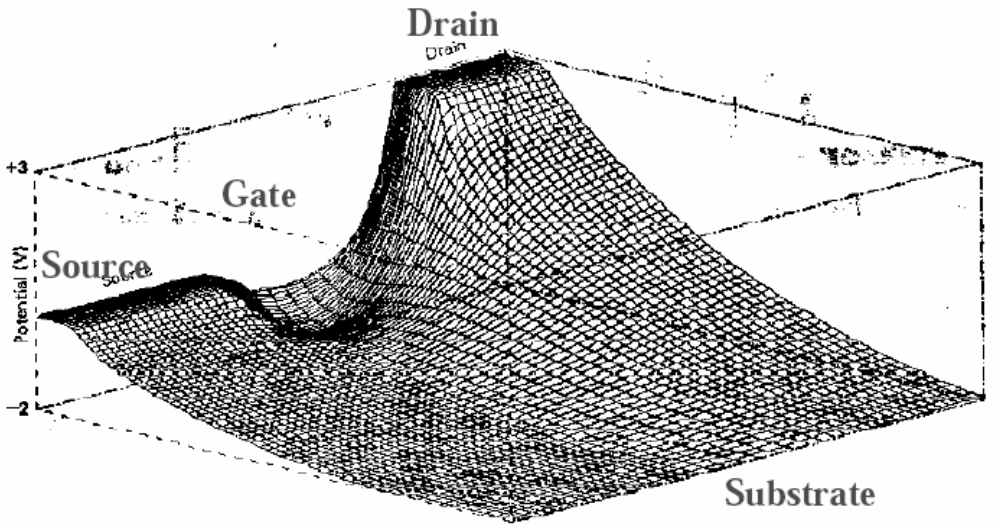

Figure 18. The drain voltage pulls the potential barrier down

To a large extent scaling was not challenged previously. Early signs of scaling limits started more in high performance devices only in the recent technology node. In the past, subthreshold leakage has been solved by using reduced gate oxide thickness, reduced junction depths, as well as complex channel engineering. It is amazing that planer bulk technology has moved so far. However, Planer Bulk Devices have a very simple fabrication process and wafer cost/availability, but challenges such as short channel effects, high doping effects statistical variation, and parasitic junction capacitance limits the further scaling of Plane Bulk technology as mentioned in papers [34-35]. As gate lengths approach 35nm and below, scaling of bulk devices will face limitations such as the thickness of the insulator, low atomic layer, and it will become even more challenging to gain projected performance of 35% per new technology node.

Further down the road, practical material and process technology limits necessitate alternative transistor structures to enable MOSFET scaling below 35nm gate length. Among all devices, the Ultra-Thin-Body and Double Gate MOSFET are the most promising devices for nano-meter range [36-37] and both devices will be discussed in detail in following next two sections.

3.3 Ultra-Thin-Body MOSFET

There are two ways to suppress the subthreshold leakage or submerged leakage path. One is by reducing the semiconductor channel by infinitely small amounts and implanting on surface of SiO_2 shown in Figure 19 [38]. Another way to suppress the submerged leakage path is by reducing the thickness of the oxide as explained previously. Reduced thickness of the semiconductor channel brings the gate electrode closer to the submerged leakage path called Ultra-Thin-Body MOSFET as shown in Figure 20. By reducing the thickness of the Silicon film, a result will be lowered subthreshold leakage as shown in Figure 21 [38] and discussed in [38] in detail.

Reducing the channel a thin semiconductor layer as shown in Figure 19 [38] will ensure that no part of the channel is far from the gate electrode, which provides improved gate control, Less-Induced Barrier Lowering and well control subthreshold leakage automatically provides a shallow junction (compare with Planar Bulk MOSFET). Thickness of the silicon film is made very small, say less than 5nm, so the leakage path is not far from the gate electrode. The worst path of subthreshold along the bottom of the silicon as shown in Figure 19 is still far from the gate electrode.

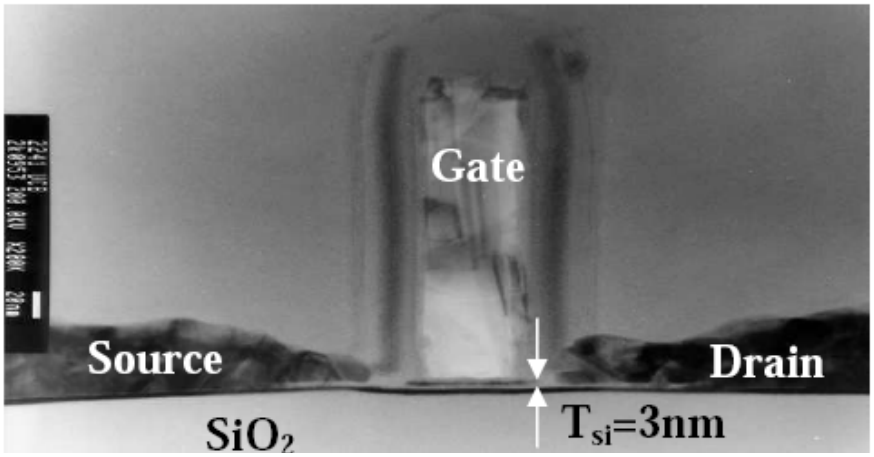

Figure 19. The SEM cross-section of Ultra-Thin-Body

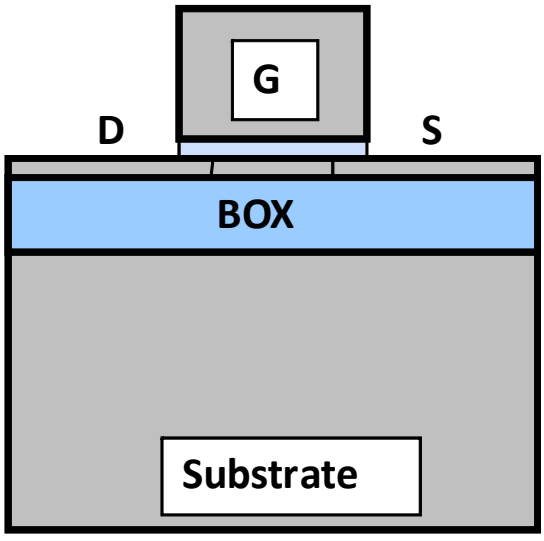

Figure 20. Ultra-Thin-Body MOSFET

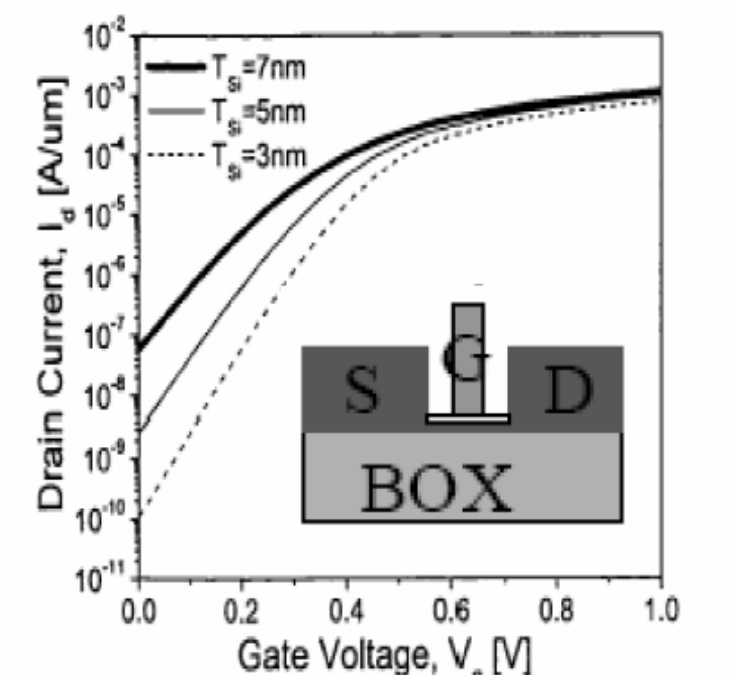

Figure 21. The subthreshold leakage is reduced as the T_{si} made thinner

However, Planer Bulk Device has a very simple fabrication process and wafer cost/availability, but the challenges of short channel effects, high doping effects statistical variation, and parasitic junction capacitance limits the further scaling of Plane Bulk technology as mentioned in papers [34-35].

Ultra-Thin-Body has several advantages over the planer bulk such as lower junction capacitance, lighter doping is possible and threshold voltage V_t can be set by work function of the metal gate electrode. But in the nano-meter ranges below 22nm, Ultra-Thin-Body will face challenges such as Short-channel effect scaling difficulties, sensitivity to Si-thickness (very small) and Wafer cost/availability will limit further scaling of CMOS technology as mentioned in [34].

3.4 Double-Gate MOSFET

Ultra-Thin-Body MOSFET has several limitations below 22nm gate length such as short channel-effect scaling difficulties, sensitivity to Si- thickness (very small), and wafer cost/availability as mentioned in the previous section. To address these challenges and to fill the gap between 22nm to10nm gate length multigate device, Double-Gate MOSFET as shown in Figure 22, is the most promising device as mentioned by [22, 34-35, 37, 39-40]. As Double-Gate MOSFET offers gate control from both sides of the channel, lower junction capacitance, threshold voltage can set by work function of gate electrode, two times drive current, improved gate control, less induced barrier lowering, well-control leakage. All these enhance the scalability of the Double-Gate MOSFET. But nano-meter range below 10nm gate length DG-MOSFET will face the challenges such as two times gate capacitances high series resistance due to raised source/drain region. Alignment of DG-MOSFET required a very complex process.

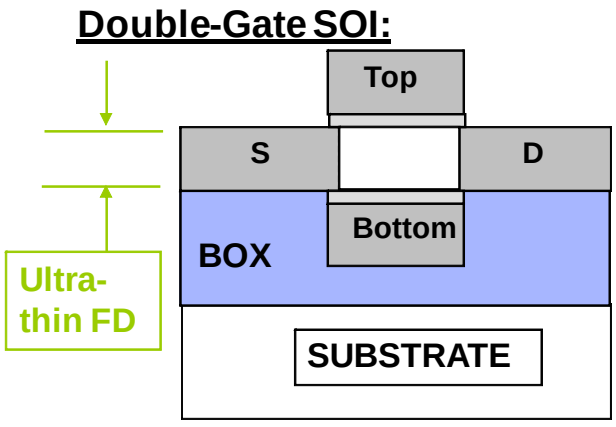

Figure 22. Double-Gate MOSFET for future CMOS device

3.5 Other Multigate Devices Below 22nm Technology Node

According to ITRS roadmap shown in Figure 23 [16] that DG-FinFET or triple gate has better control over variability and short channel effect. It is the future device for CMOS technology compared with planar and DG-MOSFET [22]. Also, there are several multigate devices proposed by AMD, Hitachi, IBM, Infineon, Intel, TSMC, Freescale, UC Berkeley and others such as 1) single gate, 2) double gate, 3) triple gate, 4) quadruple gate, 5) new proposed Pi-gate MOSFET as shown in Figure 24. As mentioned in [41], stability increases by increasing the number of gate, but at the same time process complexity also increases.

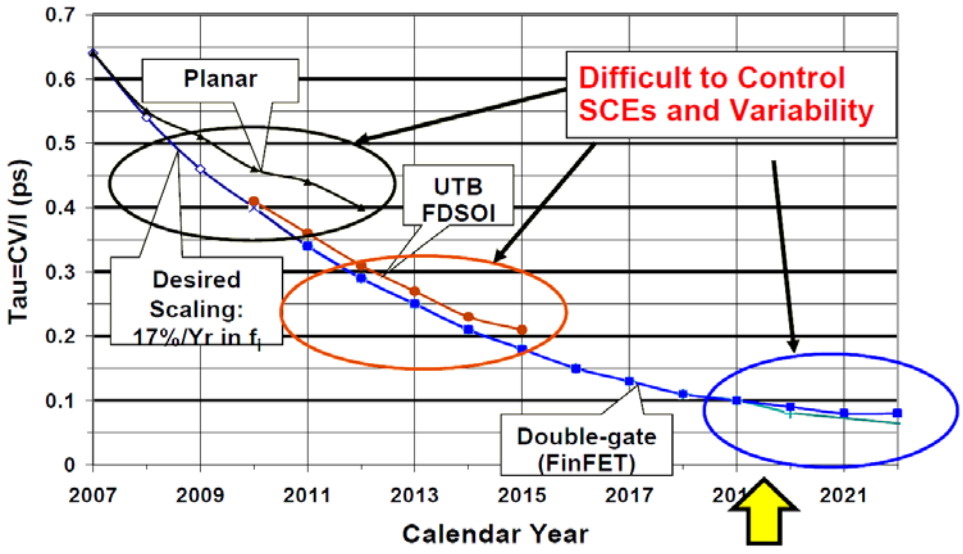

Figure 23. ITRS roadmap for below 22nm

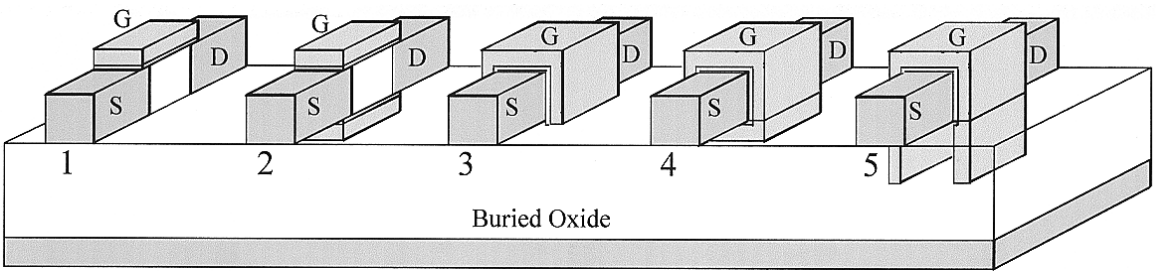

Figure 24. Different gate configurations for SOI devices

CHAPTER 4
DESIGN OF FINFET FOR ACCUMULATION MODE AND ENHANCE MODE DEVICE

4.1 Introduction

There are several multigate devices which have been introduced for below 22nm technology node. The named FinFET originated at the University of California Berkeley, with combined effort from three senior research Professors (Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor) [42]. FinFET is the leading double gate MOSFET, and fabrication of FinFET is compatible with existing CMOS technology [43]. Also, the most unique quality of this device is the conducting channel wrapped around the silicon film called fin which forms the body of FinFET and distinguishes it from other devices. The dimension of the fin determines the effective channel width of the device. Also, as the gate is wrapped around the channel in FinFET, it provides better control over the short channel effect compared with previous counterpart devices like Ultra-Thin-Body and Double-Gate MOSFET. It makes FinFET one of the potential CMOS devices for scaling below sub-10nm gate length. Yet, still there is sizeable road block at this level due to processing and fundamental device physics limitations.

4.2 FinFET Structure

Figure 25 shows the basic structure of a FinFET which is an extension of DG-MOSFET; crucial device dimensions are shown in Table 3. The number of fin between source and drain can be increased more than one. For example, if the fin number is increased to 3, the drive current will be enhanced by 3 times. As H_{fin} is 3 times greater than T_{si} which provides better area efficiency for on-state current. Also, fabrication of FinFET is less complex compared with the other conventional MOSFET.

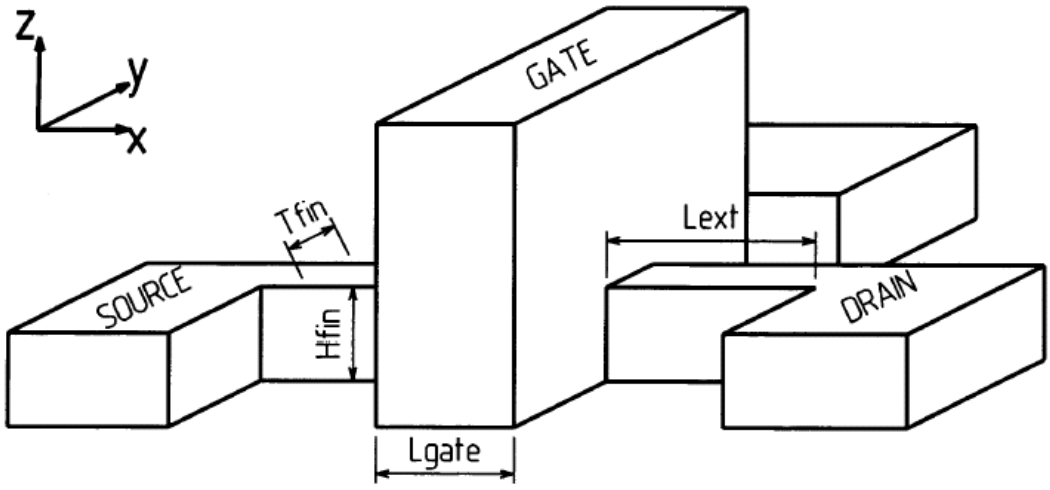

Figure 25. Schematic of FinFET

Table 3. Geometrical Dimensions of the FinFET

Names	Device Parameters
Printed gate length	L_g
Effective gate length which is determined by the distance of the junctions	L_{eff}
Width of the fin which is the distance between the gate oxides of the two gates	T_{fin}
Height of the fin	H_{fin}
Extended length of source and drain to the channel	L_{ext}

4.2.1 3-D structure of FinFET. The 3-D structure of FinFET was developed by the Taurus-Device Editor [44] and geometrical dimensions are shown in Figure 26 for 9nm gate length. In this case, the gate is wrapped all around the channel which provides better control over short channel effects. Also, the height of the fin is 3 times the T_{si} or $H_{fin} = 3T_{si}$ which provides better area efficiency for drive current.

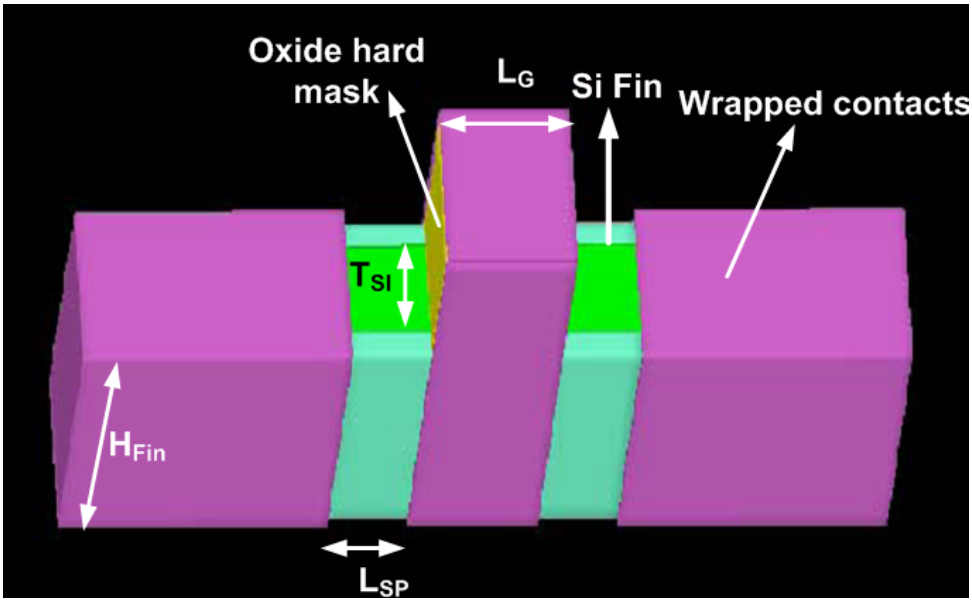

Figure 26. 3-D structure of FinFET was developed by using Taurus-Device Editor

4.2.2 Contour plot. A contour plot is a graphical technique for representing a 3-dimensional surface by plotting constant z slices, called contours, on a 2-dimensional format. That is, given a value for z, lines are drawn for connecting the (x,y) coordinates where that z value occurs. The contour plot is an alternative way to represent a 3-D surface plot [45].

4.2.2.1 Contour plot for net doping in accumulation mode. Contour plot of the ACM is used to show net doping in the source/drain and the channel. In the case of the ACM device the same type of dopant is used in the source/drain and the channel such as $n^+n\ n^+$ or $p^+p\ p^+$as shown in Figure 27. The ACM device has an accumulation layer of the majority carrier and is formed in the channel as electrons in n-type device and holes in the p-type device are also formed. As the source/drain and channel is doped with the same type of dopant this allows the channel to be heavily doped compared with the ECM device.

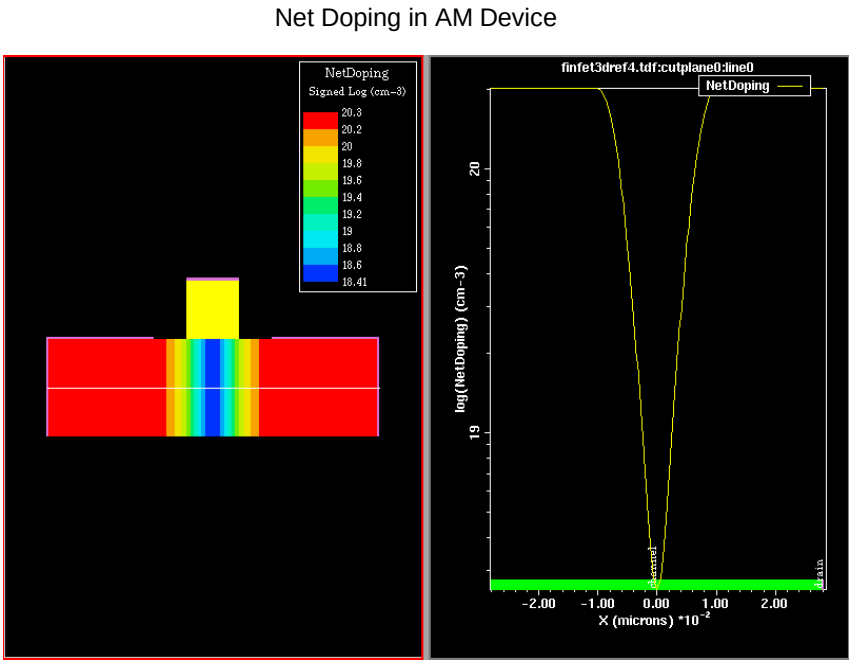

Figure 27. Net doping in the S/D and channel in the ACM device

Having the same type of dopant in the source/drain and the channel region eliminates one of the biggest technological challenges: the ultra-abruptness of the p-n junction

associated with the conventional MOSFET. This also further provides a less challenging processing technique which can be used below the 10nm gate length. Also, it allows higher doping in the channel compared with conventional MOSFET to maintain a low channel resistance in the on-state. Using the ACM FinFET device provides a simple and easy processing technique with no ultra-abruptness p-n junction for nano-scale range or below sub-10nm gate length. This makes the ACM FinFET one of the potential CMOS devices for scaling below 10nm and will allow further scaling for the next few decades.

4.2.2.2 Contour plot for net doping in enhance mode. The contour plot of ECM is used to show net doping in the source/drain and channel. In the case of the ECM device, there is a different type of dopant being used in the source/drain and channel such as n^+p n^+ or p^+n p^+. Figure 28 shows a higher doping concentration used in the source/drain (10^{22} dopant per atom) compared with channel (10^{19} dopant per atom). In the ECM, the device minority charges carrier form the inversion layer in the channel. N-type is in the case of P-type and P-type is in the case of n-type. In sub 10nm gate length the biggest technological challenge is to achieve ultra-high abruptness p-n junction in the case of conventional MOSFET (ECM device) including fundamental device physics limitations.

Net Doping in EM Device

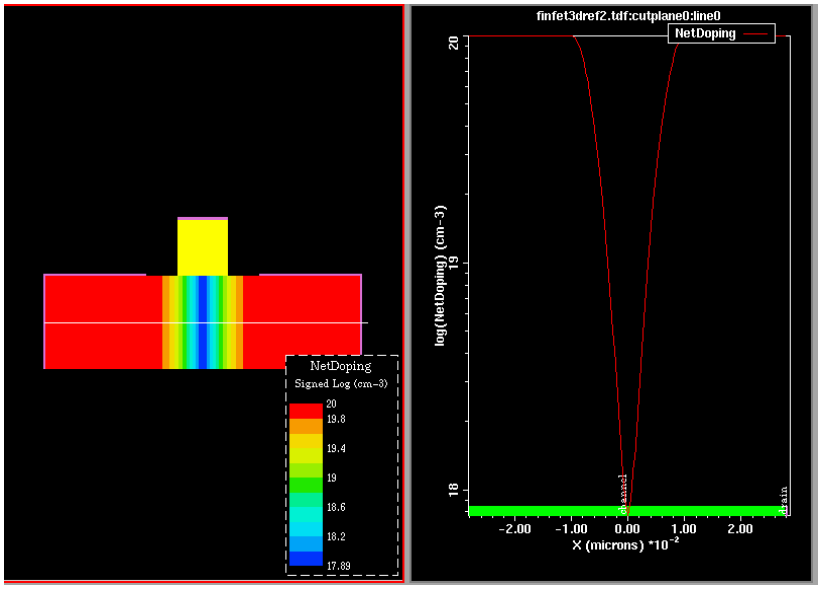

Figure 28. Net doping in S/D and channel in ECM device

4.3 Device Simulation Parameters

The 3-D structure of the Accumulation mode (ACM) and Enhance mode (ECM) FinFET was developed by the Taurus-Device Editor [44] as shown in Figure 26, 27, and 28 previously. The design of both ACM and ECM FinFET was optimized for high-performance IC applications to meet ITRS specification for I_{off} current, for 9nm gate length.

The design of ACM FinFET is optimized, analyzed and compared against conventional ECM FinFET with respect to DIBL, SS, operation and performance characteristics with varying electrical and physical parameters as shown in Table 4 T_{si} (Silicon thickness), σ_{sd} (Source/Drain doping gradient), L_{eff} (electrical channel length), L_{sp} (lacer spacer width) and r_{sd} (Source/Drain Contact Resistance).

Table 4. Device Parametes and Values

Device Parameters	Values
T_{si}	6nm
σ_{sd}	3nm/decade
N_{body}	2E16 cm^3
V_{dd}	0.8V
I_{off}	1E-6A/μm
r_{sd}	8.69E-9W-cm^2
L_{sp}	10nm

Finally, both designs were optimized for 9nm gate length to meet ITRS specifications I_{off}. The simulation solves and includes Poisson, drift-diffusion transport equation and 3D-Schrodinger equation self-consistently.

4.3.1 Drain induced barrier lower (DIBL) and subthreshold swing (SS). Drain induced barrier lower (DIBL) and sub-threshold swing (SS) becomes very important along with the scaling of the CMOS device. Both contribute to a major part of the leakage current. Leakage current is unimportant in higher gate length devices and becomes very important in nano-scaled devices (small gate length device). The leakage current contributes to the static power of the device when the device is in off state. This is the one of major challenges today and will be even more challenging in the coming years when the total power of a device will be dominated by static power more than on-state current means active power. Further, this makes its DIBL and SS very important device parameters in the nano-scale device as both will contribute to the leakage current.

4.3.1.1 Drain induced barrier lower (DIBL). As the gate length or channel length decreases, the barrier to be surmounted by an electron from the source on its way to the drain reduces, which is called drain-induced-barrier-lowering (DIBL) [46] as shown in Fig-

ure 15. This is a major cause of leakage as tunneling current passes through the source and drain. As tunneling current is one of the major challenges for nano-scale in the sub10nm gate length range, it requires a device with higher DIBL to limit the tunneling current.

4.3.1.2 Subthreshold swing (SS). Also contributes to leakage current which is different from leakage current passing through the gate oxide and tunneling current passing through the source and drain.

4.3.2 Calculation of DIBL and SS for ACM and ECM FinFET. Table 5 shows the value of DIBL and SS for ACM and ECM FinFET with r_{sd} when its value equal to zero and 8.69E-9W-cm^2. The following two subsections calculate, compare and analyze DIBL and SS for ACM and ECM FinFET.

Table 5. DIBL and SS for ACM and ECM

		ACM		ECM	
$\mathbf{r}_{sd}$		0	$8.69E-9$W-cm^2	0	$8.69E-9$W-cm^2
DIBL		120mV/V	110mV/V	99mV/V	99mV/V
	$V_{dd} = 50mV$	98mV/dec	115mV/dec	80mV/dec	100mV/dec
	$V_{dd} = 0.8V$	103mV/dec	100mV/dec	95mV/dec	100mmV/dec

4.3.2.1 S-D contact resistance = 0. As shown in Figure 29, drain current I_d is plotted with varying gate voltages V_g through 0.0V to 0.8V. Simulation is repeated for ACM FinFET and ECM FinFET for two different values of drain voltage 50mV and 0.8V with source/drain contact resistance $r_{sd} = 0$. As shown in Figure 29, below the drain induced barrier lower (DIBL) is calculated for ACM and ECM FinFET. Further sub-threshold swing (SS) is calculated for drain voltage for 50mV and 0.8V for ACM and ECM FinFET device. As in the case of the ACM device DIBL is 120mV/V which is higher than in the case of

ECM DIBL equal to 99mV/V. Higher value of DIBL or constant value is desirable along the scaling to limit the tunneling current through source to drain. Also the Sub-threshold swing for ACM and ECM is calculated at 50mV and 0.8V and compared with each other as shown in Figure 29 and Table 5.

The Sub-threshold Swing (SS) for ACM FinFET at 50mV and 0.8V is 98mV/decade and 103mV/decade, respectively. In the case of ECM Sub-threshold Swing (SS) has a lower value at 50mV and 0.8V is 80mV/decade and 95mV/decade compared with ACM FinFET with zero source/drain resistance $r_{sd} = 0$. In case of ACM FinFET there is less variation in SS at 50mV and 0.8V compared with SS in ECM having a larger window of variation in SS between these two drain voltages.

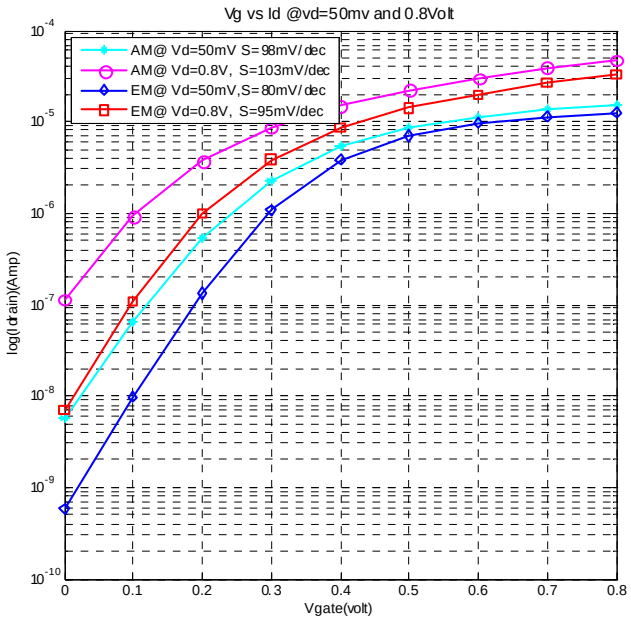

Figure 29. SS and DIBL with $r_{sd} = 0$ for ACM and ECM FinFET

4.3.2.2 S-D contact resistance = 8.69E-9W-cm^2. As shown in Figure 30 I_d drain current is plotted with varying gate voltage through 0.0V to 0.8V. Simulation is repeated for ACM FinFET and ECM FinFET for two different values of the drain voltage 50mV and 0.8V with source/drain contact resistance $r_{sd} = 8.68E-9$W-cm^2. As shown in Table 5 and Figure 30 below the Drain Induced Barrier Lower (DIBL) and Subthreshold Swing (SS) for ACM and ECM device is calculated with source/drain contact resistance $r_{sd} = 8.68E-9$W-cm^2. In the case of the ACM device DIBL is 110mV/V which is higher than in the case of ECM DIBL, it is equal to 100mV/V.

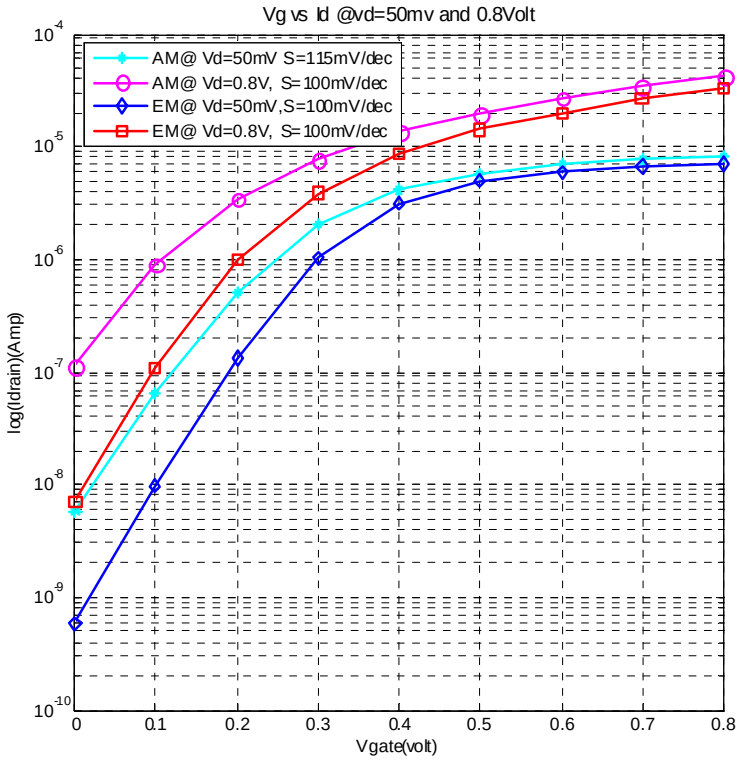

Figure 30. SS and DIBL with $r_{sd} = 8.69E-9$W-cm^2 for ACM and ECM FinFET

Further, the Subthreshold Swing for ACM and ECM is calculated at 50mV and 0.8V is calculated and compared with each other. In this case ECM FinFET has fewer variations in SS at these two different drain voltages when value of contact resistance r_{sd} is included.

4.4 I_d-V_d Plot

The next two subsections are I_d-V_d plots for ACM and ECM FinFET where I_d is plotted with varying V_d through 0.0V to 0.8V for gate voltage is equal to $V_g = 0.0$, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7 and 0.8V. The simulations repeated for different value of $r_{sd} = 8.68E-9$W-cm^2 and $r_{sd} = 0$ for ACM and ECM FinFET. All four case simulations solve and include Poisson, drift-diffusion transport equation and 3D-Schrodinger equation self-consistently for ACM and ECM FinFET.

4.4.1 I_d-V_d plot for ACM FinFET. The following two subsections are the explanation for I_d-V_d plot for ACM FinFET with r_{sd} =0 and 8.68E-9W-cm^2.

4.4.1.1 S-D contact resistance = 0. The plot of I_d-V_d with fixed value V_g and r_{sd} which equals zero for ACM FinFET as shown in Figure 31. In this case, V_d will vary from 0.0V to 0.8V. In each plot of I_d-V_d the value of the gate voltage increases through a step of 0.1V, starting from 0.0V to 0.8V the value of the contact r_{sd} remains constant in each plot. As gate voltage increases from 0.0V to 0.8V, the drain current I_d also increases along the subthreshold current. When gate voltage and drain voltage equal to 0.8V, there will be maximum drain current with the highest subthreshold current as well. Also minimum I_d as well as minimum I_{off} with drain and gate voltages equal to 0.0V.

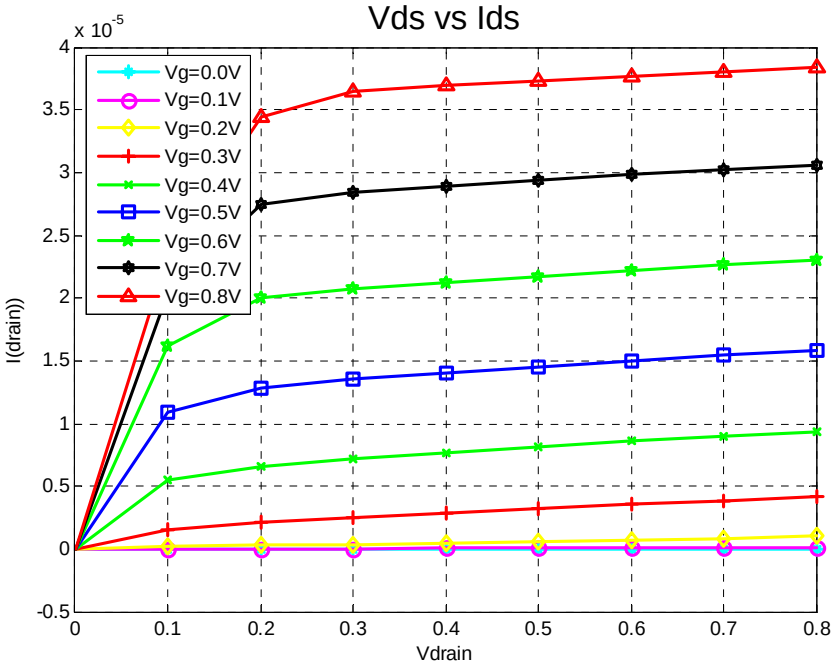

Figure 31. I_{ds}-V_{ds} **for ACM FinFET with** $r_{sd} = 0$

4.4.1.2 S-D contact resistance = 8.68E-9W-cm^2 The plot of the drain current vs. drain voltage with fixed value V_g and $r_{sd} = 8.68E-9$W-cm^2 for ACM FinFET as shown in Figure 32. In this case, drain voltage will vary from 0.0V to 0.8V. In each plot of I_d-V_d the value of the gate voltage increases through a step of 0.1V, starting from 0.0V to 0.8V. The value of the contact r_{sd} remains constant. As gate voltage increases from 0.0V to 0.8V the drain current I_d (on current) also increases along the subthreshold current. As gate voltage and drain voltage equal to 0.8V, there will be maximum drain current with the highest subthreshold current as well. Also, minimum drain current as well as minimum subthreshold leakage current with drain and gate voltages equal to 0.0V as shown in Figure 32. By comparing the $I_d - V_d$ plots of ACM FinFET for case ($r_{sd} = 0$) and case

($r_{sd} = 8.68$E-9W-cm^2), the value of drain current in case ($r_{sd} = 8.68$E-9W-cm^2) has higher value.

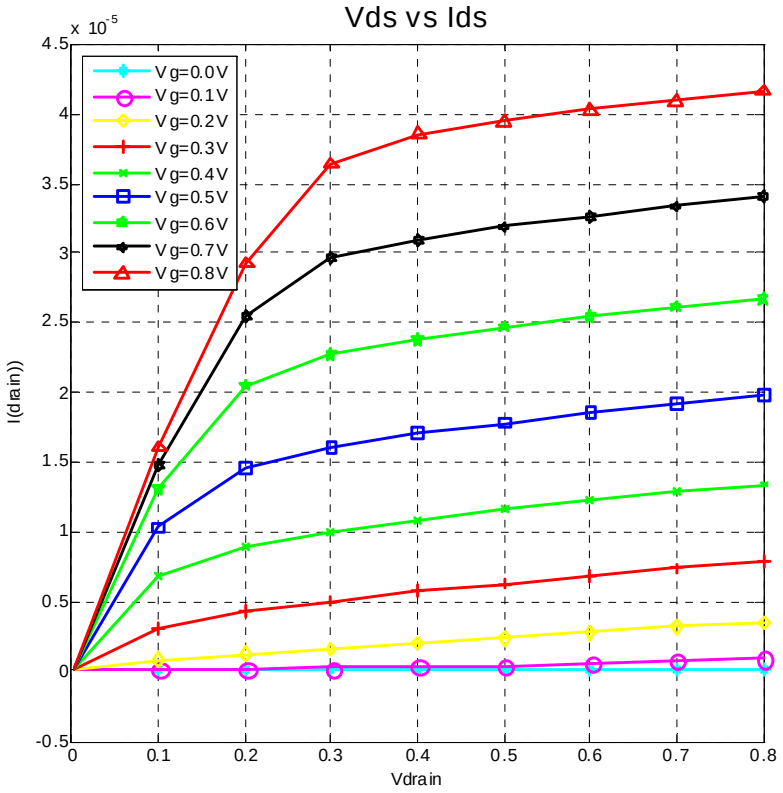

Figure 32. I_{ds}-V_{ds} **for ACM FinFET with** $r_{sd} = 8.68E - 9$**W-cm**^{2}

4.4.2 I$_d$-V$_d$ plot for ECM FinFET. The following two subsections are the explanation for I_d-V_d plot for ECM FinFET with $r_{sd} = 0$ and 8.68E-9W-cm^2.

4.4.2.1 S-D contact resistance = 0. The plot of the drain current vs. drain voltage with fixed value V_g and $r_{sd} = 0$ for ECM FinFET as shown in Figure 33. In this case drain voltage will vary from 0.0 V to 0.8V. In each plot of I_d-V_d the value of the gate voltage

increases through a step of 0.1V, starting from 0.0V to 0.8V the value of the contact r_{sd} remains constant. As gate voltage increases from 0.0V through to 0.8V the drain current I_d (on current) also increases along the subthreshold current. At gate voltage and drain voltage equal to 0.8V, there will be maximum drain current with the highest subthreshold current as well. Also, minimum drain current as well as minimum subthreshold leakage current with drain and gate voltages equal to 0.0V as shown in Figure 33.

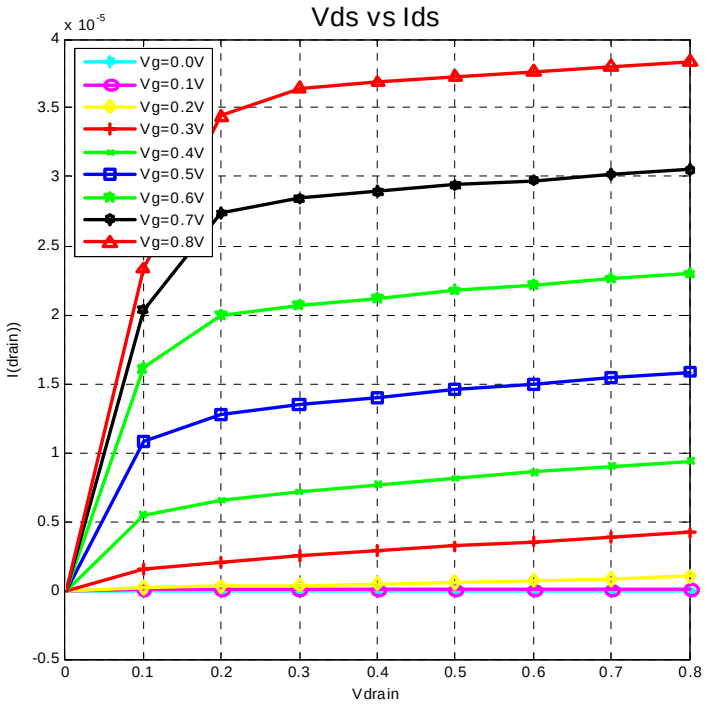

Figure 33. I_{ds}-V_{ds} **for ECM FinFET with** $r_{sd} = 0$

4.4.2.2 S-D contact resistance = 8.68E-9W-cm^2. The plot of the drain current vs. drain voltage with fixed value V_g and $r_{sd} = 8.68E-9$W-cm^2 for ECM FinFET as shown in Figure 34. In this case drain voltage will vary from 0.0V to 0.8V. In each plot of I_d-V_d the value of the gate voltage increases through a step of 0.1V, starting from 0.0V to 0.8V the value of the contact r_{sd} remains constant. As gate voltage increases from 0.0V through to 0.8V the drain current I_d (on current) also increases along the subthreshold current. As gate voltage and drain voltage equal to 0.8V, there will be maximum drain current with the highest subthreshold current as well. Also, minimum drain current as well as minimum subthreshold leakage current with drain and gate voltages equal to 0.0V as shown in Figure 34.

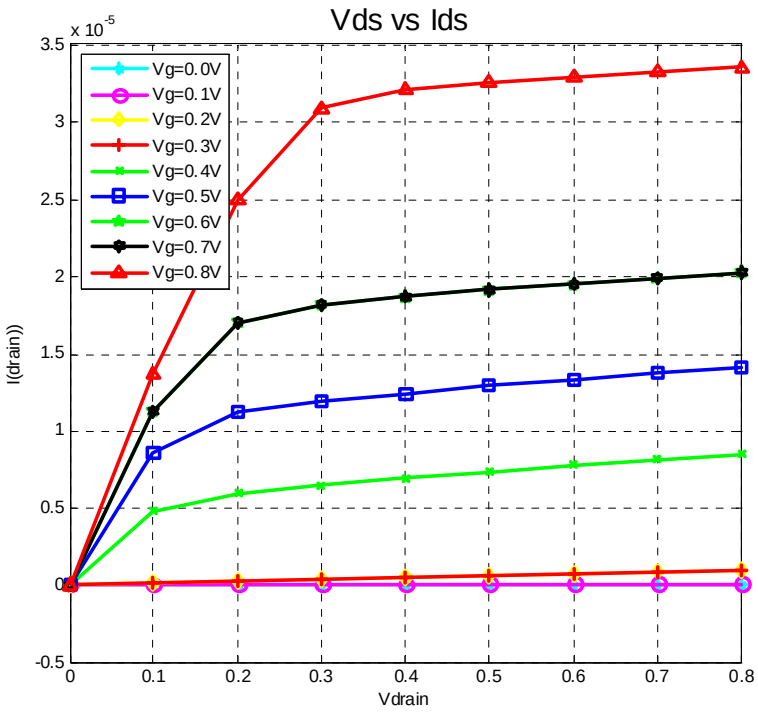

Figure 34. I_{ds}-V_{ds} **for ECM FinFET with** $r_{sd} = 8.68E-9$**W-cm**^{2}

By comparing the $I_d - V_d$ plots of ECM FinFET for case ($r_{sd} = 0$) and case ($r_{sd} = 8.68$E-9W-cm^2), the value of drain current in case ($r_{sd} = 0$) has higher value.

4.5 I_{ds}-V_{gs} Plot with Varying T_{si} and σ_{sd}

In this section the main objective is to find the best possible and practical value of electrical channel length (L_{eff}) which is different than gate length (L_g). Gate length is manually controlled in fab, but electrical channel length (L_{eff}) depends on several other parameters: σ_{sd} (source/drain gradient), T_{si} (silicon thickness) and L_{sp} (lacer spacer width); also, device performance depends on L_{eff}. The electrical channel length L_{eff} is very important in small scale devices, but it is less important in higher gate length devices. It is always desirable that $L_{eff} \geqslant L_G$ in the case of nano scale devices, which further makes the right selection of device parameters σ_{sd}, L_{sp} and T_{si} crucial in achieving correct L_{eff}. In this case $L_{sp} = 10$nm is chosen as the best possible value after repeating the set of simulations containing the value of L_{sp} from 5nm to 25nm. The total channel length is $2L_{sp} + L_g$~29nm when $L_{sp} = 10$nm. In each plot, I_{ds} (drain current) vs. V_{gs} (gate voltage) is plotted with varying gate voltages from 0.0V to 0.8V and source/drain gradient σ_{sd} from 1 to 5nm/decade. The values of drain voltage $V_{ds} = 0.8$V and a source/drain contact resistance $r_{sd} = 8.68E - 9$W-cm^2 are kept constant in each plot. The same set of simulation is repeated for $T_{si} = 5.5, 4.5, 3.5, 2.5$ for ACM FinFET and ECM FinFET. All simulations solve and include the Poisson, drift-diffusion transport equation and the 3D-Schrodinger equation self-consistently for ACM and ECM FinFET.

4.5.1 I_{ds}-V_{gs} **plot for ACM and ECM FinFET with** $T_{si} = 5.5$**nm.** The following next two subsection is I_{ds}-V_{gs} plot for ACM and ECM FinFET for $T_{si} = 5.5$nm and $L_{sp} = 10$nm for $\sigma_{sd} = 1, 2, ..., 5$nm/decade.

4.5.1.1 Accumulation mode (ACM) FinFET. As shown in Figure 35, the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. The effective channel length L_{eff} is calculated for each value of source/drain gradient σ_{sd} from 1 to 5nm. As source/drain gradient σ_{sd} increases the value of electrical channel length, L_{eff}, decreases with increase in drain current as well as subthreshold leakage current.

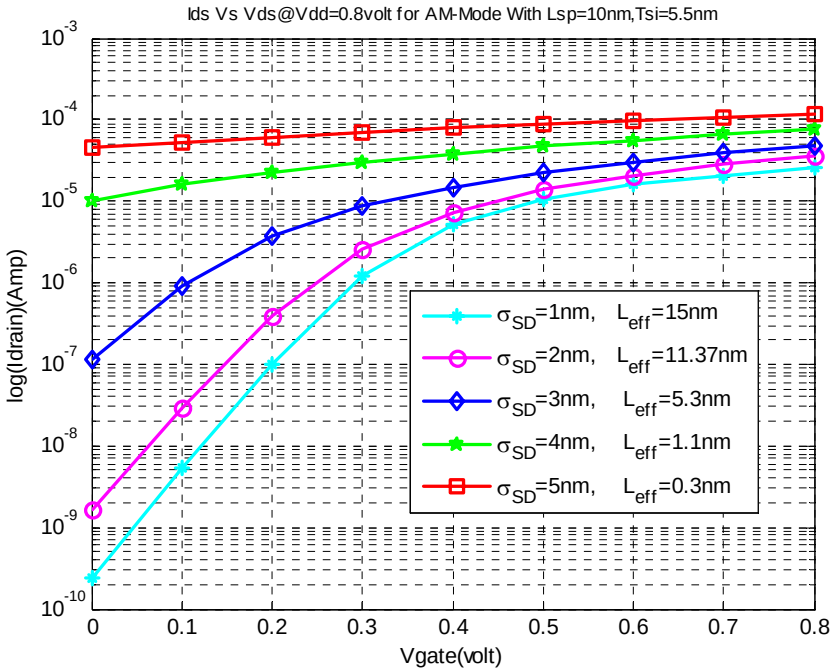

Figure 35. I_{ds} **vs** V_{gs} **for** $T_{si} = 5.5$**nm for ACM FinFET**

The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} (drain current) with the lowest subthreshold leakage current I_{off} as well as source/drain gradient $\sigma_{sd} = 5$nm has lowest L_{eff} with the highest I_{ds} current with highest subthreshold leakage current I_{off} shown in Figure 35. Also, as the σ_{sd} increases, the gate voltage V_g means the gate electrical field has less control over channel compared with the drain voltage. Referring to Table 6, in case of $\sigma_{sd} = 1$ and 2nm $L_{eff} > L_g$ and also in this case the gate voltage has more control over channel compared with the drain voltage. When $\sigma_{sd} = 3$nm the gate voltage still has control over channel but definitely gate voltage, V_g, has less control over channel compared with the plot of $\sigma_{sd} = 1$ and 2nm. In the case of $\sigma_{sd} = 4$ and 5nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g also channel is underlapped under the gate electrode. The best possible and practical value of σ_{sd} lies in between 2nm and 3nm. For $\sigma_{sd} = 1$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in case of $\sigma_{sd} = 4$nm and 5nm, smaller value of L_{eff} compared with L_g has worst subthreshold leakage current due to higher short channel effect and tunneling current through source to drain region.

Table 6. Tsi=5.5nm for ACM FinFET

$\boldsymbol{\sigma_{sd}}$	$\mathbf{L_{eff}}$	**Comparison**
1nm	15.00nm	$L_{eff} > L_g$
2nm	11.37nm	$L_{eff} > L_g$
3nm	05.30nm	$L_{eff} < L_g$
4nm	01.10nm	$L_{eff} < L_g$
5nm	00.30nm	$L_{eff} < L_g$

4.5.1.2 Enhance mode (ECM) FinFET. As shown in Figure 36, the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. The effective channel length L_{eff} is calculated for each value of source/drain gradient σ_{sd} through 1 to 5nm. As source/drain gradient σ_{sd} increases the value of electrical channel length, L_{eff}, decreases with increase in drain current as well as subthreshold leakage current.

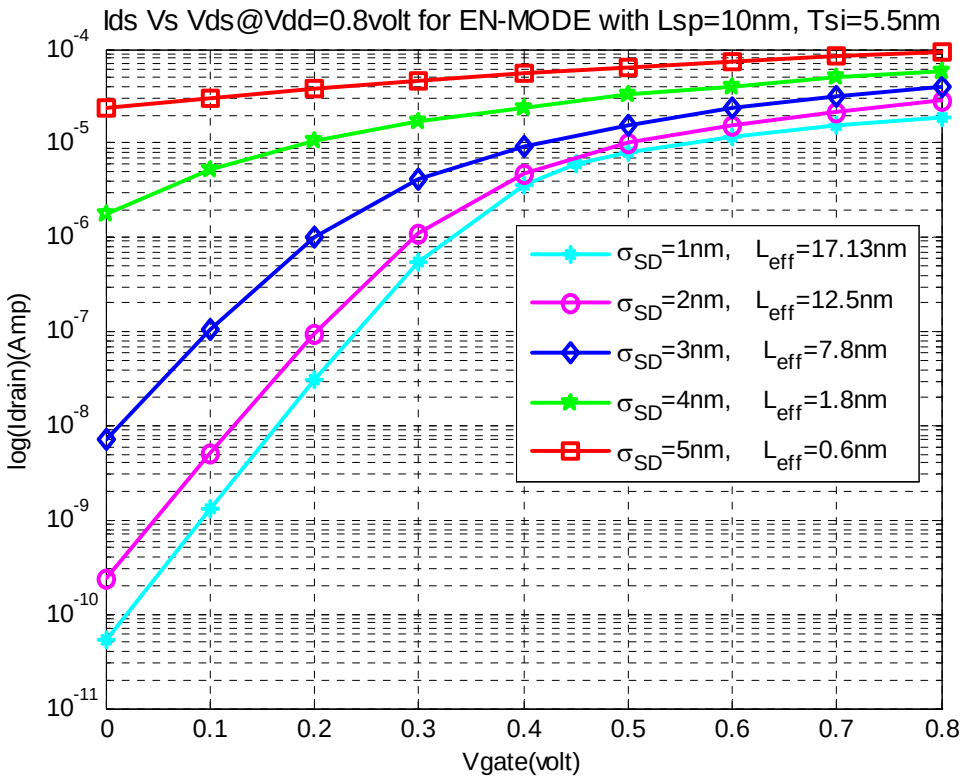

Figure 36. I_{ds} **vs** V_{gs} **for** $T_{si} = 5.5$**nm for ECM FinFET**

The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} (drain current) with the lowest subthreshold leakage current I_{off} as well as source/drain gradient $\sigma_{sd} = 5$nm has lowest L_{eff} with the highest I_{ds} current with highest subthreshold leakage current I_{off} as shown in Figure 36. As the σ_{sd} increases, the gate voltage V_g means electrical field produced by gate voltage starts losing control over channel compared with the drain voltage.Referring to Table 7, in case of $\sigma_{sd} = 1$ and 2nm $L_{eff} > L_g$ and also in this case the gate voltage has more control over channel compared with the drain voltage. When $\sigma_{sd} = 3$nm the gate voltage still has control over channel but definitely gate voltage, V_g, has less control over channel compared with the plot of $\sigma_{sd} = 1$ and 2nm. In the case of $\sigma_{sd} = 4$ and 5nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g also channel is underlapped under the gate electrode. The best possible and practical value of σ_{sd} lies in between 2nm and 3nm. For $\sigma_{sd} = 1$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in case of $\sigma_{sd} = 4$nm and 5nm, smaller value of L_{eff} compared with L_g has worst subthreshold leakage current due to higher short channel effect and tunneling current through source to drain region.

Table 7. Tsi=5.5nm for ECM FinFET

σ_{sd}	L_{eff}	Comparison
1nm	17.13nm	$L_{eff} > L_g$
2nm	12.50nm	$L_{eff} > L_g$
3nm	07.80nm	$L_{eff} < L_g$
4nm	01.80nm	$L_{eff} < L_g$
5nm	00.60nm	$L_{eff} < L_g$

4.5.1.3 Comparison. The difference in Figure 35, 36 and Table 6 and 7, L_{eff} is greater in case of ECM FinFET device compared with ACM FinFET for the same value of σ_{sd}. In case of ECM FinFET has lower subthreshold leakage current as well lower I_{on} current compared with ACM FinFET for $T_{si} = 5.5$nm.

4.5.2 I_{ds}-V_{gs} plot for ACM and ECM FinFET with $T_{si} = 4.5$nm. The following next two subsection is I_{ds}-V_{gs} plot for ACM and ECM FinFET for $T_{si} = 4.5$nm and $L_{sp} = 10$nm for $\sigma_{sd} = 1, 1.5, 2, ..., 4.5$nm/decade.

4.5.2.1 Accumulation mode (ACM) FinFET. As shown in Figure 37 the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 1.5, 2, ..., 4.5$nm/decade. For each value of source/drain gradient σ_{sd} the effective channel length L_{eff} is calculated. As source/drain gradient σ_{sd} increases the value of L_{eff} electrical channel length decreases with increase in drain current. In this case, the simulation is successfully completed for the value of $\sigma_{sd} = 1, ..., 3.5$ nm and only these values will be used for comparison and analyzation amongst each other. The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} (drain current) with the lowest subthreshold current I_{off} as well as source/drain gradient $\sigma_{sd} = 3.5$nm has lowest L_{eff} with the highest I_{ds} current with highest subthreshold current I_{off}. Also, as the σ_{sd} increases, the gate voltage V_g or gate electrical field has less control over channel compared with the drain voltage. Referring to Table 8, for $\sigma_{sd} = 1, 1.5, 2$ and 2.5nm the electrical channel length $L_{eff} > L_g$ and the gate voltage has full control over channel compared with drain voltage. When $\sigma_{sd} = 3$ and 3.5nm has better on state current and the electrical channel length L_{eff} has lower value than the physical gate length

L_g which means higher subthreshold leakage current compared with $\sigma_{sd} = 1, 1.5, 2$ and 2.5nm. Also in this case the best possible and practical value σ_{sd} of should be between 2 and 3 nm.

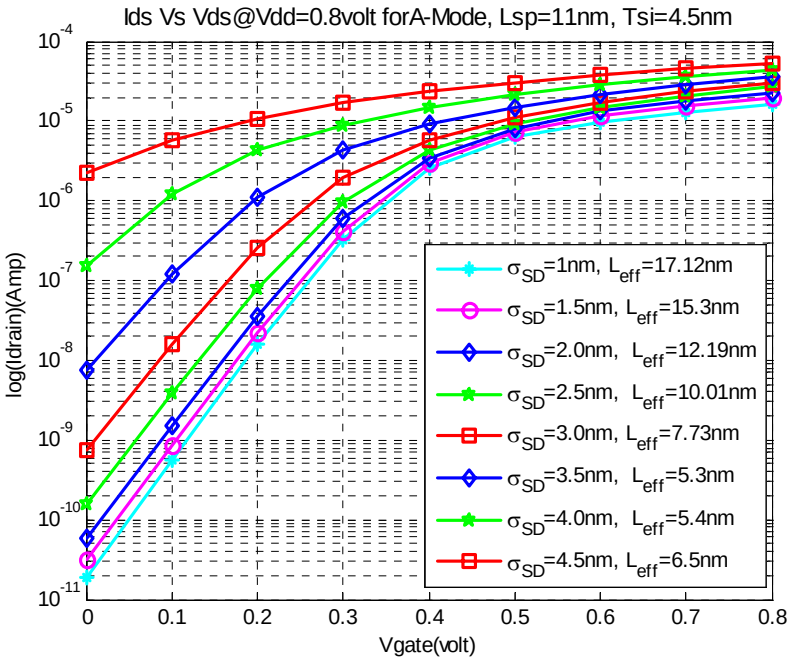

Figure 37. I_{ds} **vs** V_{gs} **for** $T_{si} = 4.5$**nm for ACM FinFET**

Table 8. Tsi=4.5nm for ACM FinFET

σ_{sd}	L_{eff}	Comparison
1nm	17.12nm	$L_{eff} > L_g$
1.5nm	15.30nm	$L_{eff} > L_g$
2nm	12.19nm	$L_{eff} > L_g$
2.5nm	10.01nm	$L_{eff} > L_g$
3nm	07.73nm	$L_{eff} < L_g$
3.5nm	05.30nm	$L_{eff} < L_g$
4nm	05.40nm	$L_{eff} < L_g$
4.5nm	06.30nm	$L_{eff} < L_g$

4.5.2.2 Enhance mode (ECM) FinFET. As shown in Figure 38 the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 1.5, 2, ..., 4.5$nm/decade.

In this case, the simulation is successfully completed for the value of $\sigma_{sd} = 1, ..., 3$nm and only these values will be used for comparison and analyzation amongst among each other. For each value of source/drain gradient σ_{sd} the effective channel length L_{eff} is calculated. As source/drain gradient σ_{sd} increases the value of L_{eff} electrical channel length decreases with the increase in subthreshold leakage current as well as drain current.

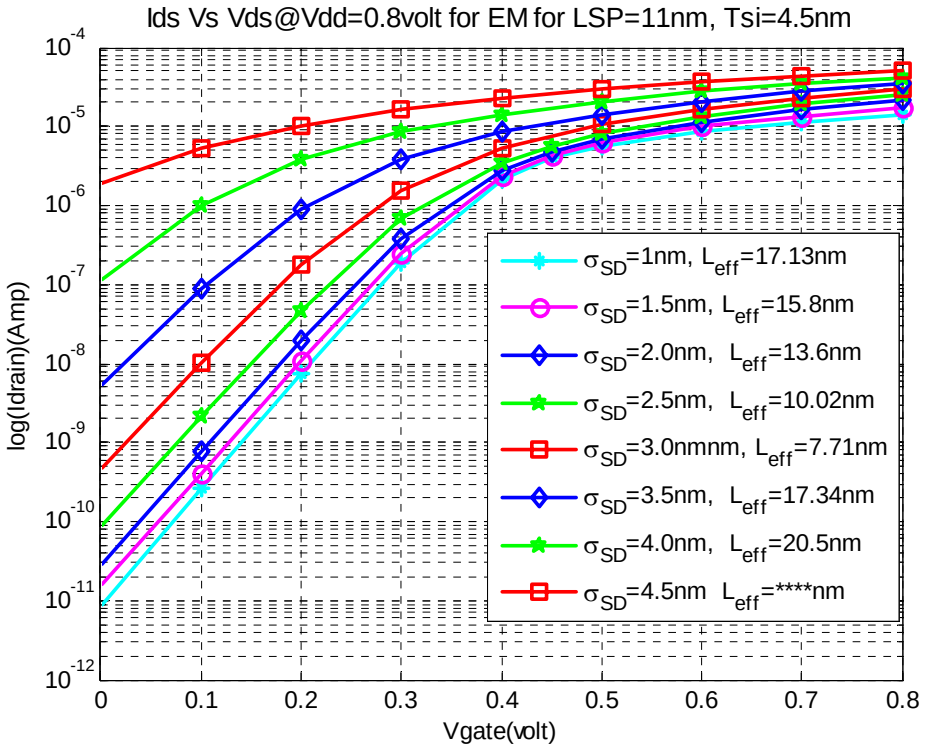

Figure 38. I_{ds} **vs** V_{gs} **for** $T_{si} = 4.5$**nm for ECM FinFET**

The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} (drain current) with the lowest subthreshold leakage current I_{off} as well as source/drain gradient $\sigma_{sd} = 3$nm has lowest L_{eff} with the highest I_{ds} current with highest subthreshold leakage current I_{off}. Also, as the σ_{sd} increases, the gate voltage V_g or gate electrical field has less control over channel compared with the drain voltage. Referring to Table 9, for $\sigma_{sd} = 1, 1.5, 2$ and 2.5nm the electrical channel length $L_{eff} > L_g$ and the gate voltage has full control over channel compared with drain voltage. When $\sigma_{sd} = 3$ has better on state current and the electrical channel length L_{eff} has lower value than the physical gate length L_g which means higher subthreshold leakage current compared with $\sigma_{sd} = 1, 1.5, 2$ and 2.5nm. Also in this case the best possible and practical value σ_{sd} of should be between 2.5 and 3 nm.

4.5.2.3 Comparison. In both cases of ACM and ECM FinFET for $T_{si} = 4.5$nm has lower subthreshold leakage current compared with ACM and ECM FinFET for $T_{si} = 5.5$nm. As the short channel effect is better control in the case of $T_{si} = 4.5$nm.

Table 9. Tsi=4.5nm for ECM FinFET

σ_{sd}	L_{eff}	**Comparison**
1nm	17.13nm	$L_{eff} > L_g$
1.5nm	15.80nm	$L_{eff} > L_g$
2nm	13.60nm	$L_{eff} > L_g$
2.5nm	10.02nm	$L_{eff} > L_g$
3nm	07.71nm	$L_{eff} < L_g$
3.5nm	17.34nm	$L_{eff} < L_g$
4nm	20.50nm	$L_{eff} < L_g$
4.5nm	$***$nm	

4.5.3 I_{ds}-V_{gs} plot for ACM and ECM FinFET with $T_{si} = 3.5$nm. The following next two subsection is I_{ds}-V_{gs} plot for ACM and ECM FinFET for $T_{si} = 3.5$nm and $L_{sp} = 10$nm for $\sigma_{sd} = 1, 2, ..., 5$nm/decade.

4.5.3.1 Accumulation mode (ACM) FinFET. As shown in Figure 39 the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. In this case, the simulation is successfully completed for the value of $\sigma_{sd} = 2, 3,$ and 4nm and only these values will be used for comparison and analyzation amongst each other. The effective channel length L_{eff} is calculated for each value of source/drain gradient σ_{sd} from 1 to 5nm.

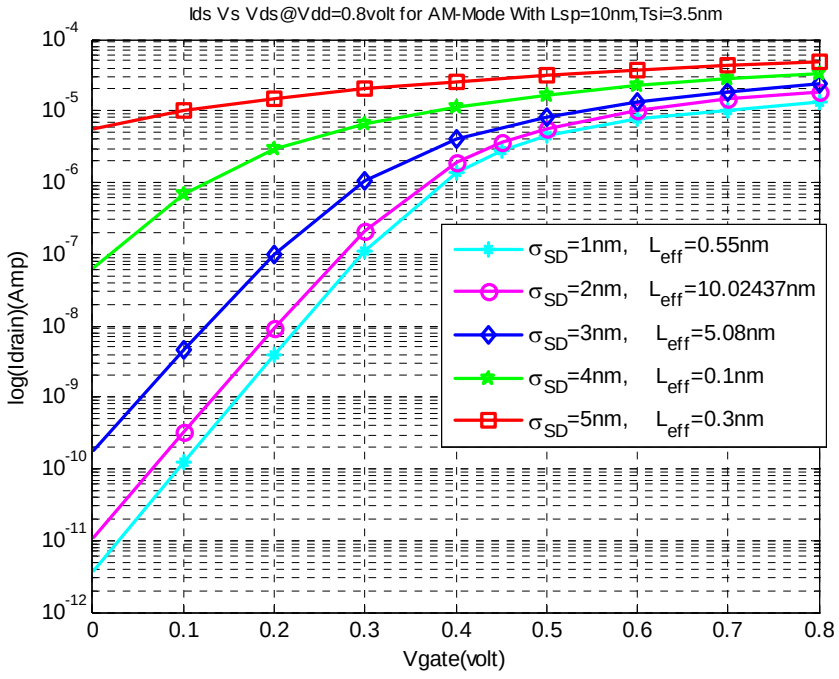

Figure 39. I_{ds} vs V_{gs} for $T_{si} = 3.5$nm for ACM FinFET

As the source/drain gradient σ_{sd} increases the value of the L_{eff} decreases with an increase in drain current as well as in subthreshold leakage current. The source/drain gradient $\sigma_{sd} = 2$nm has the highest L_{eff} with the lowest I_{ds} and the lowest subthreshold leakage current I_{off} as well as source/drain gradient $\sigma_{sd} = 4$nm has lowest L_{eff} with the highest I_{ds} current and the highest I_{off} shown in Figure 39 and Table 10. Also, as the σ_{sd} increases, the gate voltage V_g (means the gate electrical field) has less control over the channel compared with the drain voltage. Referring to Table 10, for $\sigma_{sd} = 2$nm, $L_{eff} > L_g$ and also in this case the gate voltage has more control over the channel compared with the drain voltage. When $\sigma_{sd} = 3$nm the gate voltage still has control over the channel, but definitely gate voltage V_g has less control over the channel compared with the plot of $\sigma_{sd} = 2$nm. In the case of $\sigma_{sd} = 4$nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g. Also the channel is underlapped under the gate electrode. The best possible and practical value of σ_{sd} lies in between 2nm and 3nm. For $\sigma_{sd} = 2$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in case of $\sigma_{sd} = 4$nm, smaller value of L_{eff} compared with L_g has the worst subthreshold leakage current due to a higher short channel effect and tunneling current through the source to drain region.

Table 10. Tsi=3.5nm for ACM FinFET

$\boldsymbol{\sigma_{sd}}$	$\mathbf{L_{eff}}$	**Comparison**
1nm	00.55nm	$L_{eff} > L_g$
2nm	10.02nm	$L_{eff} > L_g$
3nm	05.80nm	$L_{eff} < L_g$
4nm	00.10nm	$L_{eff} < L_g$
5nm	00.30nm	$L_{eff} < L_g$

4.5.3.2 Enhance mode (ECM) FinFET. As shown in Figure 40 the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of the source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. In this case, the simulation is successfully completed for the value of $\sigma_{sd} = 1, 2, 4$ and 5nm and only these values will be used for comparison and analyzation amongst each other. The effective channel length L_{eff} is calculated for each value of the source/drain gradient σ_{sd} through 1 to 5nm.

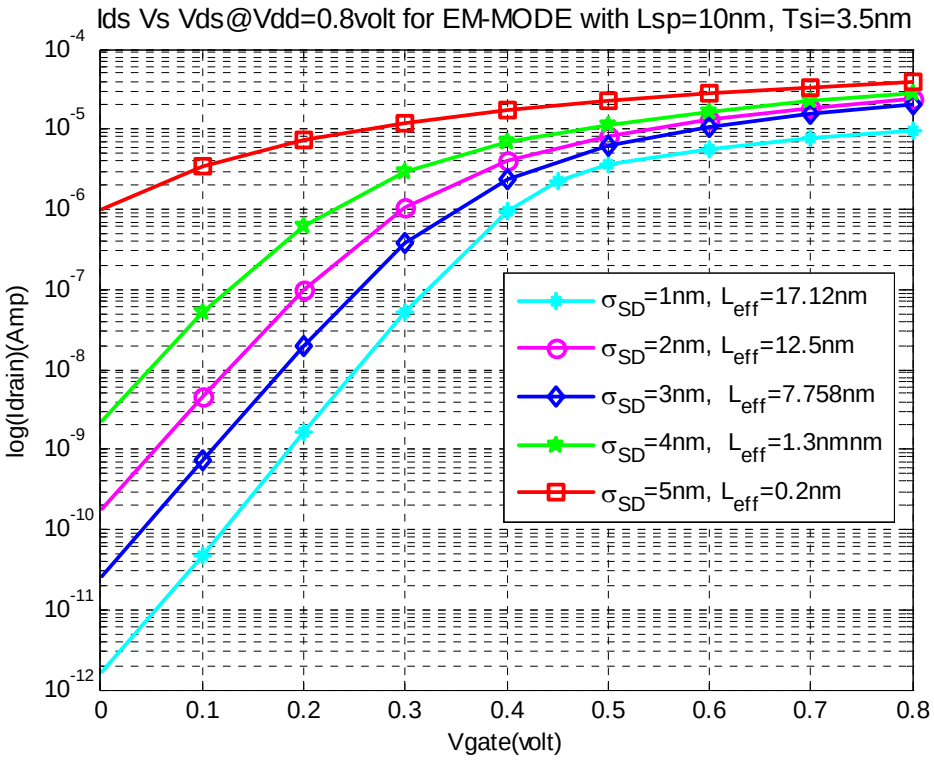

Figure 40. I_{ds} **vs** V_{gs} **for** $T_{si} = 3.5$**nm for ECM FinFET**

As the source/drain gradient σ_{sd} increases the value of the L_{eff} decreases with an increase in the drain current as well as the subthreshold leakage current. The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} and the lowest subthreshold leakage current I_{off} as well as the source/drain gradient $\sigma_{sd} = 5$nm has the lowest L_{eff} with the highest I_{ds} current and highest subthreshold leakage current I_{off} as shown in Figure 40 and Table 11. As the σ_{sd} increases, the gate voltage V_g means the electrical field produced by the gate voltage starts losing control over the channel compared with the drain voltage. Referring to Table 11, in the case of $\sigma_{sd} = 1$ and 2nm $L_{eff} > L_g$ and also in this case, the gate voltage has more control over the channel compared with the drain voltage. In the case of $\sigma_{sd} = 4$ and 5nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g also the channel is underlapped under the gate electrode. For $\sigma_{sd} = 1$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in the case of $\sigma_{sd} = 4$nm and 5nm, smaller value of L_{eff} compared with L_g has the worst subthreshold leakage current due to the higher short channel effect and tunneling current through the source to drain region. The best possible and practical value of σ_{sd} lies in between 2nm and 3nm.

Table 11. Tsi=3.5nm for ECM FinFET

σ_{sd}	L_{eff}	Comparison
1nm	17.12nm	$L_{eff} > L_g$
2nm	12.50nm	$L_{eff} > L_g$
3nm	07.75nm	$L_{eff} < L_g$
4nm	01.30nm	$L_{eff} < L_g$
5nm	00.20nm	$L_{eff} < L_g$

4.5.3.3 Comparison. The difference in Figure 39 and 40 that L_{eff} is greater and the short channel effects are well controlled in ECM FinFET for same value of T_{si}, L_{sp} and σ_{sd}.

4.5.4 I_{ds}-V_{gs} plot for ACM and ECM FinFET with $T_{si} = 2.5$nm. The following subsections are I_{ds}-V_{gs} plotted for ACM and ECM FinFET for $T_{si} = 2.5$nm and $L_{sp} = 10$nm for $\sigma_{sd} = 1, 2, ..., 5$nm/decade.

4.5.4.1 Accumulation mode (ACM) FinFET. As shown in Figure 41, the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of the source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. In this case, the simulation is successfully completed for the value of $\sigma_{sd} = 1, 3, 4$ and 5nm and only these values will be used for comparison and analyzation amongst each other. The effective channel length L_{eff} is calculated for each value of the source/drain gradient σ_{sd}.

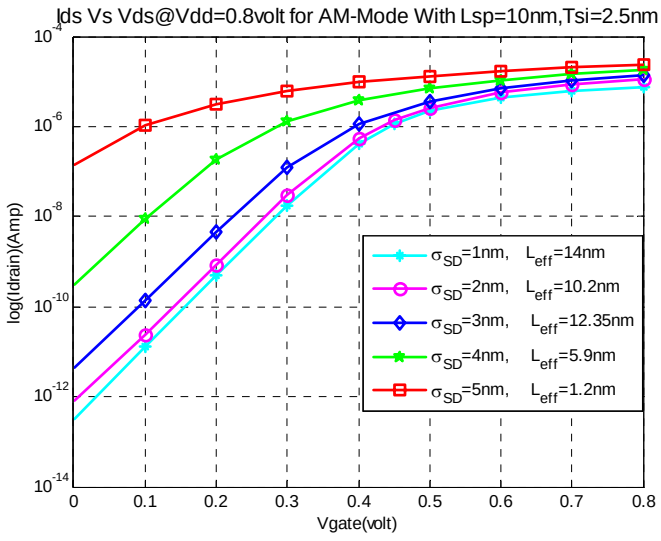

Figure 41. I_{ds} vs V_{gs} for $T_{si} = 2.5$nm for ACM FinFET

As the source/drain gradient σ_{sd} increases the value of the L_{eff} decreases with an increase in the drain current as well as the subthreshold leakage current. The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} and the lowest subthreshold leakage current I_{off} as well as the source/drain gradient $\sigma_{sd} = 5$nm has the lowest L_{eff} with the highest I_{ds} current and the highest I_{off} as shown in Figure 41. Also, as the σ_{sd} increases, gate voltage V_g means the gate electrical field has less control over the channel compared with the drain voltage. Referring to Table 12 in case of $\sigma_{sd} = 1$ and 3nm $L_{eff} > L_g$ and also in this case the gate voltage has more control over the channel compared with the drain voltage. When $\sigma_{sd} = 4$nm the gate voltage still has control over the channel but definitely gate voltage, V_g, has less control over channel compared with the plot of $\sigma_{sd} = 1$ and 3nm. In the case of $\sigma_{sd} = 5$nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g also the channel is underlapped under the gate electrode. For $\sigma_{sd} = 1$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in the case of $\sigma_{sd} = 5$nm, the smaller value of L_{eff} compared with L_g has the worst subthreshold leakage current due to the higher short channel effect and tunneling current through the source to drain region. The best possible and practical value of σ_{sd} lies in between 3nm and 4nm.

Table 12. Tsi=2.5nm for ACM FinFET

σ_{sd}	L_{eff}	Comparison
1nm	14.00nm	$L_{eff} > L_g$
2nm	10.20nm	$L_{eff} > L_g$
3nm	12.35nm	$L_{eff} > L_g$
4nm	05.90nm	$L_{eff} < L_g$
5nm	01.20nm	$L_{eff} < L_g$

4.5.4.2 Enhance mode (ECM) FinFET. As shown in Figure 42, the plot is between I_{ds} vs. V_{gs} with the drain voltage $V_{ds} = 0.8$V. This simulation is repeated for different values of source/drain gradient $\sigma_{sd} = 1, 2, 3, ..., 5$nm/decade. The effective channel length L_{eff} is calculated for each value of the source/drain gradient σ_{sd} through 1 to 5nm. As source/drain gradient σ_{sd} increases the value of electrical channel length, L_{eff}, decreases with an increase in the drain current as well as the subthreshold leakage current. The source/drain gradient $\sigma_{sd} = 1$nm has the highest L_{eff} with the lowest I_{ds} and the lowest subthreshold leakage current I_{off} as well as the source/drain gradient $\sigma_{sd} = 5$nm has lowest L_{eff} with the highest I_{ds} current and highest subthreshold leakage current I_{off}.

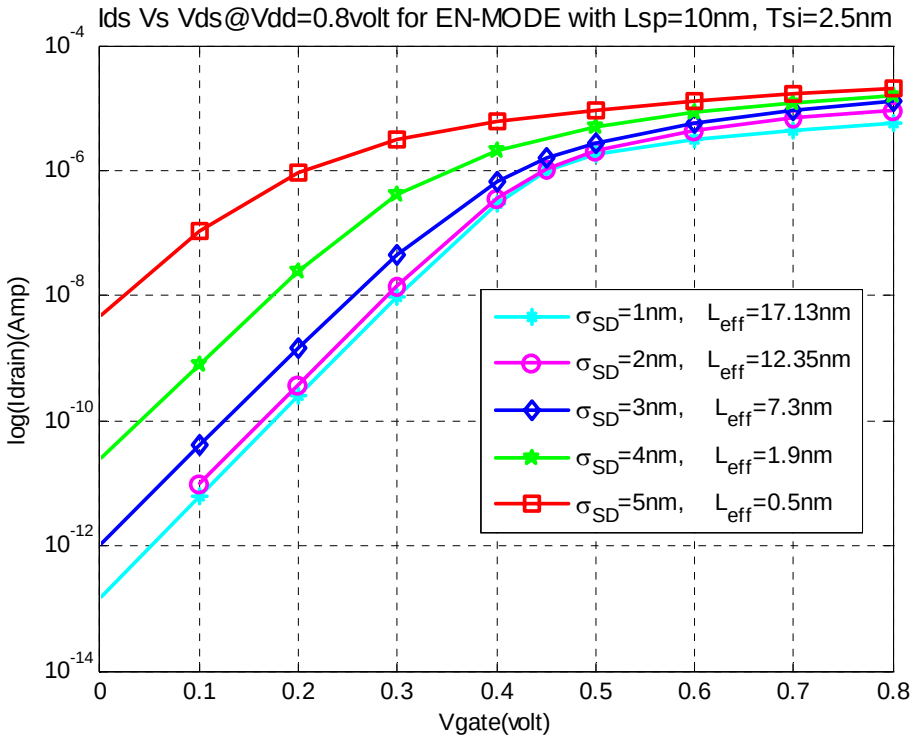

Figure 42. I_{ds} **vs** V_{gs} **for** $T_{si} = 2.5$**nm for ECM FinFET**

As the σ_{sd} increases, the gate voltage V_g means electrical field produced by the gate voltage starts losing control over the channel compared with the drain voltage. Referring to Table 13, in case of $\sigma_{sd} = 1$ and 2nm $L_{eff} > L_g$ and also in this case the gate voltage has more control over the channel compared with the drain voltage. When $\sigma_{sd} = 3$nm the gate voltage still has control over the channel but definitely the gate voltage, V_g, has less control over the channel compared with the plot of $\sigma_{sd} = 1$ and 2nm. In the case of $\sigma_{sd} = 4$ and 5nm, the subthreshold leakage is the worst as the drain voltage has full control over the channel compared with the gate voltage V_g also the channel is underlapped under the gate electrode. The best possible and practical value of σ_{sd} lies in between 2nm and 3nm. For $\sigma_{sd} = 1$nm the higher value of L_{eff} degrades the I_{on} state current i.e. device performance. While in case of $\sigma_{sd} = 4$nm and 5nm, the smaller value of L_{eff} compared with L_g has the worst subthreshold leakage current due to the higher short channel effect and tunneling current through the source to drain region.

4.5.4.3 Comparison. The difference in Figure 41 and 42 that L_{eff} is greater in case of ECM FinFET. Also the short channel effects are well controlled in both cases compared with the $T_{si} = 5.5, 4.5$ and 3.5nm for same value of L_{sp} and σ_{sd}.

Table 13. Tsi=2.5nm for ECM FinFET

σ_{sd}	$\mathbf{L}_{eff}$	**Comparison**
1nm	17.13nm	$L_{eff} > L_g$
2nm	12.35nm	$L_{eff} > L_g$
3nm	07.30nm	$L_{eff} > L_g$
4nm	01.90nm	$L_{eff} < L_g$
5nm	00.50nm	$L_{eff} < L_g$

4.6 Device Operations and Optimizations for ACM and ECM FinFET

In this section, ACM and ECM FinFET for 9nm gate length designs were optimized for maximum performance (I_{on} current which meets the ITRS specification for I_{off}) by adjusting the L_{sp} i.e. by and adjusting the separation between the heavily doped source/drain regions for the different T_{si}. The other parameters used in optimization for the $\sigma_{sd} = 3$nm/decade were chosen from previous simulations, as those are the best possible practical values that are achievable. For each value of L_{sp} the gate work function $\Phi_M = 4.45$eV is kept constant, and so is the threshold voltage $V_t = 0.4$V in order to keep a minimum low I_{off} current. Each T_{si} simulation (I_{ds} vs. V_{gs} plot) is repeated for varying values of L_{sp} from 5nm to 25nm. Furthermore, the only I_{on} current that meets the ITRS specifications for I_{off} current is plotted for each value of L_{sp} for ACM and ECM FinFET. The device parameters for optimization are selected in such a way that it provides the highest I_{on} current, while meeting the ITRS specification for I_{off} current. I_{on} vs. L_{sp} curves for ACM and ECM FinFET devices are shown in Figure 43 and Figure 44. The value of L_{sp} should be kept high enough so that $L_{eff} > L_g$ in order to avoid the short-channel effect and to maintain a high I_{on} current. As L_{sp} increases, L_{eff} also increases, which further reduces the short channel effect and allows for a lower value of V_t, as I_{on} current is proportional to (V_{dd}-V_t) with the lower value of V_t and allows an improved on-state current. Also, the value of L_{sp} is chosen such that $L_{sp} > L_g$ but L_{sp} should not be too large as compared to the gate length. As it will further increase the series resistance results in decreasing I_{on} current. On the other hand, if $L_{sp} < L_g$, the subthreshold leakage will be very high and the total power will be dominated by the static power.

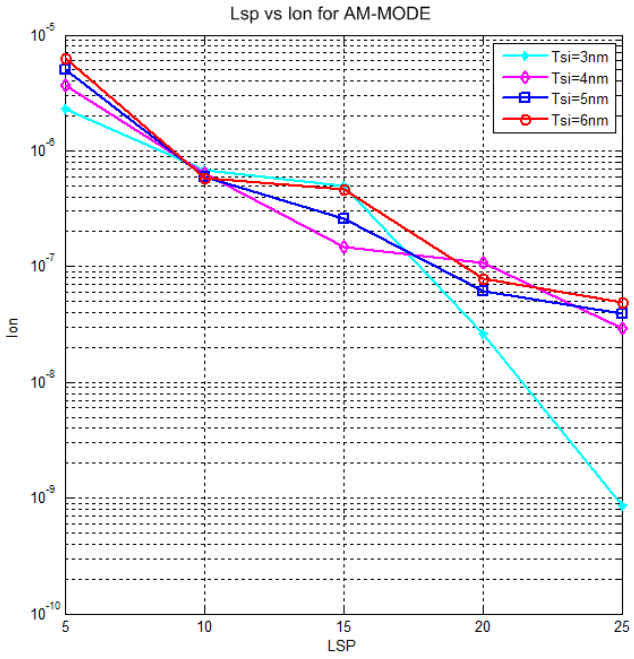

Figure 43. I_{on} vs L_{sp} for ACM FinFET where $I_{on}@I_{off}$=210nA/mm

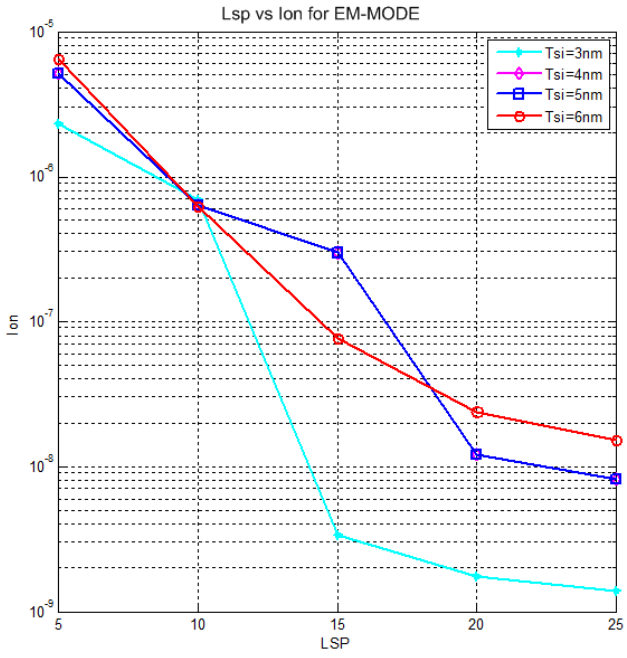

Figure 44. I_{on} vs L_{sp} for ECM FinFET where $I_{on}@I_{off}$=210nA/mm

4.6.1 Comparison. Referring to Figure 43 and Figure 44, for $L_{sp} < 5$nm the sub-threshold leakage current is very high for all the different thickness of silicon and it does not meet the ITRS specification for I_{off} current. However, when $L_{sp} = 5$nm in both ACM and ECM designs, it has the best performance and meets the ITRS specification for I_{off} current. In the case of silicon thickness ($T_{si} = 3$nm) has an advantage over higher thicknesses in terms of the short channel effect in both ACM and ECM FinFET devices. Also, T_{si} can not be too small as the thickness of silicon film is sensitive to device performance and short channel effect. So there is a trade off between the I_{off} current and the short channel effect. When L_{sp} is greater than gate length ($L_g = 9$nm), on-state current starts degrading in both ACM and ECM FinFET devices. In the case of the ACM FinFET ($L_{sp} = 15$nm), due to the same type heavy doping in the channel, the current does not fall off as fast as in the ECM FinFET ($L_{sp} = 10$nm) because the series resistance limits the performance.

The ACM device provides non p-n junction structure between source/drain and channel. It makes simple processing steps less technologically challenging compared with conventional MOSFET i.e. ECM device. Also, larger value of L_{eff} and lower value of V_t is possible in the case of ACM FinFET compared with ECM FinFET.

CHAPTER 5
CONCLUSIONS

It is amazing that CMOS device scaling has been continued so far with the use of embicated gate oxide insulator (silicon dioxide). The thickness of gate oxide will be left to only few atomic layers in the coming few years. In others words, planar bulk devices will be reaching material limitations and the further scaling of planar bulk CMOS technology will be very challenging and also to continue with the same performance rate 35% per technology node.

Among all the new inventive devices proposed below 22nm gate lengths, Double Gate MOSFET is one of the most promising CMOS devices because it has a better control over the channel i.e. submerged leakage paths. Also, the second way of eliminating deep submerged leakage paths is to provide lower junction capacitance, and the threshold voltage can then be set by work function of the gate electrode and two times more drive current. All these factors enhance the scalability of the Double Gate MOSFET compared with pervious counter parts Planar Bulk and Ultra-Thin-Body MOSFET. At this level or below 10nm gate length, processing of the Double-Gate MOSFET is very complex and challenging and it is one of the biggest road blocks along the fundamental device physics limitations. The background research and study is explained in the Chapter 2 and Chapter 3.

Today is the million dollar questions for IC industry how the scaling of CMOS device will continue in the future or below 22nm technology node? There are several multi-gate devices that have been introduced for below 22nm technology node length and for

future CMOS technology. The one named FinFET originated at the University of California Berkeley, with combined effort from three senior research Professor (Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor). As FinFET is the leading Double Gate MOSFET and its fabrication is compatible with existing CMOS technology. Also, the most unique quality of this device is the conducting channel wrapped around the silicon film called fin which forms the body of FinFET and distinguishes it from other devices. The dimension of the fin determines the effective channel width of the device. As the gate is wrapped around the channel in FinFET, it provides better control over the short channel effect than previous counterpart devices like the Ultra-Thin Body and Double Gate MOSFET. All this makes FinFET one of the potential CMOS devices for future scaling. But, as the processing of the Double-Gate MOSFET or by using conventional design is the biggest roadblock for scaling in below 10nm gate length.

In this work has shown that FinFET with the Accumulation Mode design can provide less technologically challenging processing steps compared with the conventionally designed (Enhance Mode device). Having the same type of dopant in the source/drain and the channel region eliminates one of the biggest technological challenges: the ultra-abruptness of the p-n junction associated with the conventional MOSFET i.e Enhance Mode devices. Also, it allows higher doping in the channel compared with conventional MOSFET to maintain a low channel resistance in the on-state. The ACM FinFET device provides a simple and easy processing technique with no ultra-abruptness p-n junction for nano-scale range or below sub-10nm gate length. This makes the ACM FinFET one of the

potential CMOS devices for scaling below 10nm gate length and will allow further scaling for the at least next few decades.

But in the case of the ACM device, due to heavy doping in the channel, the current does not fall off as fast as in the ECM device because the series resistance limits the performance. The only disadvantage of using the ACM device is that having the heavily doped same type doping in the channel as the source/drain will degrade the I_{on} current due to Columbic scattering, as compared to the ECM device.

BIBLIOGRAPHY

[1] The Nobel Prize in Physics 1956, [Online]. Available: *http://nobelprize.org/nobel_prizes /physics/laureates/1956/index.html*.

[2] B. Donlan and D. Pricer, "Pushing the Limits: Looking Forward...Looking Back," *Microelectronic Design*, vol. 1, 1987.

[3] A Science Odyssey: People and Discoveries: Transistor is Invented, [Online]. Available: *http://www.pbs.org/wgbh/aso/ databank/entries/dt47tr.html*.

[4] U.S. patent # 2,524,035, [Online]. Available: *http://www.jmargolin.com/history/2524035.pdf*, October 5, 1950.

[5] Semiconductor Milestones, [Online]. Available: *http://www.lucent.com/minds/trends/trends _v4n3/timeline.html*.

[6] MOSFET Technology Scaling, [Online]. Available: *http://inst.eecs.berkeley.edu*.

[7] I. M. Ross, "The Invention of the Transistor," *Processing of the IEEE*, vol. 86, no. 1, January 1998, pp. 7-28.

[8] S. Ma and W. Zukowski, "Transistor and Integrated Circuit: William Shokley (Inventor of Transistors)," [Online]. Available: *http://www.yrbe.edu.on.ca/~bayv/dpt3a/transistor.html*.

[9] C. Lécuyer, *Making Silicon Valley: Innovation and the Growth of High Tech, 1930-1970 (Inside Technology)*, The MIT Press, 1^{st} edition, 2005.

[10] T. R. Reid, *The Chip: How Two Americans Invented the Microchip and Launched a Revolution*, New York: Simon and Schuster, 1984.

[11] S. Augarten, *Bit by Bit - An Illustrated History of Computers*, Stated First Edition edition, Ticknor & Fields, New York, 1984.

[12] G. H. Stine, *The Untold Story of the Computer Revolution - Bits, Bytes, Bauds, and Brains*, Arbor House, New York, 1985.

[13] Integrated Circuits, 1958: Invention of the Integrated Circuit, [Online]. Available: *http:// www.pbs.org/transistor/background1/events/icinv.html*.

[14] K. Kahng and S. M. Sze, "A floating-gate and its application to memory devices," *IEEE Transactions on Electron Devices*, vol. 14 , issue 9, 1967, pp. 629-629.

[15] U.S.Patent # 3,356,858, [Online]. Available: *http://en.wikisource.org/wiki/ United_States*

_patent_3356858.

[16] International Technology Roadmap For Semiconductor, [Online]. Available: *http://www.itrs.net/home*.

[17] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, January 1998, pp. 82-85.

[18] M. Nathan, "Moore's Law Corollary: Pixel Power," *New York Times Online*, [Online]. Available: *http://www.nytimes.com/2006/06/07/technology/circuits/07essay.html*.

[19] J. Geelan,"Moore's Law: "We See No End in Sight," Says Intel's Pat Gelsinger," [Online]. Available: *http://java.sys-con.com/node/557154.*

[20] C. Disco, B. V. D. Meulen, *Getting new technologies together,* New York: Walter de Gruyter, 1998, pp. 206–207.

[21] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, A. Smith, K. Zawadzki, S. Thompson, M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," *IEEE International Electron Devices Meeting, 2003. IEDM '03 Technical Digest*, 2003, pp. 11.6.1-11.6.3.

[22] International Technology Roadmap 2008. [Online]. Available: *http://www.itrs.net/links/2008 ITRS/Home2008.htm.*

[23] K. Goto, Y. Tagawa, H. Ohta, H. Morioka, S. Pidin, Y. Momiyama, H. Kokura, S. Inagaki, N. Tamura, M. Hori, T. Mori, M. Kase, K. Hashimoto, M. Kojima, T. Sugii, "High performance 25 nm gate CMOSFETs for 65 nm node high speed MPUs," *IEEE International Electron Devices Meeting, 2003. IEDM '03 Technical Digest*, 2003 , pp. 27.1.1-27.1.4.

[24] W. Tsai, L. A. Ragnarsson, L. Pantisano, P. J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax, S. De Gendt, and M. Heyns, "Performace comparison of sub 1nm sputtered TiN/HfO_2nMOS and pMOSFETs," *IEDM Technical Digest*, 2004, pp. 311-314.

[25] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, V. De, "Parameter variations and impact on circuit and microarchitecture," *in Proceedings 2003 Design Autmations Confrence*, June 2-6, 2003, pp. 338-342.

[26] S. Nassif, "Delay variabilty : Source, impacts and treands," *in 2000 IEEE International Solid State Circuits Confrence Digest Of Tecchnical papers*, 2000, pp 368-369.

[27] C. Yu, Q. Huifang, R. Wang, P. Friedberg, A. Vladimirescu, and J. Rabaey, "Yield opti-

mization with energy-delay constraints in low-power digital circuits," *in IEEE Conference on Electron Devices and Solid-State Circuits,* 2003, pp. 285-288.

[28] S. Borkar, "Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation," *IEEE Micro*, vol. 25, no. 6, 2005, pp. 10-16.

[29] A. R. Brown, A. Asenov, and J. R. Watling, "Intrinsic fluctuations in sub 10-nm double-gate MOSFETs introduced by discreteness of charge and matter," *IEEE Transactions on Nanotechnology,* vol. 1 , 2002, pp. 195-200.

[30] J. O. Plouchart, K. Jonghae, B. J. Gross, W. Kun, R. Trzcinski, V. Karam, P. Hyde, R. Williams, N. Myung-Hee, J. Mc Cullen, and W. Clark, "SOI 90-nm ring oscillator sub-ps model-hardware correlation and parasitic-aware optimization leading to 1.94-ps switching delay," *IEEE International Electron Devices Meeting IEDM Technical Digest*, 2005, pp. 1033-1036.

[31] Y. Jie, E. Cohen, C. Tabery, N. Rodriguez, and M. Craig, "An up-stream design auto-fix flow for manufacturability enhancement," *IEEE Design Automation Conference*, 2006, pp. 73-76.

[32] Y. Taur, D. A Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, H.-S. Wong, "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, April 1997, pp. 486-504.

[33] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, M. V. Fischetti, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development,* vol. 50 , issue 4.5, 2006, pp. 339-361.

[34] P. M. Zeitzoff, J. A. Hutchby and H. R. Huff, "MOSFET and Front-End Process Integration: Scaling Trends, Challenges, and Potential Solutions Through The End of The Roadmap," *International Journal of High-Speed Electronics and Systems*, vol. 12, 2002, pp. 267-293.

[35] M. Bohr, ECS Meeting PV 2001-2, Spring, 2001.

[36] L. Chang, C. Yang-kyu, D. Ha, P. Ranade, X. Shiying, J. Bokor, H. Chenming, T. J. King, "Extremely scaled silicon nano-CMOS devices," *Proc. IEEE,* vol. 91, 2003[3], pp. 1860-1873.

[37] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS Spacer FinFET for the Terabit Era," *IEEE Electron Device Letters,* vol. 23, 2002, pp. 25-27.

[38] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron ere," *IEEE Electron Device Letters*, vol. 21, no. 5, May 2000, pp. 254-255.

[39] S. Tang , T.-J. King , J. Bokor , C. Hu, “Gate length scaling and threshold voltage control of double-gate MOSFETs,” *International Electron Devices Meeting Technical Digest*, 2000, pp. 719–722.

[40] S. Balasubramanian, L. Chang, B. Nikolic, T.-J. King, “Circuit-Performance implications for Double-gate MOSFET scaling below 25nm,” *Proceedings of the 2003 Silicon Nano-electronics Workshop*, Kyoto, Japan, June 8-9, 2003, pp. 16.

[41] J.-T. Park, and J.-P. Colinge, "Multiple-Gate SOI MOSFETs:Device Design Guidelines," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, December 2002, pp. 2222-2229.

[42] Multigate device, [Online]. Available: *http://en.wikipedia.org/wiki/Finfet.*

[43] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, J. Kedzierski, E. Anderson , H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J King, J. Bokor, C. Hu, "Sub 50-nm FinFET: PMOS," *International Electron Devices Meeting Technical Digest*, December 5–8, 1999, pp. 67.

[44] Taurus-Device User Guide, December 2003, Synopsys, Inc., [Online]. Available: *http://eceftp.niu.edu.tw/sycheng/td_X-2005.10_ug.pdf.*

[45] Contour Plot, [Online]. Available: *http://www.itl.nist.gov/div898/handbook/eda/section3/contour.htm.*

[46] Drain Induced Barrier Lowering, [Online]. Available: *http://en.wikipedia.org/wiki/Drain_Induced_Barrier_Lowering.*