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CMOS Rotary Traveling Wave Oscillators (RTWOs)

Marvin Aidoo

North Carolina A&T State University

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Department: Electrical and Computer Engineering

Major: Electrical Engineering

Major Professor: Dr. Numan S. Dogan

Greensboro, North Carolina

2014

The Graduate School
North Carolina Agricultural and Technical State University
This is to certify that the Doctoral Dissertation of

Marvin Aidoo

has met the dissertation requirements of
North Carolina Agricultural and Technical State University

Greensboro, North Carolina
2014

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2014

Biographical Sketch

Marvin Aidoo was born in Tema, Ghana, on July 13, 1984. He did his undergraduate studies in Computer Engineering at Kwame Nkrumah University of Science and Technology, Kumasi, Ghana, from 2003 to 2007. He joined the Department of Electrical and Computer Engineering at North Carolina Agricultural and Technical State University, Greensboro, North Carolina, in Fall 2008 for the Master of Science degree in Electrical Engineering which he completed in spring 2010. In Fall 2010, he enrolled in the Doctor of Philosophy (PhD) in the same department. He has been working in the RF Microelectronics Laboratory at North Carolina Agricultural and Technical State University under the supervision of Dr. Numan S. Dogan and Dr. Zhijian Xie. His research work involved design and implementation of CMOS Rotary Traveling Wave Oscillators (RTWOs).

Dedication

This is dedicated to my lovely wife, Sarah Fremah Aidoo and son, Daniel Andrew Aidoo.

Acknowledgements

I am extremely grateful to the Almighty God for bringing me thus far despite all the challenges. I would like to thank all the staff members of the Department of Electrical and Computer Engineering at North Carolina Agricultural and Technical State University (NC A&T SU), Greensboro, North Carolina, for their help and encouragement in pursuit of my graduate education. My keen appreciation is also extended to Dr. Numan S. Dogan, my advisor for giving me the opportunity to work on this project. Special thanks go to Dr. Zhijian Xie and Dr. Patrick Roblin for their invaluable contribution to the success of this research work as my co-advisors.

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Finally, I wish to acknowledge the support by the National Science Foundation. (Award ID: ECCS 1129053).

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Abstract

Rotary Traveling Wave Oscillator (RTWO) represents a transmission line based technology for multi-gigahertz multiple phase clock generation. RTWO is known for providing low jitter and low phase noise signals but the issue of high power consumption is a major drawback in its application. Direction of wave propagation is random and is determined by the least resistance path in the absence of an external direction control circuit. The objective of this research is to address some of the problems of RTWO design, including high power consumption, uncertainty of propagation direction and optimization of design variables. Included is the modeling of RTWO for sensitivity, phase noise and power analysis. Research objectives were met through design, simulation and implementation. Different designs of RTWO in terms of ring size and number of amplifier stages were implemented and tested. Design tools employed include Agilent ADS, Cadence EDA, SONNET and Altium PCB Designer. Test chip was fabricated using IBM 0.18 μm RF CMOS technology.

Performance measures of interest are tuning range, phase noise and power consumption. Agilent ADS and SONNET were used for electromagnetic modeling of transmission lines and electromagnetic field radiation. For each design, electromagnetic simulations were carried out followed by oscillation synthesis based on circuit simulation in Cadence Spectre. RTWO frequencies between 2 GHz and 12 GHz were measured based on the ring size of transmission lines. Simulated microstrip transmission line segments had a quality factor between 5.5 and 18. For the various designs, power consumption ranged from 20 mW to 120 mW. Measured phase noise ranged between -123 dBc/Hz and -87 dBc/Hz at 1 MHz offset.

Development also included the design of a wide band buffer and a printed circuit board with high signal integrity for accurate measurement of oscillation frequency and other

performance measures. Simulated performance, schematics and measurement results are presented.

CHAPTER 1

Introduction

1.1 Background

The current wireless spectrum in most radio frequency and signal processing applications is focused around 900 MHz to 6 GHz. For example, Wireless Local Area Networks (WLAN) are, 5.4 GHz to 5.9 GHz; Bluetooth is 2.4 GHz and Mobile Television is between 450 MHz and 750 MHz. Producing the power needed for analog and digital systems' applications requires two main types of electronic oscillators that produces repetitive electronic signals: the harmonic oscillator and the relaxation oscillator, in the form of timing signals. The harmonic oscillator produces a sinusoidal output, whereas the relaxation oscillator is often used to produce a non-sinusoidal output, such as a square wave or sawtooth.

Advances in the design of electronic oscillators have resulted into varied forms of design implementations. The most conventional design is comprised of an inductor-capacitor (LC) resonant tank with a negative resistance compensating amplifier circuit. The approach used in this work produces multiple-phase signals and falls into a class of oscillators that utilizes the distributed LC nature of a transmission line. The emergence of this new technology called the Rotary Travelling Wave Oscillator (RTWO), has witnessed designs in different frequencies as low as 925 MHz to about 50 GHz. This underscores the potential of RTWO for UHF to Terahertz applications.

John Wood, who first proposed the concept of RTWO, was successful at presenting experimental results of a 0.25 μm CMOS test chip with 950-MHz and 3.4-GHz rings indicating 5.5-ps jitter and 34-dB power supply rejection ratio (PSRR) [1]. G. Le Grand de Mercey of University of Bundeswehr did a similar design resulting in an 18 GHz operating frequency with

a phase noise power spectral density of -117 dBc/Hz at a 1-MHz offset from the carrier using TSMC 0.13μm CMOS process [2]. A review of recent developments in Standing Wave Oscillator designs presented by William Andress and Donhee Ham [3] as well as other researchers attest to the fact that Wave-based Oscillators strongly fulfill certain design criteria, including high-frequency operation and low-skew low-jitter clock distribution.

1.2 Research Objectives

Successful design of RTWO to meet optimal performance measures involves simultaneous consideration of all the design variables. Important considerations for oscillators in RF and microwave systems include frequency tuning range, power and phase noise. A behavioral model helps to make predictions about the system performance. RTWO design is a multi-parameter, multi-objective problem. Analytical modeling is important for understanding of the working principles and obtaining optimal solutions for the parameters.

RTWO finds its application mostly in synchronous and timing circuits. The stringent performance requirements imply accurate poly-phase signal generation. RTWO is an ideal solution as multiple phases of signals are easily available by tapping different positions on the transmission line.

Due to the topologically symmetric nature of the RTWO, the wave rotary direction has been attributed to uncontrollable factors such as initial symmetric breaking and least resistance path [1-4]. Direction control is necessary as spurious signals propagating in reverse direction potentially degrade phase noise. One drawback of RTWO wireless and microwave application is its high power consumption. The growing demand for performance in terms of low power consumption highlights the need to reduce the power consumption of conventional RTWO.

The main purpose of this research is to design, implement and characterize novel RTWOs in IBM 0.18μm RF CMOS technology. Specifically, the objectives of this research are;

- Analytical modeling of RTWO for sensitivity, phase noise and power optimization
- Design and implementation of direction control technique of oscillation of RTWO
- Design and implementation of a novel low power RTWO

1.3 Organization of the Dissertation

The dissertation is divided into five chapters. Chapter 1 introduces the research topic and objectives. Chapter 2 presents literature review of RTWO. Chapter 3 discusses design optimization and sensitivity analysis. Design and implementation of RTWO in CMOS technology is covered in Chapter 4. Chapter 5 discusses measurement results. Chapter 6 provides conclusions and suggests future directions.

CHAPTER 2

RTWO Design Review

This chapter presents literature review of RTWO and conceptual basis of oscillation in these structures. Beginning with a general study of oscillator theory, the rotary traveling wave oscillator (RTWO) is introduced.

2.1 Oscillator Theory

Almost all radio equipment built contains at least one oscillator. It may be a simple crystal controlled circuit, a tuned inductor-capacitor (LC) variable frequency oscillator, or even a direct-signal synthesizer. Radio frequency (RF) oscillators share a fundamental design concept made up of an amplifier whose output is feedback through a frequency selective system. Oscillators may be classified in a number of ways. For example, the circuit can be categorized by the devices used for the active element and the resonator, such as the bipolar transistor, crystal controlled oscillator, and the JFET LC oscillator. Oscillators can be categorized according to a historic circuit form, such as Colpitts or Hartley. Additionally, oscillators can be classified by the active device configuration, such as common-emitter. Finally, they can be classified according to the method used during design, such as negative resistance oscillators. Most recently, they can be classified by the propagation of signal such as Rotary Travelling Wave Oscillator (RTWOs). Beyond their practical importance, oscillators are highly complex circuits that include both positive feedback, which causes oscillation to start at the desired frequency, and device nonlinearity that maintains operating amplitude constant with time. An oscillator produces a periodic output, usually in the form of voltage by converting DC power to AC waveform. As such, the circuit has no input while sustaining the output indefinitely. For

oscillation to occur, the circuit or system must satisfy the Barkhausen's criteria for oscillation. A two port linear feedback model of the oscillator is shown in Figure 2.1.

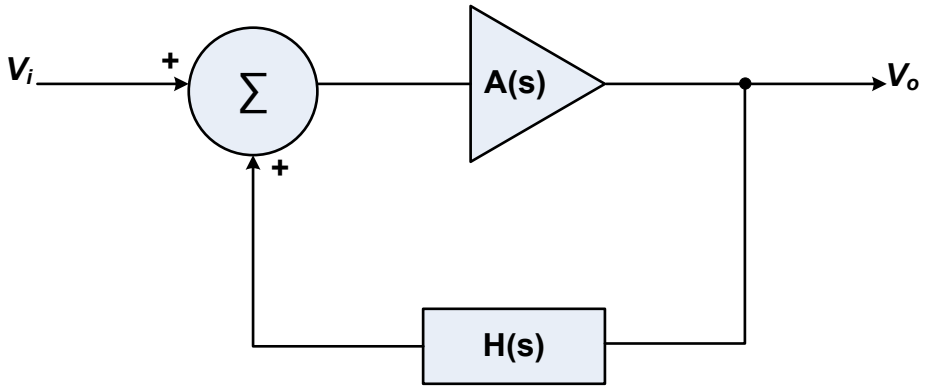


Figure 2.1. Two port linear feedback model of oscillator

Most RF oscillators produce sinusoidal outputs, which minimizes undesired harmonics and noise sidebands. As shown in Figure 2.1, an amplifier with a transfer function *A(s)* has an output voltage *Vo*. This voltage passes through a feedback network with a frequency dependent transfer function *H(s)*, and is added to the input *Vi* of the circuit. The output voltage (V_o) in terms of the input voltage (V_i) is given by:

$$V_o(\omega) = \frac{A(\omega)}{1 - A(\omega)H(\omega)} V_i(\omega) \qquad (2.1)$$

If the denominator becomes zero, the closed loop gain of the circuit approaches infinity. The circuit amplifies its own noise components at ω_o indefinitely making it possible to achieve a non-zero output voltage from a zero input voltage, thus forming an oscillator.

2.2 Conceptual Basis of Rotary Traveling Wave Oscillator (RTWO)

Rotary Traveling Wave Oscillator (RTWO) was first introduced as a new transmission line approach for gigahertz-rate clock generation [1]. The basic RTWO architecture is a mobius-ring-like transmission line with cross-coupled inverter pairs distributed along its path as shown in Figure 2.2.

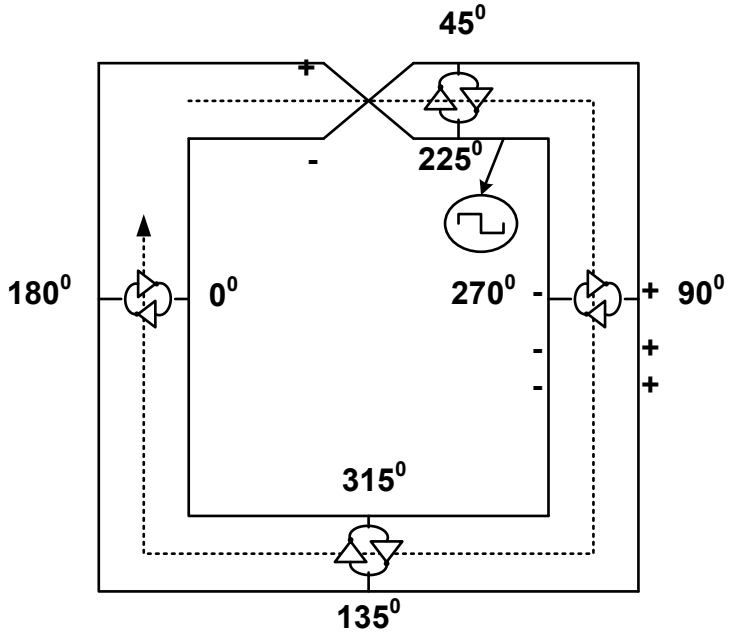


Figure 2.2. RTWO circuit topology

The coupled transmission line operates in the odd mode regime imposed by a gain stage typically consisting of cross-coupled inverter pairs (CCIPs) with the voltages on the same positions having 180^o phase difference. In addition to imposing the odd mode operations for the differential line, CCIP sustains the oscillation and replenishing the energy loss in the transmission line. Compared with LC tank oscillators and other wave-based oscillators, RTWO is not susceptible to mismatches due to its unique crossover reverse feedback segments. Once enough gain is provided, there is no latch-up danger for this design technique; since it utilizes a single-line DC-coupled closed loop structure. Performance of RTWO is compatible with other designs including low power consumption, phase noise, and accurate frequency tuning range.

The reverse feedback imposes a signal inversion after one round delay (τ), so that oscillations between the two polarization states of the line occur with a period of $T = 2\tau$. There are various ways of analyzing the working principle of RTWO. Based on a recent work by Koji et al, RTWO can be viewed as a superposition of multiple quarter wave length (λ/4) Standing

Wave Oscillators [5] for phase noise analysis. The operating principle of the circuit is also quite similar to two distributed voltage controlled oscillators (DVCOs) cross-coupled to each other. Another proposed description of RTWO is a cascade of iterative two-port networks as long as the cutoff frequency of each continuous transmission line is significantly higher compared to the oscillation frequency. Gain stage or CCIP will be used interchangeably throughout this work.

2.3 RTWO – Filter Stage

2.3.1 Theory of Transmission lines. Transmission lines can generally be classified as distributed resonant filters due to the presence of inductive (L) and capacitive (C) components. For one to observe the transmission line effects, wire inductance has to dominate the delay behavior relative to wire resistance. The transmission line has the prime property that a signal propagates over the interconnection medium as a wave. In the wave mode, a signal propagates by alternatively transferring energy from the electric to the magnetic fields, or equivalently from the capacitive to inductive modes. Accounting for losses in the conductors and dielectric material, transmission lines can be modeled as distributed RLCG electrical model shown in Figure 2.3.

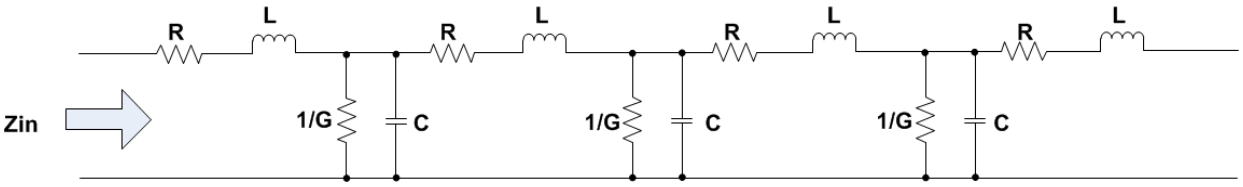


Figure 2.3. Lossy single transmission line electrical model

Many planar transmission line structures have been conceived and variants are still being developed. Each structure comprises a combination of metal lines and dielectric layers. The dielectric can be a single material or combination of more than one, each with its

permittivity (ε). The choice of structure depends upon several factors including the type of circuit or sub-system and its operating frequency. Information in a signal is contained in the electromagnetic wave and when the electric and magnetic fields are in the plane perpendicular to the direction of travel the fields are said to be Transverse Electromagnetic (TEM). If they are nearly confined to the transverse plane then they are called quasi-TEM modes. Figure 2.4 shows the circuit model of section (Δz) of transmission line.

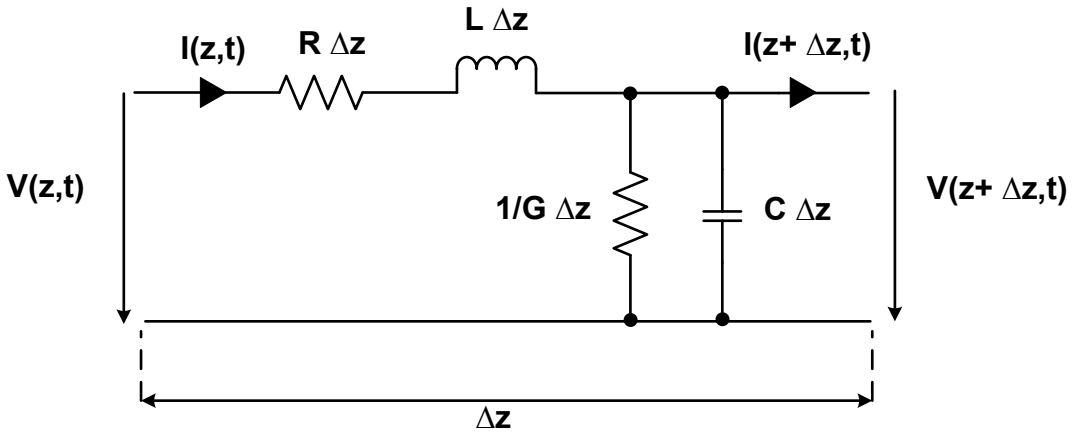


Figure 2.4. Equivalent circuit model of a length Δz of a transmission line

2.3.2 Transmission line equations. The relevant parameters of a transmission line can be obtained by solving the telegrapher's equations in time domain. In sinusoidal steady state condition where the transients are no longer important, the equations in frequency domain simplify to:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.2}$$

$$\frac{dV(z)}{dz} = -(G + j\omega C)V(z) \tag{2.3}$$

where *z* is the direction of wave propagation. The elements *L, R, C and G* are *per unit length* quantities. The inductance (L) models the energy stored in the magnetic field, while the series resistance accounts for losses in the signal line. The shunt capacitance models the energy stored

in the electric field whereas the shunt conductance models the losses due to dielectric material and ohmic leakage. The two equations solved simultaneously yielding wave equations for current and voltage are expressed as:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.4}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.5}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$ is the complex propagation constant, α and β are the attenuation constant (Np/m) and phase constant (rad/m) of the line respectively. Equations 2.2 and 2.3 result in traveling wave solutions given by:

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{2.6}$$

$$I(z) = I_o^+ e^{-\gamma z} + I_o^- e^{\gamma z} \tag{2.7}$$

where $e^{-\gamma z}$ and $e^{\gamma z}$ represent wave propagations in the positive and negative directions in the z plane. V_o^+ and V_o^- represent amplitudes of forward and backward waves at the start of propagation which then varies exponentially. Equation 2.6 can be written as:

$$I(z) = \frac{1}{Z_0}(V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z}) \tag{2.8}$$

where Z_0 is the characteristic impedance of the transmission line given by:

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.9}$$

For design purposes, three cases of propagation are considered for analysis and approximate derivation of design equations namely lossless, low loss, and lossy.

In the lossless limit, $R=G=0$, the propagation constant parameters α and β are given by $\alpha = 0, \beta = \omega\sqrt{LC}$. The phase velocity ($V_p$) is given by:

$$V_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \tag{2.10}$$

The characteristic impedance is given by:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.11}$$

In the low loss limit, $R<<\omega L$ *and* $G<<\omega C$, the propagation constant parameters α and β are given by [6]:

$$\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} + \frac{G}{2}\sqrt{\frac{L}{C}} \approx \frac{R}{2Z_0} + \frac{GZ_0}{2} \tag{2.12}$$

$$\beta = \omega\sqrt{LC}$$

In the lossy limit, α and β are given by [6]:

$$\alpha = \sqrt{\frac{1}{2}[\sqrt{\omega^4(LC)^2 + \omega^2[(LG)^2 + (RC)^2] + (RG)^2} + (RG - \omega^2 LC)]} \tag{2.13}$$

$$\beta = \sqrt{\frac{1}{2}[\sqrt{\omega^4(LC)^2 + \omega^2[(LG)^2 + (RC)^2] + (RG)^2} - (RG - \omega^2 LC)]} \tag{2.14}$$

2.3.3 RTWO travelling wave equation. The energy injected at any point by the amplifier into the Mobius ring will typically split equally and will travel symmetrically along the ring in both forward and backward direction .The direction of wave propagation once oscillation is initiated is guided whether forward and backwards. Assuming the waves are travelling clockwise (forward), such waves are amplified whereas any backward travelling waves are attenuation. In simplistic terms, the initial current that is driven by thermal voltage always takes the path of least resistance and this dictates the initial direction of propagation though this direction can be interrupted and controlled. After oscillation is sustained by a combination of positive feedback and Barkhausen criteria, self-locking directivity of travel is

maintained by the non-linear latching action of the amplifiers. A latched state is level sensitive. An attempt by the backward energy to cause a further switching into a new state will be resisted due to self-locking directivity of the amplifiers. Perfect symmetry of RTWO is not possible due to layout mismatch. In a practical RTWO structure, the voltage and current of backward traveling waves are of small amplitude compared to the forward traveling waves. We will discuss the effect of the ON resistance of the amplifiers on these waves and its role in maintaining established direction in chapter 3. Least resistance path, ON resistance, and directivity of non-linear latching actions all combine to define the direction of propagation. It is desirable to operate RTWO in the strongly nonlinear region due to the possibility of backward wave propagation. The weakly nonlinear region which represents the transition between the linear and saturated regions promotes backward wave propagation. To do this one needs to pay attention to the sizing of the active devices. Backward waves cause the perturbation of fundamental travelling wave which degrade phase noise. Equation 2.6 can be rewritten as:

$$V(z) = (V_o^+ - V_o^-)e^{-\gamma z} + V_o^-(e^{\gamma z} + e^{-\gamma z}) \tag{2.15}$$

For a forward wave dominated mode of operation, equation 2.15 simplifies to:

$$V(z) = V_o^+ e^{-\gamma z} \tag{2.16}$$

where $V_o^- \approx 0$. Small signal analysis to determine startup condition will be based on this simplification.

2.3.4 Transmission line design parameters. Microstrip line, coplanar waveguide, coplanar stripline and differential coplanar waveguide are some of the most common transmission line structures for propagating electromagnetic wave from one point to the other. Figure 2.5 shows the 2-D models of these structures.

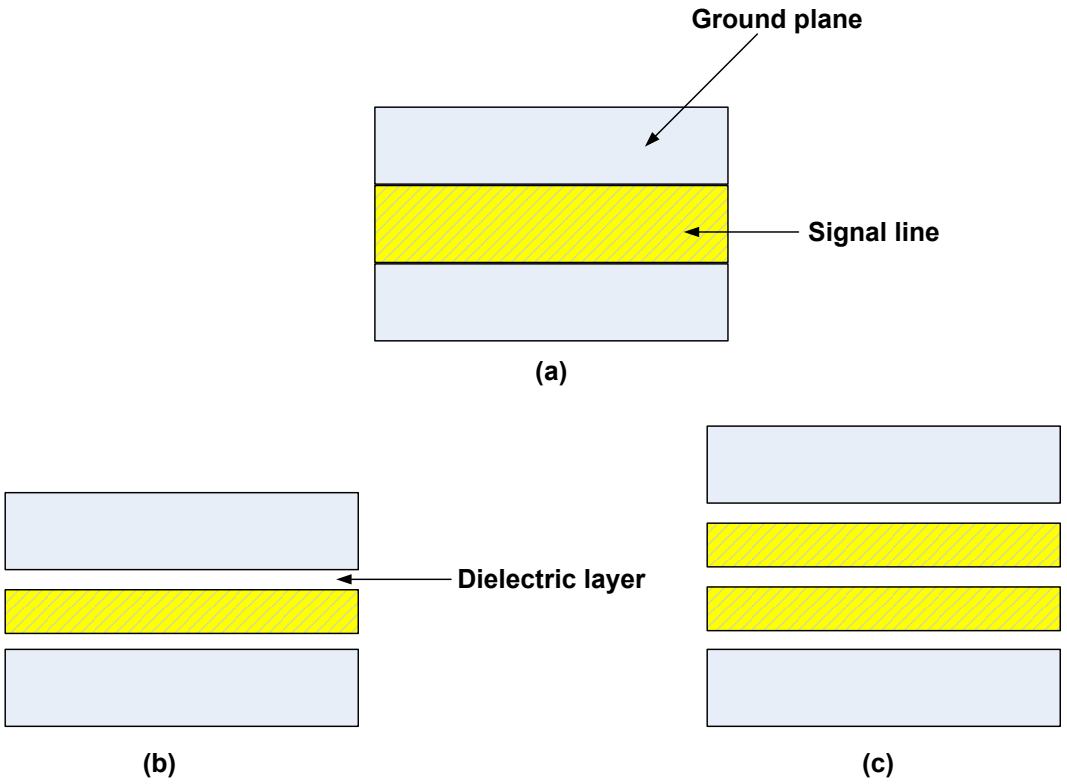


Figure 2.5. (a) Microstrip line; (b) Coplanar Stripline; (c) Differential Coplanar Waveguide

The common structures used for RTWO distributed filter is either the differential coupled microstrip line or the differential coupled coplanar waveguide. Differential propagation involves two conductors placed a distance away from each other. The physical parameters of interest to an RTWO designer include width, spacing, metal layer thickness, effective dielectric, and distance from the reference plane. The metal layer thickness, the effective dielectric constant are process dependence, leaving the designer with the width and spacing to vary to optimize for the desired performance.

The selection of width and spacing determines the RLGC parameters of the line which affects the propagation constant (γ), characteristic impedance (Z_0) and quality factor (Q). Small spacing between lines creates low inductance because of the high flux cancellation in the tight loop. Capacitance (C) is a function of signal spacing to the return path. Small spacing creates a

large capacitance value. In RTWO design, Z_0 is an important parameter which affects the oscillation conditions, the resulting wave form and the phase noise. The Q-factor affects the phase noise and γ affects the oscillation condition. The latching characteristics of the cross coupled inverter forces the RTWO to operate in the differential or odd mode. The fast wave (even) mode is undesirable since it leads to power dissipation. Assuming negligible losses, Z_0 in slow wave or odd mode can be expressed as [7]:

$$Z_{0-diff} = \sqrt{\frac{L_0}{C_0}} \tag{2.17}$$

where differential inductance $(L_0) = L_s\text{-}M$ and differential capacitance $(C_0) = C_s+2Cc$. *Ls* and *M* are self and mutual inductance respectively. C_s and C_c are the self and coupling capacitance respectively. All parameters for calculating Z_0 are in per-unit-length. The per-unit-length differential inductance (L_0) taking into account mutual inductance can be calculated using expression in [8] given as:

$$L_0 = \left(\frac{\mu_0}{\pi}\right) log\left\{\left(\frac{\pi . s}{w+t}\right)+1\right\} \tag{2.18}$$

where *s* is the spacing between the conductors, *w* is the width of the conductor and *t* is the thickness of the conductor.

The coupling capacitance (C_c) can be computed using [9]:

$$C_c = \epsilon_0\epsilon_r\left(0.03.\left(\frac{w}{h}\right)+0.83.\left(\frac{t}{h}\right)-0.07.\left(\frac{t}{h}\right)^{0.222}\right).\left(\frac{s}{h}\right)^{1.34} \tag{2.19}$$

where *h* is the effective dielectric height.

Self-capacitance (C_s) and inductance (L_s) can be computed as:

$$C_s = \frac{1}{Z_0 . V_p} \tag{2.20}$$

$$L_s = Z_0^2 . C_s \tag{2.21}$$

where V_p is the phase velocity. The resistance of the line can be accounted for as DC resistance (R_{dc}) at low frequencies or AC resistance (R_{ac}) at high frequency typical called skin resistance. The effective resistance is the average of the two resistances. At low frequencies, the current flowing through a conductor spreads out evenly and DC losses per unit length is determined by the cross sectional area and the resistivity of the material. As frequency increases, the current migrates towards the periphery of the conductor typically known as the "skin effect". Skin effect creates a skin depth (δ) as shown in Figure 2.6.

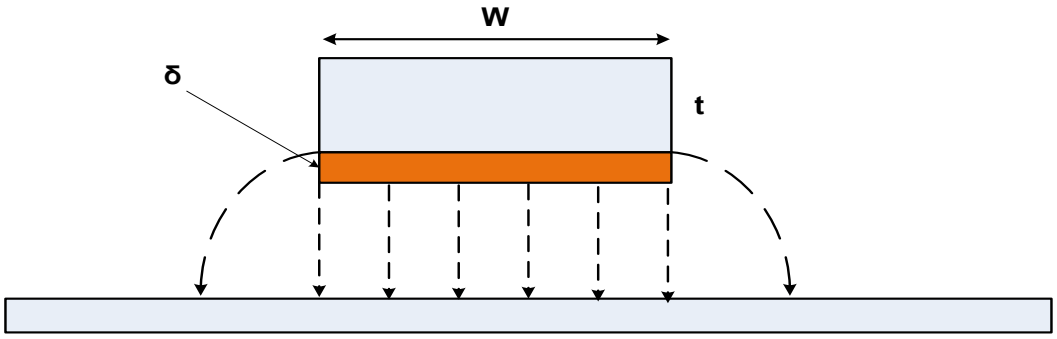


Figure 2.6. Microstrip line with annotated skin depth

The skin effect creates a depth of resistive region where current is concentrated and this causes resistance to increase above the nominal DC resistance. At high frequencies, AC resistance becomes significant and is approximated as:

$$R_{ac} = \frac{\rho L}{\delta \times W} = \frac{\rho L}{W . \sqrt{\frac{\rho}{\pi \mu f}}} \tag{2.22}$$

where δ is the skin depth thickness, μ is magnetic permeability of the conductor, L is the conductor length, w is the conductor width, f is the signal frequency, and ρ is the resistivity of the conductor.

2.3.5 Transmission line modeling – Extracting RLGC. The schematic entry and simulation of RTWO requires precise extraction of RLGC parameters of the transmission line section and additional parasitic capacitances from the amplifier stage. Extraction of transmission line parameters is done typically at the highest possible frequency of operation. Extraction helps the designer to perform transient, periodic steady state, and sensitivity analysis. The top metal layer of a process metal stack is mostly used to fabricate the differential lines because of the reduced sheet resistance and thicker dielectric layer over the substrate. The first step in the extraction process involves the measurement of the s-parameters and conversion to RLGC. Conversion can either be by curve fitting or approximate mathematical formulas. Approximate mathematical formulas can be found in the works by Degerstrom et al [10] and Sampath, M.K [11]. In chapter 4 the results of extraction using curve fitting will be presented.

2.4 RTWO – Amplifier Stage

The amplifier or gain stage in most RTWO topologies and LC oscillators is realized by connecting two inverters back-to-back. Without a current source, RTWO operates in the voltage-limited regime and the amplitude of the filter tank is limited by the voltage supply. Even though this topology benefits from the omission of additional noise from the current source, the power supply has to be kept stable to avoid frequency pushing and perturbation noise injection. With a current source bias, the amplitude of the filter tank is estimated as:

$$V_{filtank} = \frac{I_{bias}}{g_{line}} \tag{2.23}$$

where g_{line} is the conductance of the distributed filter (transmission line) and I_{bias} is current that sets the operating point of the oscillator. Another implementation of the amplifier involves all NMOS transistors. All NMOS CCIP is ideal for high frequency operation of RTWO. Figure 2.7 shows the schematic of the cross-coupled inverter pair.

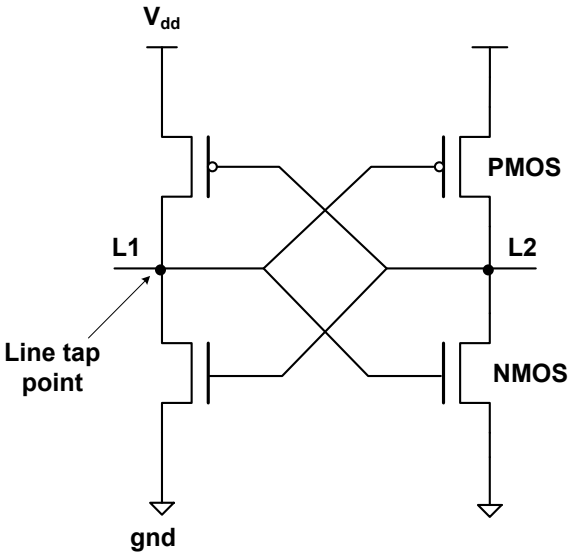


Figure 2.7. Complementary cross-coupled inverter without current source

2.4.1 Qualitative model of CCIP. In order to derive the qualitative model we first plot the response of CCIP to a differential input signal. The response is a plot of current versus voltage. The plot identifies the various regions of operation and helps us validate the CCIP as a negative resistance element for a range of voltage inputs. Figure 2.8 is test circuit for such analysis.

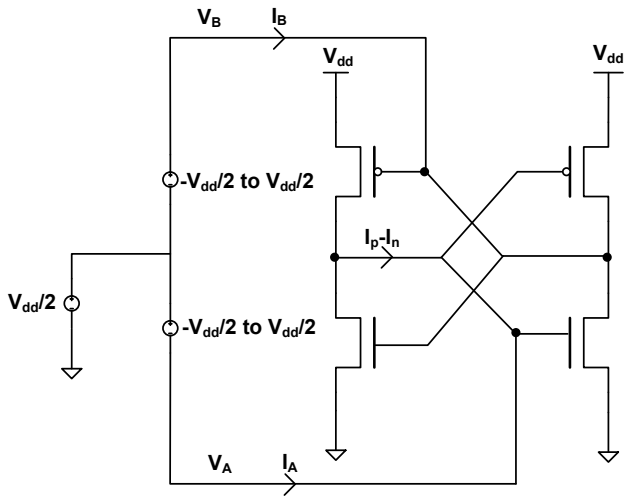


Figure 2.8. Differential response test circuit

Figure 2.9 shows the current versus voltage as a sinusoid with two ohmic and one gain regions of operation.

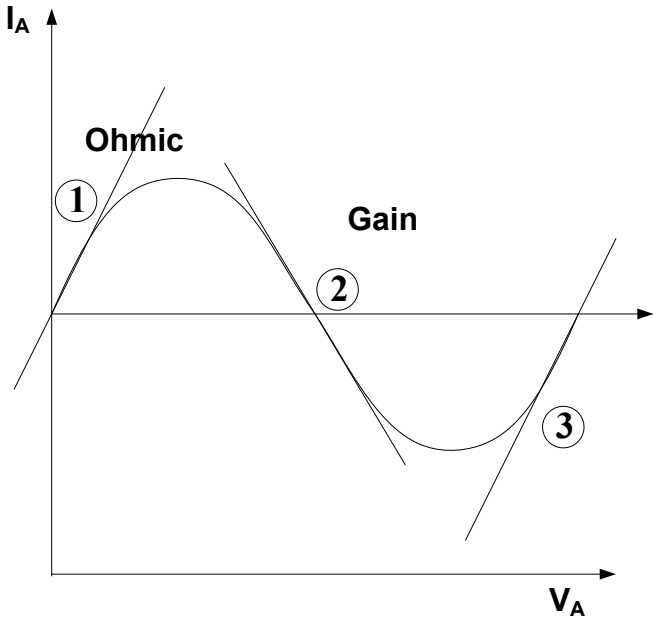


Figure 2.9. Plot of current versus differential voltage

For a symmetric case, the line current through the CCIP can be approximated as:

$$I = -g_m \times \frac{V_{dd}}{2} \times sin\left[\pi \times \frac{\Delta V}{V_{dd}/2}\right] \tag{2.24}$$

where g_m is the differential transconductance, V_{dd} is the supply voltage and ΔV is the incremental voltage where the line voltage switches from a low voltage level to a high voltage level. From equation 2.24:

$I=0$ for $\Delta V=0, V_{dd}/2, -V_{dd}/2$

$I<0$ for $\Delta V>0$

$I>0$ for $\Delta V<0$

The maximum differential negative resistance ($-1/g_m$) is determined when $\Delta V \rightarrow 0$ and $\Delta I \rightarrow 0$ taking into account transient effects. For quantitative analysis, the asymmetry of CCIP and transmission line has to be included.

2.5 Integrated Amplifier and Filter Stages

A negative resistance model of an oscillator is a one port model as shown in Figure 2.10.

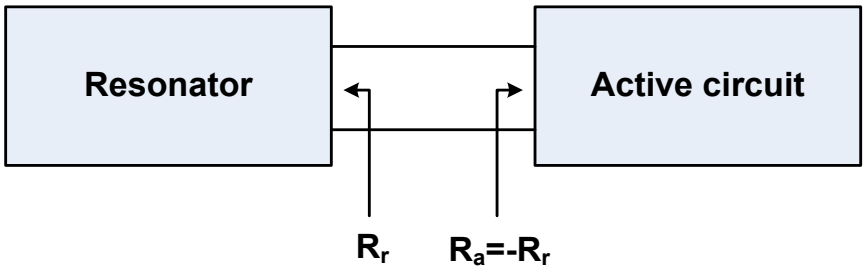


Figure 2.10. One port negative resistance model

The negative resistance of the active circuit compensates for the energy lost from the passive resonator network in every cycle of oscillation. Even if Barkhausen criteria stipulates equal absolute values of resistance, the *–Ra* is practically chosen to be more negative to ensure good start-up and amplitude stability conditions.

2.5.1 Oscillation startup condition. Oscillation typically starts with the pole placement in the right hand side (RHS) of the S-plane (open loop gain >1) and approaches marginal stability at the pole placement on the imaginary axis (open loop gain =1). With marginal stability the closed loop gain is infinite, a necessary condition to sustain oscillation with negligible perturbation in the oscillation amplitude. The small signal model for oscillation startup analysis is shown in Figure 2.11.

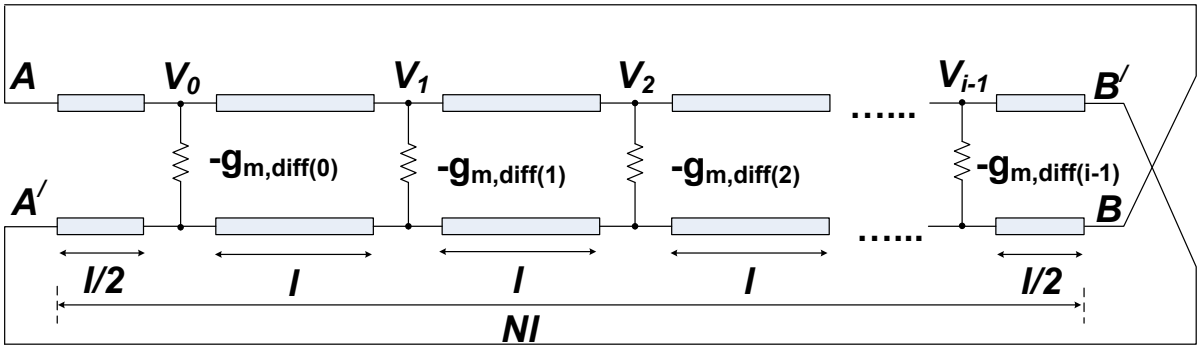


Figure 2.11. Small signal equivalent circuit

In order to determine the startup condition for RTWO, we first construct a small signal model shown in Figure 2.11. Assuming an injected signal at node A, the open loop gain after reverser feedback is computed by observing the signal at node B. The equivalent impedance seen by the *–Gm* cell at the point of current injection is given by $Z_0/2$. As the injected signal propagates along the line, it experiences repeated attenuated and amplification. It must be noted that the periodic loading by the active devices breaks the circuit into cascades of coupled two port networks. The total transconductance (g_m) is an integral sum of the individual g_m per section. The voltage gain that an incoming signal sees at each loading node is given by:

$$A_v = \frac{1}{2} g_m Z_0 \tag{2.25}$$

where Z_0 is the characteristic impedance of the line which is constant irrespective of the number of sections. The low frequency round trip total open loop gain of the oscillator without considering inherent losses is given by:

$$A_v = \frac{N}{2} g_m Z_0 \tag{2.26}$$

where N is the number of sections

The voltages at the loading nodes of the amplifier stages can be expressed as:

$$V_i = V_{i-1} \times \left(\frac{1}{2} g_m Z_0\right) \times \exp(-\gamma l) \tag{2.27}$$

where *l* is the section length. The observed signal at node B is given by:

$$V_B = -V_B{}' = -V_A \left(\frac{1}{2} g_m Z_0\right)^N \times \exp(-N\gamma l) \tag{2.28}$$

where *N* is the number of sections. The open loop gain is defined as:

$$H(s) = \frac{V_B}{V_A} = -\left(\frac{1}{2} g_m Z_0\right)^N \times \exp(-N\gamma l) \tag{2.29}$$

From equation 2.29, Barkhausen criteria is satisfied for the case of positive feedback if:

$$-\left(\left(\frac{1}{2} g_m Z_0\right) \times \exp(-\gamma l)\right)^N \leq 1 \tag{2.30}$$

$$\left(\left(\frac{1}{2} g_m Z_0\right) \times \exp(-\gamma l)\right)^N \geq 1 \tag{2.31}$$

$$\left(\frac{1}{2} g_m Z_0\right) \times \exp(-(\alpha l + j\beta l)) \geq 1 \tag{2.32}$$

The imaginary part accounts for phase synchronization and must be ignored. Equation 2.32 can be reduced to:

$$\left(\frac{1}{2} g_m Z_0\right) \times \exp(-\alpha l) \geq 1 \tag{2.33}$$

where the electrical length (βl) is given by:

$$\beta l = \frac{n\pi}{N} \tag{2.34}$$

where n is an arbitrary odd integer. For four sections (N=4) and a fundamental mode of oscillation, the electrical length is 45^0. The transconductance (g_m) required for oscillator is given by:

$$g_m \geq \frac{2}{Z_0} \exp(\alpha l) \tag{2.35}$$

2.5.2 Frequency and amplitude estimation. Unlike the transmission line with infinite bandwidth, the RTWO is bandwidth limited with the highest possible frequency determined by the cutoff frequency of the equivalent lump section of the line. A lump section model typically consists of passive parasitics (RLGC) from the line, amplifier stage and loading elements as shown in Figure 2.12.

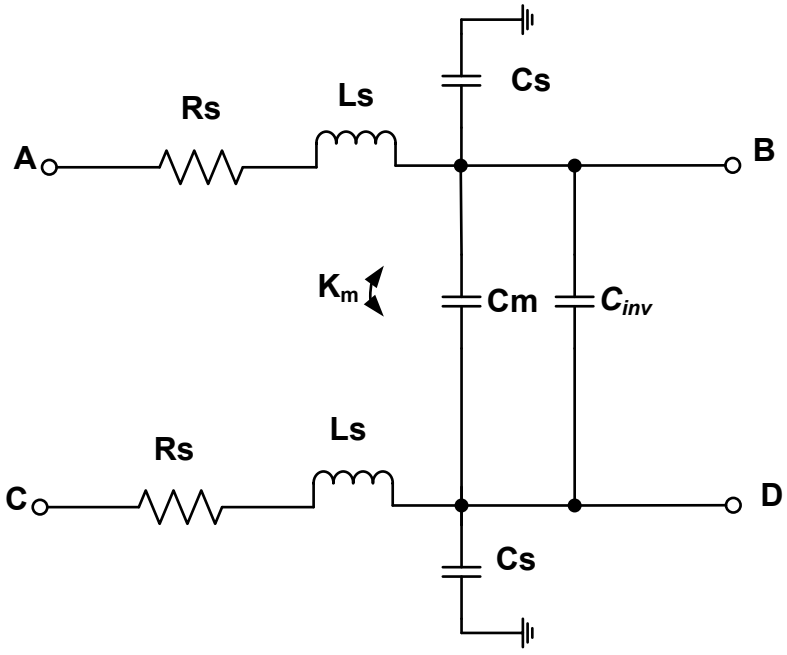


Figure 2.12. RF macro-model of one segment

Ignoring any other loading elements, the RF macro model is used to determine the design parameters namely characteristic impedance (Z_0), phase velocity, time delay, cutoff frequency and oscillation frequency. The C_{inv} represents the capacitive parasitics from the CCIP. K_m represents the inductive coupling coefficient between the two lines. The input impedance of an unloaded transmission line is high at the fundamental frequency and its harmonics owing to the infinite bandwidth. Thus a square wave injected into the line will produce a near square wave. Loading the line periodically reduces the fractional bandwidth for a given frequency of input signal and waveform. Another way to determine the waveform of

RTWO is to compare the relative speed of CCIP to the transmission line. For a faster CCIP, the state of marginal stability is characterized by a sudden change or relaxation between the ground potential and supply voltage. Oscillator amplitude either saturates (or cutoff) and stay that way for some time (pulse width) depending on the frequency before it becomes linear and heads for the opposite power rail. A faster gain stage will generally produce non-sinusoidal or quasi-square waves due to bandwidth limitation. The sinusoidal waveform is obtained for the case slower CCIP and faster line. The oscillation frequency is typically found by extracting the total inductance and capacitance and is given by:

$$f_{osc} = \frac{1}{2\sqrt{L_T C_T}} \tag{2.36}$$

where L_T and C_T are the total inductance and capacitance respectively.

Alternatively, the oscillation frequency can be expressed in terms of the phase velocity and the single round travel length as:

$$f_{osc} = \frac{V_p}{2l} \tag{2.37}$$

$$f_{osc} = \frac{1}{2l\sqrt{L_0 C_0}} \tag{2.38}$$

where l is the ring length for half cycle. L_0 and C_0 are inductance and capacitance per section length. The cutoff frequency or bragg frequency is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{L_{lump} C_{lump}}} \tag{2.39}$$

where $L_{lump} = L_T/N_{seg}$, $C_{lump} = C_T/N_{seg}$. Nseg is the number of sections. L_T and C_T are the total inductance and capacitance respectively. The amplitude of oscillation (A) is determined by the product of the equivalent resistance (R_{eq}) of the filter tank and the differential current (I_{diff})

injected by gain stage. Assuming a near square output at a tap point, the waveform can be expressed as:

$$V(t) = \left(I_{diff} R_{eq} \times \frac{2}{\pi}\right) \sum_{k=0}^{n} \frac{\sin((2k+1)\omega_0 t)}{2k+1} \tag{2.40}$$

The relationship between operating frequency and cutoff frequency determine the harmonic content of voltage waveform. A limit on the number of iterative elements limits the number of harmonics. Under a low-loss approximation, the number of harmonics that can be sustained is given by [2]:

$$n_h = \left\lfloor \frac{N}{\pi} - \frac{1}{2} \right\rfloor \tag{2.41}$$

CHAPTER 3

Design Optimization and Sensitivity Analysis

This chapter deals with methods and techniques for improving the performance of RTWO. The critical parameters of RTWO design are studied through theory, simulation, and verified by board level prototype circuits.

3.1 Characteristic Impedance (Z_0) and Quality Factor Optimization

The performance of RTWO is dependent on the value of Z_0. In the following sections of this chapter we explore the impact of Z_0 on oscillation startup, system bandwidth, quality factor, waveform shape, phase noise, and power consumption. In the analysis of the startup condition, we observed that the transconductance of the gain stage for oscillation has an inverse dependence on Z_0. For a fixed transmission line length, increasing Z_0 will reduce the required g_m of the amplifier stage. In high frequency application, designing with the minimum possible transistor sizes while maintaining amplification and oscillation is important for achieving the high operating frequency. Table 3.1 shows the required minimum g_m for different coupled microstrip transmission lines. While maintaining a constant spacing of 20 μm between two coupled transmission lines, the width of the line was varied from from 2 μm to 40 μm. Line length is 400 μm. For each step, we calculate *exp(αl)* , the corresponding Z_0, and the required minimum Gm. The coupled transmission line uses top metal layer for signal lines and lower metal layer (metal 1) as the ground layer. For most transmission lines in RFICs, conductor and dielectric losses are relatively low and attenuation constant in low loss limit is given by:

$$\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} + \frac{G}{2}\sqrt{\frac{L}{C}} \approx \frac{R}{2Z_0} + \frac{GZ_0}{2} \tag{3.1}$$

Since $G \approx 0$, α reduces to:

$$\alpha \approx \frac{R}{2Z_0} \tag{3.2}$$

Table 3.1

Required Minimum gm for Different Coupled Transmission Lines (Spacing = 20 μm, Section Length (l) = 400 μm)

Line width (μm)	Odd mode Z_0 (Ω)	Resistance (Ω/mm)	Exp(αl) (l = 0.4 mm)	$2/Z_0$ (mS)	Required g_m (mS)
2	59.51	3.5	1.0118	33.61	34.01
5	51.75	1.4	1.0054	38.65	38.86
10	42.61	0.7	1.0033	46.94	47.09
20	31.86	0.35	1.0022	62.77	62.91
40	21.38	0.175	1.0016	93.55	93.70

It is clear from Table 3.1 that $2/Z_0$ is the dominant factor to consider for the estimation of required minimum g_m. With prior knowledge of the required g_m, Z_0 has to be optimized by adjusting the width and spacing of coupled transmission line. Figure 3.1 shows characteristic impedance as a function of line width and spacing for the IBM 0.18 μm RF CMOS process. This plot gives some basis for selecting the width and spacing for an RTWO design. Z_0 is estimated from SPECTRE model of microstrip transmission line. The IBM 0.18 μm process for RF application offers six metal layers for interconnections. The transmission line model used for simulation requires a dedicated lower metal layer (metal 1) as ground. The first metal level (M1) is specified as ground and the top metal (AM) is set as the transmission line.

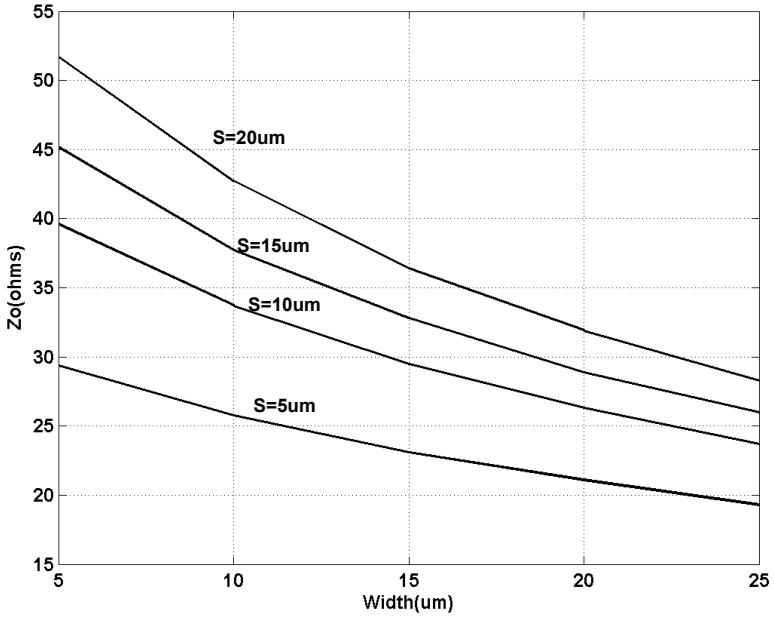


Figure 3.1. Plot of Z_0 as a function of line width and spacing

The quality factor of RF tuned circuits is important for consideration in bandwidth estimation, ringing and oscillation phase noise. The quality factor (Q) of a distributed resonator is given as:

$$Q = \omega_0 \times \frac{energy\ stored}{average\ power\ dissipated} \tag{3.3}$$

where ω_0 is the fundamental radian frequency.

In the low loss limit, Q can be rewritten as:

$$Q = \omega_0 \times \frac{(LI_{rms}^2 + CV_{rms}^2)/2}{(RI_{rms}^2 + GV_{rms}^2)/2} \tag{3.4}$$

where V_{rms} and I_{rms} are the RMS value of the voltage and current in the resonator. For periodically loaded transmission line, Q can be shown to be [12]:

$$Q_T = Q\left(1 - \frac{\omega_0^2}{\omega_c}\right) \tag{3.5}$$

where ω_c is the cutoff radians frequency for a section of the line and Q_T is the total quality factor of RTWO. You improve the total quality factor by increasing the number of periodic segments of RTWO.

3.2 Gm Cell Optimization

Cross-coupled inverter pair is the basic amplification unit for the RTWO. It is crucial to understand the interaction between CCIP and the propagating wave on the transmission line. CCIP is distributed along the transmission line to provide amplification. Preceding CCIP stage will force a mostly differential signal to the next CCIP. Figure 3.2 and 3.3 shows the large signal response test circuit and operating regions of line current versus line voltage respectively.

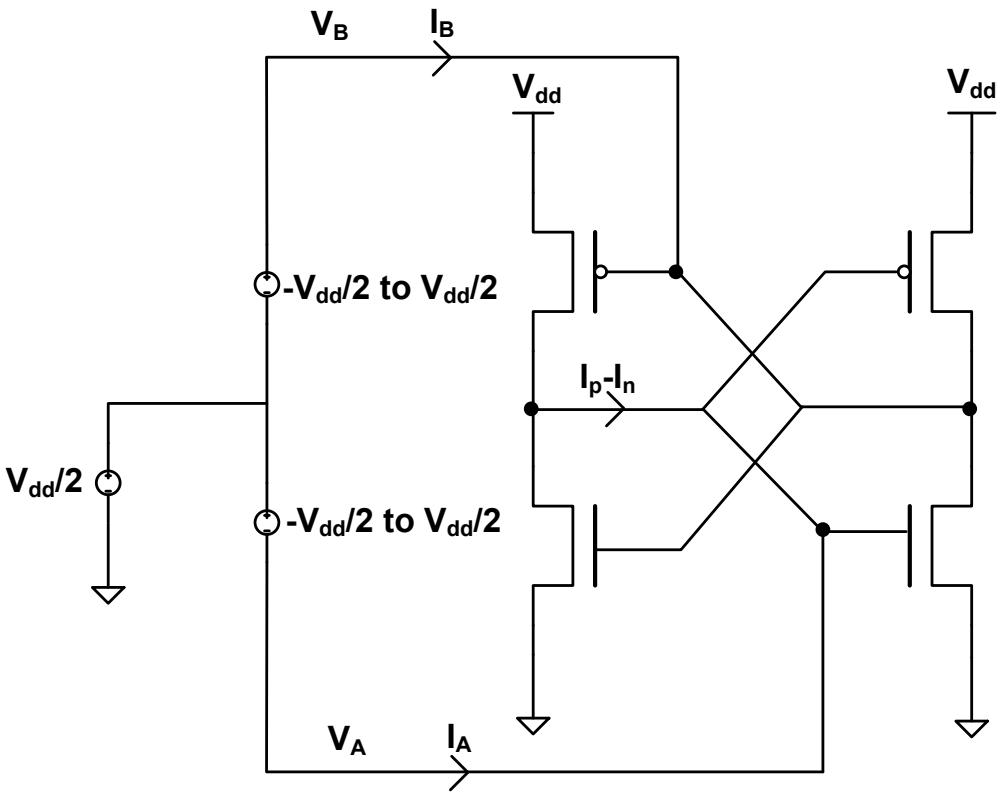


*Figure 3.2.*Large signal response test circuit

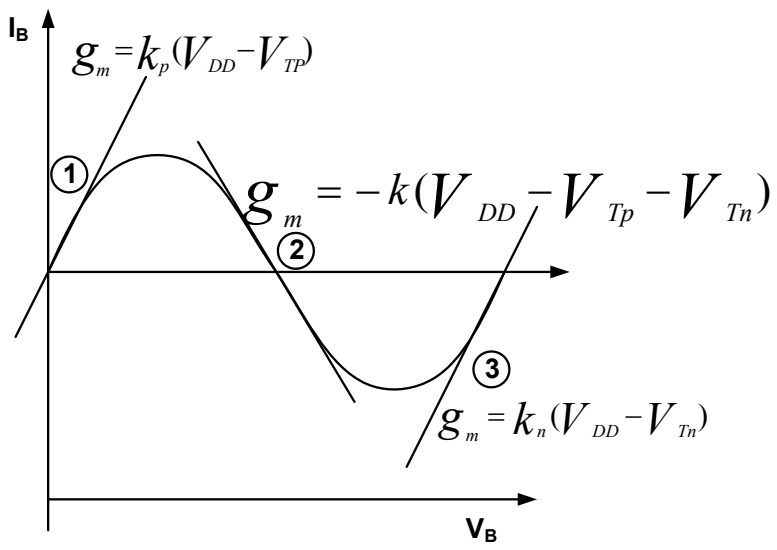


Figure 3.3. Operating regions; 2 – Gain region, 1 and 3 – Loss region

The potentials V_A, V_B and currents I_A, I_B are at the two ends of CCIP. In the differential mode, the following relations hold: $V_A+V_B=V_{DD}$ and $I_B = - I_A$. V_{TN} and V_{TP} are the threshold voltages of NMOS and PMOS, respectively. When $V_A<V_{TN}$, PMOS is in linear region and NMOS is in off-state. When $V_A> V_{DD} -|V_{TP}|$, NMOS in linear region and PMOS in off-state. When V_A is in between V_{TN} and $V_{DD} -|V_{TP}|$, the net current is the drain current difference between PMOS and NMOS transistors. Based on these relationships, the DC, I_B of CCIP in odd mode operation is expressed as:

$$I_B = \begin{cases} K_p\left(V_{DD} - \frac{3}{2}V_A - |V_{TP}|\right)V_A & V_A < V_{TN} \\ \frac{K_p}{2}(V_{DD} - V_A - |V_{TP}|)^2 - \frac{K_n}{2}(V_A - V_{TN})^2 & V_{DD} - |V_{TP}| > V_A > V_{TN} \\ -K_n\left(V_{DD} - \frac{3}{2}V_B - V_{TN}\right)V_B & V_A > V_{DD} - |V_{TP}| \end{cases} \quad (3.6)$$

Regions 1 and 3 as shown in Figure 3.3 represent positive resistance regions where the inverter pair behaves as a shunt ohmic resistor. Region 2 represents the negative resistance region where the inverter pair amplifies the input differential signal. This is the nonlinear nature

of the CCIP, which presents different effects for forward and backward waves. Backward wave has small amplitude which is attenuated by shunt ohmic resistance. Meanwhile, forward wave forces CCIP to enter region 2, gain region. It is reasonable to assume that the NMOS and PMOS transistors have the same trans-conductance parameters (properly sized transistors, that is, $K = K_n = K_p$). This ensures symmetric I-V response. The negative resistance (R) contributed by the CCIP is given as:

$$R = \frac{V - (-V)}{-g_m V} = -\frac{2}{g_m} \tag{3.7}$$

By taking the derivative of current (I_B) with respect to voltage (V_A), the negative transconductance (g_m) is given by:

$$g_m = -K \times \frac{(V_{DD} - V_{TN} - V_{TP})}{2} \tag{3.8}$$

where K is given by:

$$K = \frac{W \mu_o C_{ox}}{L} \tag{3.9}$$

3.2.1 Regenerative response analysis of CCIP. CCIP is essentially a latch or bistable circuit with two stable states, V_{dd} and ground when operated in the voltage limited regime. The CCIP as shown in Figure 3.4 consist of two inverter pairs cross connected as a sense amplifier. NMOS and PMOS transistors are sized to guarantee oscillation and are only used as initial values to study the latching properties.

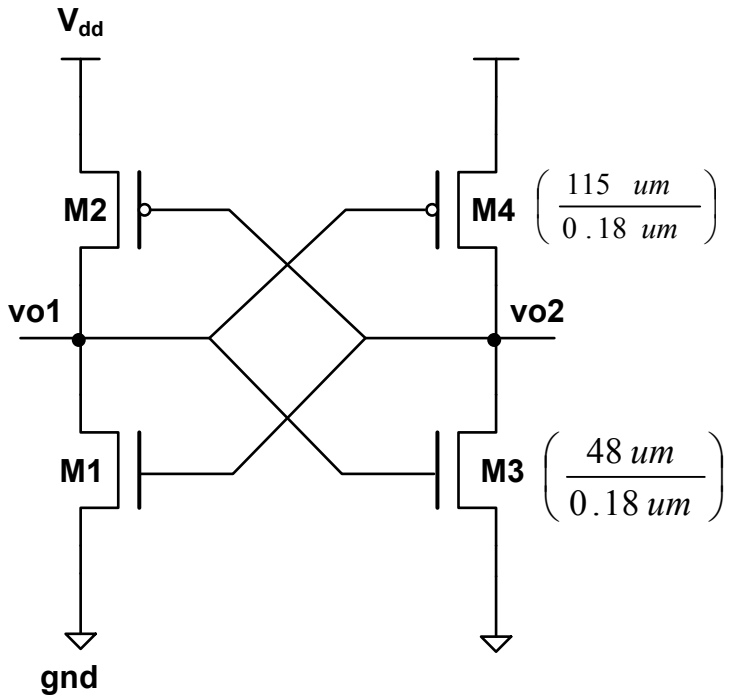


Figure 3.4. CCIP latch

Let us assume that signals v_{o1} and v_{o2} are applied to the latch's input nodes. These are initial voltages and will be designated as v'_{o1} and v'_{o2}. Depending on the relative values of initial input, one of the outputs will go high and the other will go low. Of interest to us in this section are the latch time constant and the propagation delay of CCIP for different relative initial input. Shown in Figure 3.5 is the small signal equivalent model of CCIP latch.

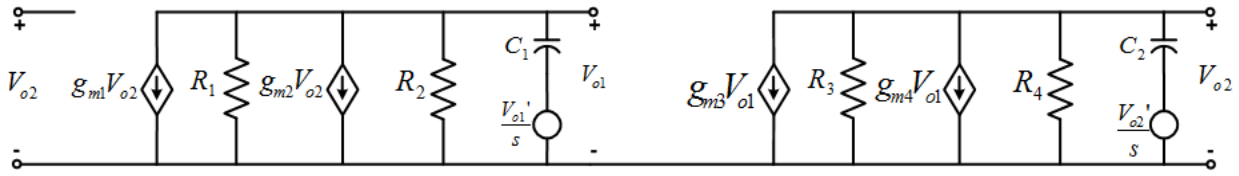


Figure 3.5. Small signal model of CCIP latch

Using nodal analysis, we can write for M1/M2

$$g_{m1}V_{o2} + G_1V_{o1} + g_{m2}V_{o2} + G_2V_{o1} + sC_1\left(V_{o1} - \frac{V_{o1}'}{s}\right) = 0 \tag{3.10}$$

Rearranging the terms in equation 3.10;

$$(g_{m1} + g_{m2})V_{o2} + (G_1+G_2)V_{o1} + sC_1V_{o1} - C_1{V_{o1}}' = 0 \tag{3.11}$$

For M3/M4,

$$g_{m3}V_{o1} + G_3V_{o2} + g_{m4}V_{o1} + G_4V_{o2} + sC_2\left(V_{o2} - \frac{{V_{o2}}'}{s}\right) = 0 \tag{3.12}$$

Rearranging the terms in equation 3.12;

$$(g_{m3} + g_{m4})V_{o1} + (G_3+G_4)V_{o2} + sC_2V_{o2} - C_2{V_{o2}}' = 0 \tag{3.13}$$

Solving for V_{o1} and V_{o2}:

$$V_{o1} = \frac{(R_1 \parallel R_2)C_1}{s(R_1 \parallel R_2)C_1 + 1}{V_{o1}}' - \frac{(g_{m1} + g_{m2})(R_1 \parallel R_2)}{s(R_1 \parallel R_2)C_1 + 1}V_{o2} \tag{3.14}$$

$$= \frac{\tau_1}{s\tau_1 + 1}{V_{o1}}' - \frac{(g_{m1} + g_{m2})(R_1 \parallel R_2)}{s\tau_1 + 1}V_{o2}$$

$$V_{o2} = \frac{(R_3 \parallel R_4)C_2}{s(R_3 \parallel R_4)C_2 + 1}{V_{o2}}' - \frac{(g_{m3} + g_{m4})(R_3 \parallel R_4)}{s(R_3 \parallel R_4)C_2 + 1}V_{o1} \tag{3.15}$$

$$= \frac{\tau_2}{s\tau_2 + 1}{V_{o2}}' - \frac{(g_{m3} + g_{m4})(R_3 \parallel R_4)}{s\tau_2 + 1}V_{o1}$$

Defining the output, ΔV_o , and the input ΔV_i as:

$$\Delta V_o = V_{o2} - V_{o1} \tag{3.16}$$

$$\Delta V_i = {V_{o2}}' - {V_{o1}}' \tag{3.17}$$

It reasonable to assume that $Gm = gm_1 + gm_2 = gm_3 + gm_4$; $\tau_{inv} = \tau_1 = \tau_2$ where Gm is the total transconductance of one inverter stage and τ_{inv} is the time constant of inverter.

Solving for ΔV_o gives:

$$\Delta V_o = V_{o2} - V_{o1} = \frac{\tau_{inv}}{s\tau_{inv} + 1}\Delta V_i + \frac{G_mR}{s\tau_{inv} + 1}\Delta V_o = \frac{\tau'\Delta V_i}{s\tau' + 1} \tag{3.18}$$

where

$$\tau' = \frac{\tau_{inv}}{1 - G_m R} \tag{3.19}$$

Taking the inverse Laplace transform gives:

$$\Delta V_{out}(t) = \Delta V_i e^{-t/\tau_{inv}} = \Delta V_i e^{-t(1-G_m R)/\tau_{inv}} \tag{3.20}$$

Define the latch time constant (τ_L) as:

$$\tau_L = \frac{\tau_{inv}}{1-G_m R} \text{ if } G_m R \gg 1, \tau_L = -\frac{\tau_{inv}}{G_m R} = -\frac{C}{G_m} \tag{3.21}$$

Normalizing ΔV_o to the final voltage difference after the latch operates gives

$$\frac{\Delta V_{out}(t)}{V_{OH} - V_{OL}} = e^{t/|\tau_L|} \frac{\Delta V_i}{V_{OH} - V_{OL}} \tag{3.22}$$

The test circuit in Figure 3.6 is used to simulate the latch response of CCIP.

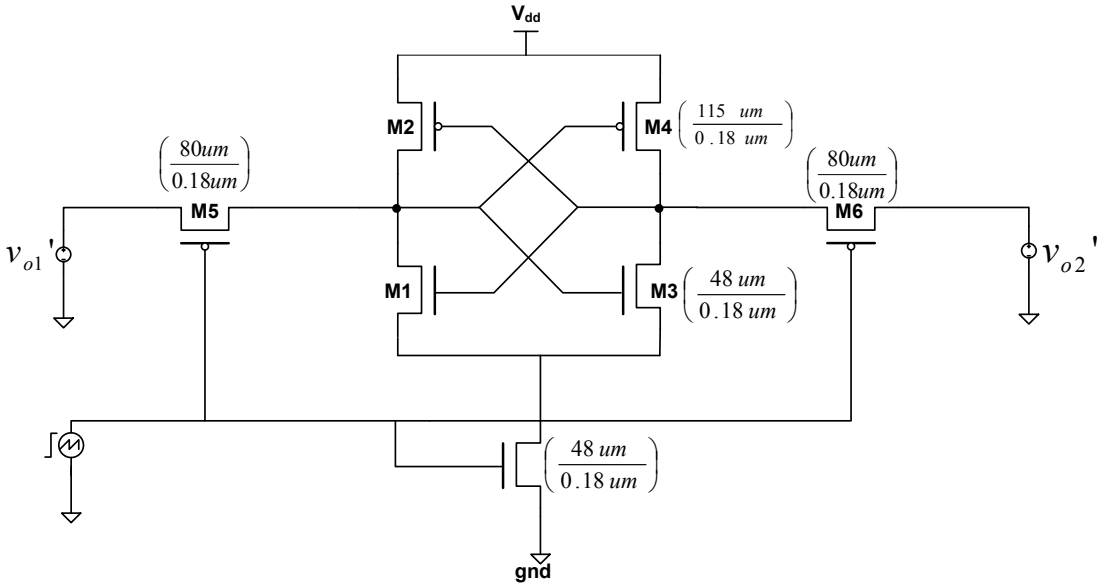


Figure 3.6. Test circuit for regenerative analysis

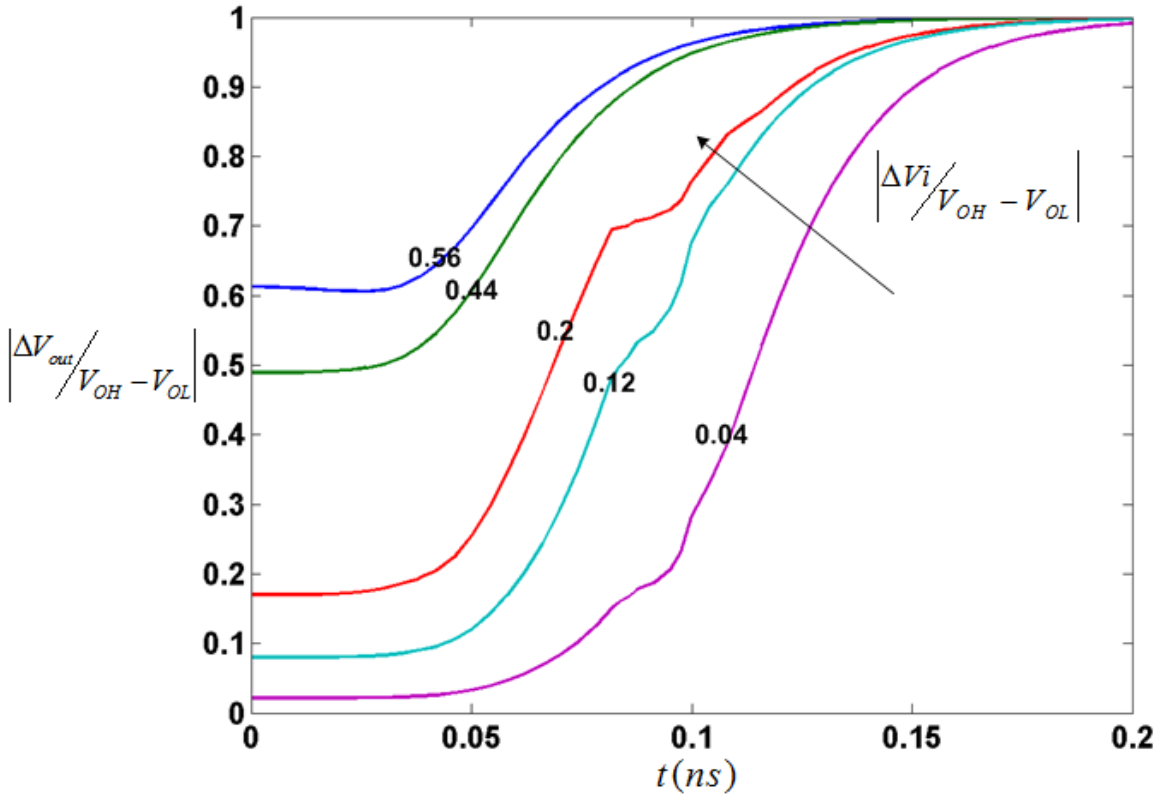


Figure 3.7. Transient response of CCIP for varying differential input voltages

The propagation delay of the latch can be found by setting equation 3.22 to 0.5 which results in;

$$t_p = \tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2\Delta V_i}\right) \tag{3.23}$$

From Figure 3.7, it can be interpreted that, the time required by $\Delta V_{out}$to reach $V_{OH}-V_{OL}$ is decreased for large initial differential input. This property can be utilized to speed up the CCIP for high frequency operation. Smaller time constant implies faster CCIP response. Figure 3.8 shows simulation of nonlinear behavior of CCIP.

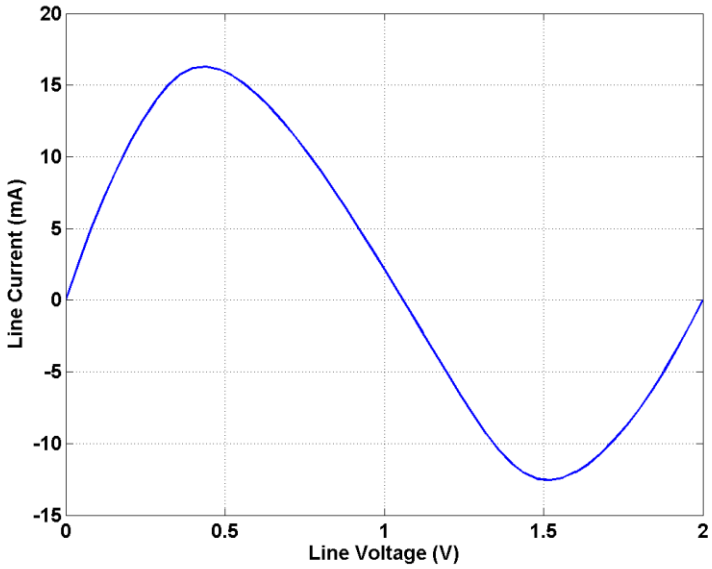


Figure 3.8. Nonlinear response of CCIP

Figure 3.9 shows a plot of the transconductance of NMOS and PMOS transistors for the CCIP shown in Figure 3.4. Maximum transconductance is achieved when line voltage is about half the voltage supply.

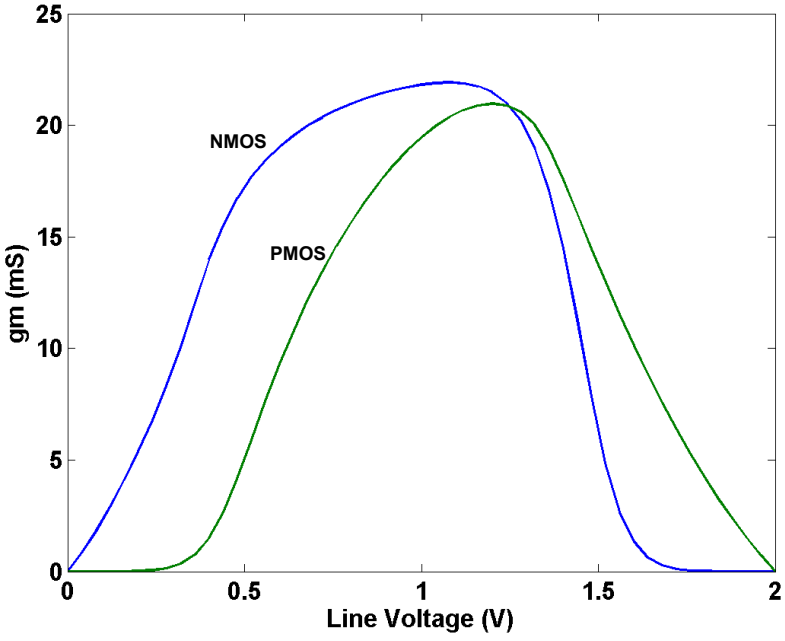


Figure 3.9. NMOS and PMOS gm plot

3.3 Phase Noise Analysis

3.3.1 Introduction. The impact of noise in both analog and digital systems design is of great importance. For example in transmitters, oscillator noise is amplified and fed to an antenna together with the transmitted signal has the potential to interfere with a near operating band. A considerable body of research has been reported on the analysis of phase noise for popular oscillators such as LC and ring oscillators. Research on RTWO phase noise research is ongoing. In reference [12], the impulse sensitivity function (ISF) proposed by Hajimiri and Lee [13] is used to derive a phase-noise expression for the RTWO. Koji et al [14] tackled this problem using a simple physical model of RTWO. In their analysis, the RTWO was considered as superposition of multiple standing wave oscillators with phase noise normalized to a single SWO. Among the three methods proposed by Hajimiri for calculating ISF, the direct measurement approach is the most accurate compared to the state-space and first derivative approach. The only drawback with this approach is that it involves simulation and can be time consuming depending on the number of transistors.

Using this approach for RTWO phase noise analysis can be daunting especially with increasing number of RTWO periodic sections which increases the number of transistors. With the normalized model of RTWO, the time involved in using the direct measurement method is reduced by a factor of N. In most of these works, the emphasis is placed on thermally induced phase noise [15-16] which is of most concern in industrial applications. Using the proposed model of Koji et al, the dynamics of coupled oscillator planar array is adapted for RTWO characterization. The normalized model helps us to extend noise analysis of LC oscillators to RTWO. It should be noted that a quarter-wave transmission line resonator can be modeled near resonance as a parallel RLC resonator. Hajimiri's method provides insights into both white

noise and 1/f noise up-conversion. The closed form solution by Grand de Mercey [12] for white noise will be used as we explore the features of coupled oscillator design that applies to RTWO and noise analysis.

3.3.2 Equivalent SWO model of RTWO. This section introduces an equivalent model of RTWO and its correlation with an array of coupled oscillators. RTWO can be converted into a single closed loop by unfolding and untwisting its crossover as shown in Figure 3.10.

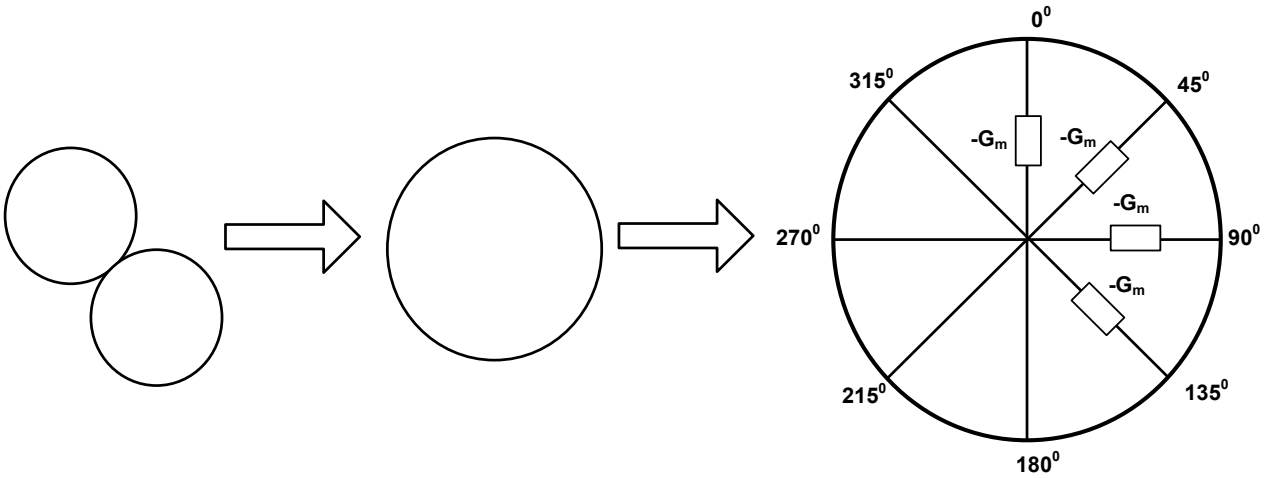


Figure 3.10. Transformation of RTWO to SWO model

This model was used by Koji et al for phase noise analysis. They also proved that RTWO can be modeled as injection locked multiple standing wave oscillators (SWOs) by solving the generalized Adler's equations [17]. These equations are typically used in coupled oscillator array dynamics. The model consists of a shared transmission line ring with differential gain stages connected to their respective relative phase nodes. Figure 3.11 shows the voltage waveform of RTWO and its SWO model at 6.5 GHz.

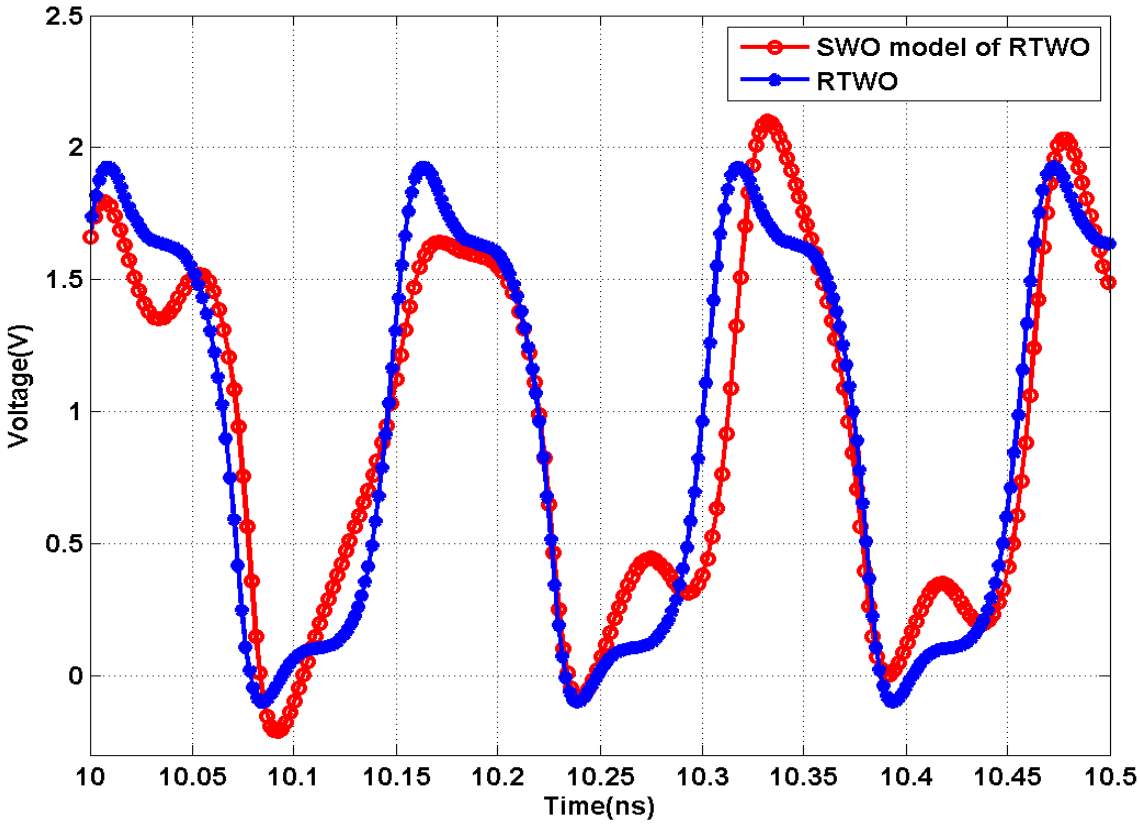


Figure 3.11. Trace plot of RTWO output versus SWO model

With this simplification, Koji extends the concept of coupled oscillator arrays (COA) to the injection locked model of RTWO. Nouri Neda [18] applied the same concept to develop a theoretical expression for the thermally induced phase noise in a 45GHz rotary wave oscillator. Phase noise analysis was based on Rael's method [19]. As shown in Figure 3.12, the SWO model of RTWO is a special case of near neighbor bilateral planar oscillator coupling where the last element of the network is feedback coupled to the first element. Oscillator elements are mutually synchronized to a common frequency called the ensemble frequency.

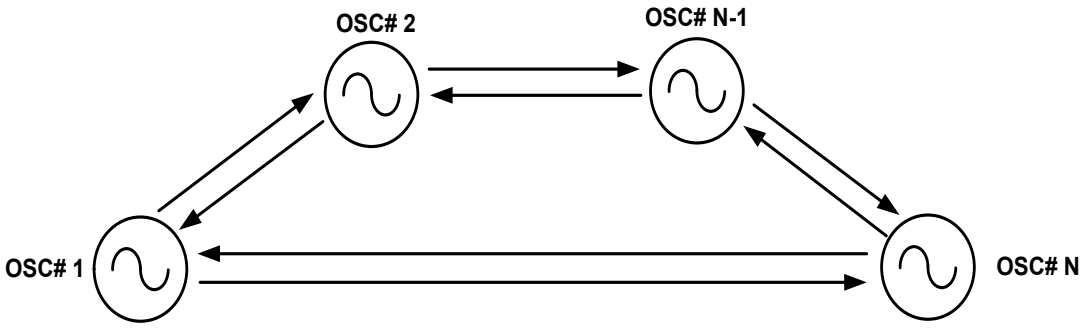


Figure 3.12. Feedback bilateral coupled SWO model of RTWO

It is generally desirable to have identical free-running frequencies for each oscillator unit with large injection-locking range. Large locking range is associated with low Q of individual oscillator. A low Q oscillator enhances phase control at the expense of phase noise, although this can be compensated by the injection-locking process to neighboring oscillators with increased coupling strength. Neglecting AM to PM conversion, its being shown by Chang et al that the total phase noise is reduced in proportion to 1/N, provided the coupling phase is chosen properly. RTWO is known for low skew low jitter clock distribution. In COA design any detuning between coupled oscillators results in skew that is directly related to the coupling strength and Q [20]. Therefore, low Q resonators that are strongly coupled are ideal for clock distribution. The RTWO can be interpreted as a low Q strongly coupled SWOs. In subsequent sections, we will describe how SWO model of RTWO agrees with this derivation. Changes of coupling strength with increased number of sections will be addressed.

3.3.3 Coupled oscillator arrays. The impact of coupling phase of COA has being described thoroughly by Sheteram et al for in- phase synchronization. Coupling is established through a transmission line based on the equivalent model of RTWO. The line network introduces phase coupling and delay in proportion to the number of sections around the RTWO ring. Before we delve into the analysis of coupling through a transmission line, we provide a

brief summary of COA theory. For an array of N parallel resonant oscillators with mutual coupling the differential equations, as derived by York, et. al. [21] are given as:

$$F_i([A],[\theta]) = j\frac{\omega_i}{2Q}\left[\frac{U^P\left(1-\frac{{A_i}^2}{{\alpha_i}^2}\right)-\sum_{j=1}^{N}\frac{Y_{ij}}{G_L}\frac{A_j}{A_i}e^{j(\theta_j-\theta_i)}}{1-j\frac{\omega_i}{2Q}\sum_{j=1}^{N}\frac{1}{G_L}\frac{\partial Y_{ij}}{\partial\omega}\frac{A_j}{A_i}e^{j(\theta_j-\theta_i)}}\right] \tag{3.24}$$

$$\frac{dA_i}{dt} = A_i \times Im\{F_i([A],[\theta])\} \tag{3.25}$$

$$\frac{d\theta_i}{dt} = \omega_i - Re\{F_i([A],[\theta])\} \tag{3.26}$$

The unknown quantities are A_i, the i^{th} oscillator's coupled amplitude; θ_i, the phase of the i^{th} oscillator; α_i, the uncoupled amplitude; ω_i, the free running frequency; Q, the quality factor; G_L, the load conductance; μ, the saturation factor; and Y_{ij}, the admittance of the coupling network from port i to port j. For broadband assumption of the coupling network,

$$\left|\frac{\omega_i}{2Q}\sum_{j=1}^{N}\frac{1}{G_L}\frac{\partial Y_{ij}}{\partial\omega}\frac{A_j}{A_i}\right| \ll 1 \tag{3.27}$$

and the denominator term can be ignored which simplifies the amplitude and phase dynamics. Y/G_L is the normalized coupling factor (ε). For N oscillators synchronized in-phase, phase dynamics can be expressed as:

$$\frac{d\theta_N}{dt} = \omega_N - \frac{\varepsilon\omega_N}{2Q}\sin(\theta_N - \theta_{N-1} + \Phi) \tag{3.28}$$

In steady state,

$$\frac{d\theta_i}{dt} = \omega, \forall i \tag{3.29}$$

The amplitude and phase dynamics in strongly coupled oscillator arrays have recently being reexamined by Seetharam and Pearson [22]. Compared to weak COA, strongly coupled oscillator arrays exhibit wider locking ranges and lower phase noise levels but violate the

broadband assumption concerning coupling network. It's being shown by Nogi et al that strongly coupled arrays exhibit many modes in which the oscillator amplitudes as well as the phases vary across the array and that only one mode has constant amplitude [23]. With this variation in amplitude, AM to PM modulation for phase noise analysis shouldn't be ignored unless the harmonic components of waveform are attenuated considerably. The coupling features of interest include delay, phase, and quality factor. The coupling network introduces time and position offset. Design parameters of coupling network include coupling strength, network bandwidth and oscillator loading. The key parameters can be derived from the denominator of equation 3.24. The approach presented by Pogorzelski [24] is used to study the SWO model of RTWO. This approach relates coupling network parameters to the network admittance matrix elements which in turn relates to the lumped elements. The physical quality factor is important for estimating the effective quality factor of SWO. The coupling strength which determines the locking range ($\Delta\omega_{lock}$) is given by:

$$\varepsilon = \left|\frac{-Y_{12}}{G_L}\right| \tag{3.30}$$

The locking range is defined as the frequency range by which the collective frequency of unit oscillators can deviate from synchronization frequency and still get locked. It expressed as:

$$\Delta\omega_{lock} = \frac{\varepsilon\omega_0}{2Q} \tag{3.31}$$

The quality factor of the coupling network, Qnet, according to Pogorzelski is given by:

$$Q_{net} = \frac{\omega}{2}\left|\frac{\frac{\partial}{\partial\omega}(Y_{11} + 2Y_{12}\cos\Delta\varphi)}{Y_{11} + 2Y_{12}\cos\Delta\varphi}\right|_{\omega=\omega_0} \tag{3.32}$$

where φ is the electrical length of the transmission line section of RTWO. The electrical length is equivalent to the relative phase between two tapping nodes. Table 3.2 compares the Qnet for

different section lengths. Results are based on the 6.5 GHz RTWO design example used for the simulation in Figure 3.11. The dimensions of the RTWO ring are 0.6-mm X 0.6-mm. Four amplifier stages are used with a section length is 600 μm. Using a line width of 10 μm and 20 μm spacing, the characteristic impedance of the line is estimated as 57 Ω. The distributed approximation stipulates that capacitive parasitics of the gain stage are absorbed into the line if the spacing between gain stages is sufficiently close. Electrical length decreases for increasing number of sections as $\cos\Delta\varphi$ approaches 1. The cutoff frequency of coupling network is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{L_{net}C_{net}}} \tag{3.33}$$

where $L_{net} = L_T/N_E$, $C_{net} = C_T/N_E$. N_E is the number of coupling network elements. L_T and C_T are the total inductance and capacitance of distributed resonator respectively.

Table 3.2

Quality Factor for Varying Number of Sections

Number of Sections	Section length (um)	Relative phase	Cuttoff frequency (GHz)	Qnet
4	600	45^0	78.85	24.6
8	300	22.5^0	157.7	49.2
16	150	11.25^0	315.4	98.4

For low loss approximation, the quality factor of the coupling network is alternatively expressed as [12]:

$$Q = \frac{\omega_0\sqrt{LC}}{R/Z_0 + GZ_0} = \frac{\beta}{2\alpha} \tag{3.34}$$

3.3.4 Analysis of ½ wavelength SWO. Each SWO unit in Koji's model of the RTWO has half wavelength (λ/2) coupled transmission line as its frequency selective unit. With each SWO unit strongly coupled to each other, the equivalent conductance of the coupling network additionally loads the SWO. From equation 3.26, G_L is approximately equal to $1/Z_0$ for low loss and broadband assumption. Ignoring the impact of parasitic loading from amplifiers especially for close spacing, the effective quality factor of oscillator is the parallel combination of the unloaded SWO Q and the Q of network. Table 3.3 compares the unloaded Q, effective and coupling strength for different number of sections.

Table 3.3

Coupling Strengths for Varying Number of Sections

Number of Sections	Unloaded SWO Q	Effective Q	Coupling strength
4	5.9	4.75	0.68
8	5.9	5.26	1.27
16	5.9	5.56	2.39

Although the effective Q is significantly low, an increase in Qnet is indicative of phase noise improvement.

3.3.5 Noise analysis

3.3.5.1 Normalized noise model. It has been shown through extensive research in the area of COA design that the phase noise of COA is related to the uncoupled single unit by the expression;

$$\left|\widetilde{\delta\theta}_{total}\right|^2 = \frac{1}{N}\left|\widetilde{\delta\theta}_i\right|^2_{uncoupled} \tag{3.35}$$

where N is the number of uncoupled oscillators. To demonstrate the validity of this approximation, the phase noise of a coupled oscillator array is simulated using Cadence Spectre. Figure 3.13 shows the plot of the COA phase noise to that of the single uncoupled SWO operating at 8.6 GHz.

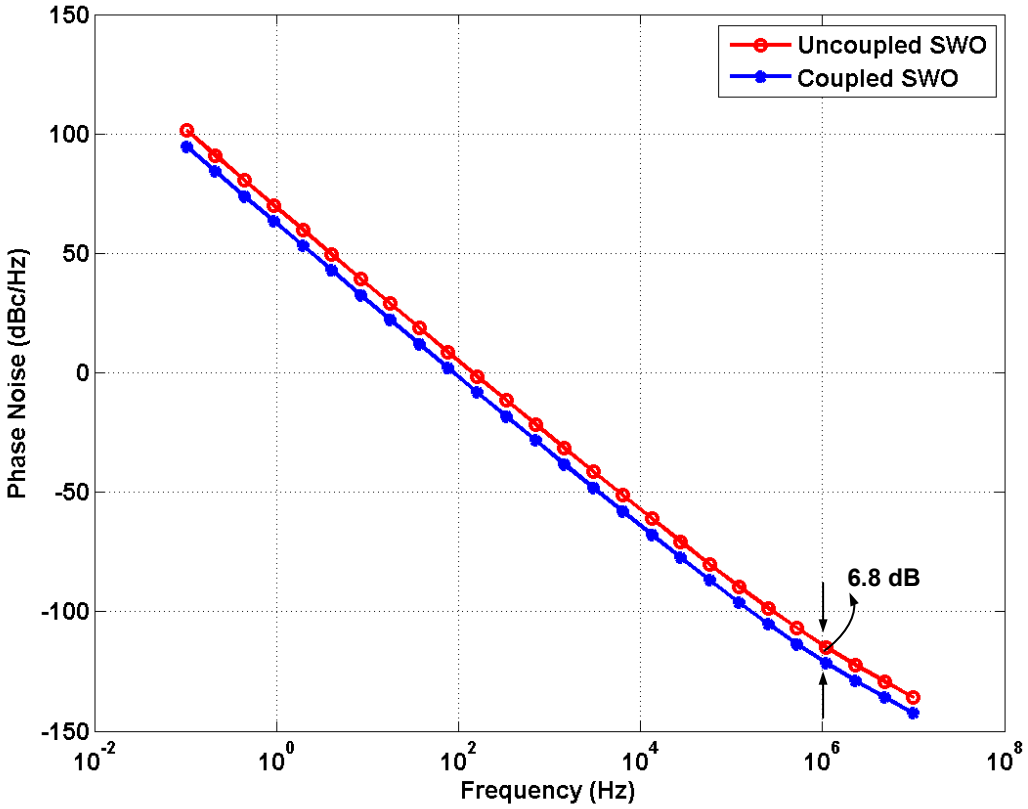


Figure 3.13. Uncoupled and coupled SWO phase noise plot

The phase difference at 1 MHz offset is 6.8 dB suggests a value of N= 4.78. The coupled oscillator consists of four sections. The fractional part can be attributed to the ignored PM-AM modulation in this simplification.

3.3.5.2 Phase noise theory. The main noise sources which impact RF circuits include thermal, shot and 1/f noise among other noise sources such as popcorn. The inevitable presence of these noise sources introduces instabilities in oscillator's output phase and amplitude. Instabilities in the frequency domain are popularly called phase noise whereas that in time domain is called jitter. In the frequency domain, noise is usually characterized in terms of the single sideband noise spectral density and has the conventional units of decibels below the carrier per Hertz (dBc/Hz). As shown in Figure 3.14, to quantify phase noise, we consider a unit bandwidth at Δω offset and calculate the noise power in this bandwidth. Phase noise is expressed as;

$$L\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}}\right] \tag{3.36}$$

where $P_{sideband}$ is the noise power at Δω offset and $P_{carrier}$ is the signal power.

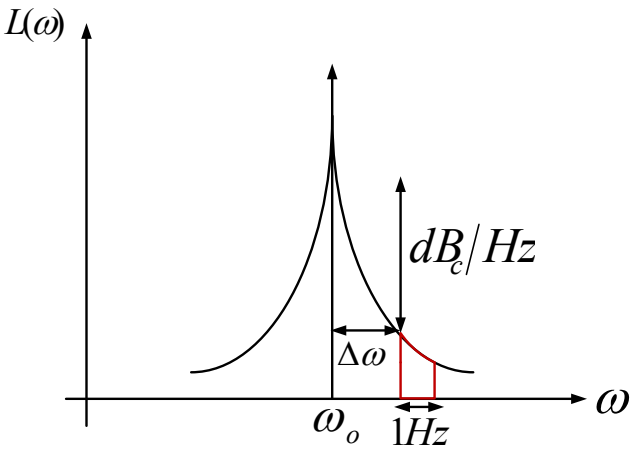


Figure 3.14. The phase noise per unit bandwidth

Figure 3.15 shows the phase noise, L(Δω), of the free-running oscillator as a function of Δω. Three distinct noise regions namely 1/f noise (A), thermal noise (B) and noise floor (C) regions are apparent in this plot.

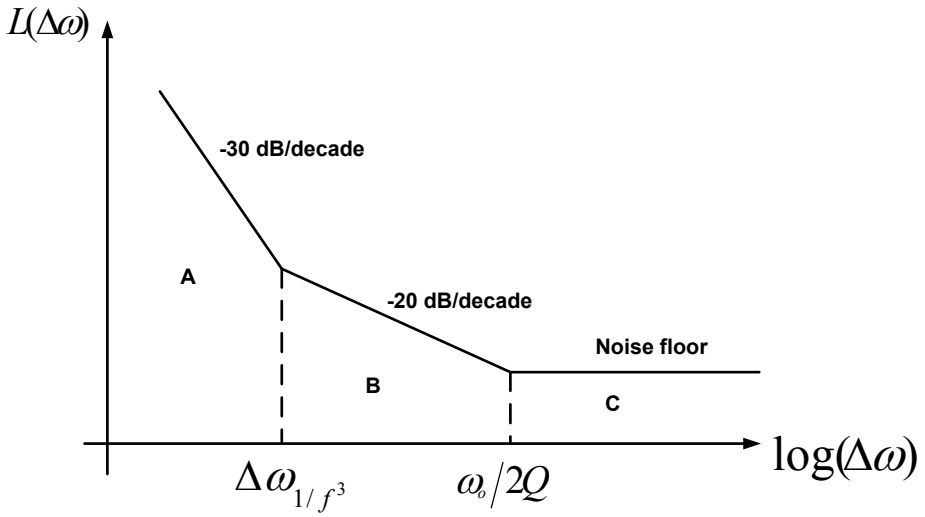


Figure 3.15. A typical phase noise plot for a free running oscillator

Flicker noise contribution is primarily from the transistors while thermal noise is from both the transistors and the resonant tank. Three popular models for analysis of the phase noise of oscillators are Leeson's model, Hajimiri's approach, and Rael's method. Hajimiri's method is a useful numerical procedure to determine phase noise and provides insights into 1/f noise up-conversion and impact of noise current modulation. Rael's method is useful for CMOS negative resistance circuits. Leeson model is based on linear time invariance and predicts phase noise as:

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega^3{}_{1/f}}{|\Delta\omega|}\right)\right] \qquad (3.37)$$

where F is an experimental parameter, k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_o is the oscillation frequency, Q_L is the effective quality factor of the tank with all loadings accounted for (also known as loaded Q), $\Delta\omega$ is the offset from the carrier, and $\omega^3{}_{1/f}$ is the frequency of the corner between $1/f^3$ and $1/f^2$ regions. Hajimiri's model introduced the concept of impulse sensitivity function (ISF) which encodes information about the sensitivity of the oscillator to an impulse

injected at a certain phase. In this model, noise is modeled as impulse current injected into the node of interest. Impulse response is written as:

$$h_{\emptyset}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{3.38}$$

where *u(t)* is the unit step function, $\Gamma(x)$ is the impulse sensitivity function (ISF), q_{max} is the maximum charge displacement across the capacitor. The maximum value of the ISF appears near the zero crossing of the oscillation. The phase noise in the 20 dB slope is given by:

$$L\{\Delta\omega\} = 10\log\left(\frac{{\Gamma^2}_{rms}}{2{q^2}_{max}}\frac{\frac{\overline{i^2_n}}{\Delta f}}{2\Delta\omega^2}\right) \tag{3.39}$$

The phase noise in the 30 dB slope is given by:

$$L\{\Delta\omega\} = 10\log\left(\frac{\frac{\overline{i^2_n}}{\Delta f}c_0^2}{8{q^2}_{max}\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{3.40}$$

where $\frac{\overline{i^2_n}}{\Delta f}$ is the total unmodulated noise spectral density of the noise across transistors in the circuit. C_0 is the DC coefficient of the fourier series expansion of the ISF.

3.3.5.3 LTV approach – single SWO oscillator. In the special case of a second-order system the ISF can be expressed as:

$$\Gamma(x) = \frac{f'}{f'^2 + f''^2} \tag{3.41}$$

where *f* is the normalized function of voltage signal. For a ring oscillator with N identical stages, the denominator can be approximated as ${f'^2}_{max}$. For the transmission line dominated oscillation, RTWO would generate square wave output. A square wave, *f(x)*, can be expressed as;

$$f(x) = \left(\frac{2}{\pi}\right)\sum_{k=1}^{n}\frac{\sin\big((2k+1)x\big)}{2k+1}. \tag{3.42}$$

It has been shown by Grand de Mercey [12] that thermally induced noise in RTWO is given by:

$$L\{\Delta\omega\} = 10\log\left(\frac{4Z_{0,l}\frac{\overline{\iota^2 n}}{\Delta f}}{NP_{diss}Q_L^2}\frac{\omega_0^2}{\Delta\omega^2}\right) \tag{3.43}$$

For a single uncoupled SWO, the phase noise expression reduces to:

$$L\{\Delta\omega\} = 10\log\left(\frac{4Z_{0,l}\frac{\overline{\iota^2 n,uncoupled}}{\Delta f}}{P_{diss}/_N\, Q_L^2}\frac{\omega_0^2}{\Delta\omega^2}\right) \tag{3.44}$$

The unmodulated noise spectral density of the gain stage (CCIP) is given by [13]:

$$\frac{\overline{\iota^2 n,uncoupled}}{\Delta f} = \frac{\overline{\iota^2 n,NMOS}}{\Delta f} + \frac{\overline{\iota^2 n,PMOS}}{\Delta f} = 4kT\gamma G_m \tag{3.45}$$

where

$$\gamma = \frac{\gamma_{NMOS} + \gamma_{PMOS}}{2} \tag{3.46}$$

Assuming

$$G_{m,NMOS} = G_{m,PMOS} = \frac{G_m}{2} \tag{3.47}$$

$Z_{0,l}$ is the loaded impedance of the line defined as:

$$Z_{0,l} = \sqrt{\frac{l_{sec}L_0}{l_{sec}C_0 + C_{equ}}} \tag{3.48}$$

where C_{equ} is the equivalent loading capacitance of the CCIP, buffer, and any other parasitics. l_{sec} is the distance between two stages in [m] Ignoring the loading from the buffer in this analysis and taking into account loading from gain stage, C_{equ} is given by:

$$C_{equ} = C_{dg,N1} + C_{dg,N2} + C_{dg,P1} + C_{dg,P2} + \left(\frac{C_{gs,N1} + C_{gs,N2} + C_{db,N1} + C_{db,N2}}{4}\right) + \left(\frac{C_{gs,P1} + C_{gs,P2} + C_{db,P1} + C_{db,P2}}{4}\right) \quad (3.49)$$

C_{equ} was calculated as 531.84 fF for the CCIP example in Figure 3.4. For a 10 μm width coupled transmission line with 20 μm spacing, the loaded characteristic impedance was calculated as 19.6 Ω. RTWO used for simulation operates at 6.5 GHz with a ring length of 4.8 mm. Table 3.4 shows the phase noise comparison for varying number of sections based on simulation. Using the analytical formula in equation 3.44, Table 3.5 shows the phase noise comparison for varying number of sections.

Table 3.4

RTWO Phase Noise for Varying Number of Sections - Simulated

Number of Sections	Uncoupled SWO Phase noise (dBc/Hz)	Phase noise (dBc/Hz) – RTWO circuit	(W/L), nmos (μm/μm)	(W/L), pmos (μm/μm)
4	-113.5	-120.8	48/0.18	115.2/0.18
8	-112	123.4	24/0.18	57.6/0.18
16	-111.1	126.2	12/0.18	28.8/0.18

Table 3.5

RTWO Phase Noise for Varying Number of Sections - Calculated

Number of Sections	Uncoupled SWO Phase noise (dBc/Hz)	Phase noise (dBc/Hz) – normalized SWO model	Phase noise (dBc/Hz) – RTWO circuit	(W/L), nmos (μm/μm)	(W/L), pmos (μm/μm)
4	-112.3	-118.3	-120.6	48/0.18	115.2/0.18
8	-111	-120	123.6	24/0.18	57.6/0.18
16	-110	-122	126.4	12/0.18	28.8/0.18

3.4 Multi-objective Optimization

RTWO design is a multi-objective optimization problem with tradeoffs of typical performance measures as power and phase noise. In this section, non-dominated based genetic algorithm for multi-objective optimization is presented to determine the Pareto optimal front of solutions for low power and phase noise with emphasis on variation of transmission line width and spacing. Optimization is followed by sensitivity assessment wherein Monte Carlo simulations and corner analysis are performed on the Pareto points with respect to process variations. The algorithm is validated in the design of RTWO whose frequency varies between 3 to 5GHz due to varying dimensions of coupled transmission line. The optimization is a two-step process. A neural network is developed from experimental data to estimate phase noise and power dissipation with transmission line width and spacing as inputs. The neural network is then coupled with genetic algorithm for subsequent design optimization. Results show a set of solutions for width and spacing with objective functions less sensitive to process variations.

3.4.1 Introduction. Compared with L-C tank oscillators and other wave-based oscillators, RTWO design is a multi-parameter optimization problem in which several design requirements must be met simultaneously. The presence of multiple objectives in a problem, in principle, gives rise to a set of optimal solutions, instead of a single optimal solution. In the absence of any further information, one of these Pareto-optimal solutions cannot be said to be better than the other. This demands a user to find as many Pareto optimal solutions as possible [25]. A Human Decision Maker (DM) is necessary to make the often difficult trade-offs between conflicting objectives of multi-objective problems. Traditional optimization methods require the continuity of design space, explicit objective function, and the derivative information of the optimization function. Genetic algorithms have been used for design and optimization because of their efficiency in nonlinear multi-parameter search and optimization [26]. Instead of a generic solution for analog circuits, a solution specific algorithm is developed and simulated.

3.4.2 Problem formulation and solution tools. The design of an electronic oscillator is characterized mainly by frequency, power, and phase measurement. Low power consumption is obtained at the expense of phase noise and vice versa. The algorithm implemented solves this problem of achieving both low phase noise and power consumption of the oscillator. The design equations in a line dominant RTWO design are provided next. The clock frequency (*f*) is given by:

$$f = \frac{V_p}{2l} \tag{3.50}$$

The power dissipation (P_{disp}) is approximately given as:

$$P_{disp} \approx \frac{{V_{DD}}^2}{{Z_0}^2} R_{loop} \tag{3.51}$$

where R_{loop} is the resistance of transmission line ring. Assuming white noise as the dominant source of noise, the phase noise for RTWO is written as:

$$L(\Delta f) = \frac{\Gamma^2{}_{rms} \times N \times \left(\bar{i}_t^{\,2} / \Delta f \right)}{q^2{}_{max} (2\pi \Delta f)^2} \tag{3.52}$$

where $\bar{i}_t^{\,2}$ is the noise density for the inverter pair, q_{max} is the maximum charge swing and $\Gamma^2{}_{rms}$ is the RMS value for the impulse sensitivity function (ISF) of the RTWO.

The genetic algorithm used in this problem, NSGA II, is an implementation of an elitist evolutionary algorithm developed by Deb K et al [27]. Table 3.6 summarizes the features of the multi-objective algorithm.

Table 3.6

Non-dominated Sorting Genetic Algorithm (NSGA) II Features

Fitness assignment	Diversity mechanism	Elitism
Ranking based on non-domination sorting	Crowding distance	Yes

There are several neural network (NN) structures and algorithms for microwave device optimization including multilayer perceptrons (MLP) and radial bases function networks (RBF). MLP falls in the feed-forward neural networks category and is used for modeling RTWO phase noise and power based on experimental data. By using neural network, one accounts for the manufacturing variations in design and implementation.

3.4.3 Optimization objective and design specification. Table 3.7 shows conflicting objective functions tackled in this problem.

Table 3.7

Conflicting Objective Functions

Function	Objective
Power	Low
Phase noise	Low

Table 3.8 shows the design variables used in the optimization and simulation of RTWO.

Table 3.8

Design Variables and Constraints

Design Variables		Constraints
Transmission line	Width	2.4 μm ≤ w ≤ 20 μm
	Spacing	2.4 μm ≤ w ≤ 20 μm
	Ring length	8 mm
CCIP	NMOS width	96 μm
	PMOS width	192 μm
	# of CCIPs	4

The selection of ring length is based on iterative simulation of RTWO for typical values of width and spacing to obtain a frequency of interest (3 to 5 GHz). The size of PMOS and NMOS transistors and the number of CCIPs are defined to guarantee oscillation and provide the needed gain to compensate for losses in the transmission line. The voltage supply to CCIP was set to a typical value of 2V. The physical constraints for the width and spacing of transmission line are based on limitation of coupled transmission line models in IBM 0.18 μm technology. In

this problem the decision variables are thus the transmission line width, spacing, and the clock frequency. Each set of width and spacing affects the total capacitance and inductance which consequently affects the power, phase noise, and oscillation frequency.

3.4.4 Optimization Process. Features of the methodology used in the optimization process are shown in Figure 3.16.

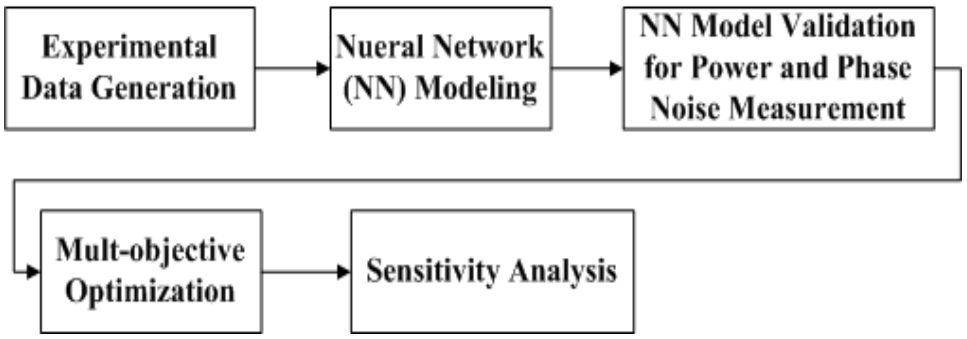


Figure 3.16. Optimization flowchart

Experimental data was generated using CADENCE IC design software. Table 3.9 shows the generated data for power and phase noise at 1 MHz offset for random values of width and spacing for training within the defined constraints.

Table 3.9

Training Data

Line Width (um)	Line Separation (um)	Phase Noise (dBc/Hz) @1MHz offset	Power (mW)
9.6	3.9	-121.0	120.68
15.3	5.8	-121.5	106.94
2.9	8.6	-118.3	140.26
5.8	2.0	-120.3	159.56
3.9	6.7	-119.4	134.16

Table 3.9

Cont.

3.9	12.4	-119.3	122.6
19.1	5.8	-121.7	107.32
8.6	11.5	-120.6	102.28
2.9	9.6	-118.6	137.88
2.0	20.0	-117.3	138.2
20.0	16.2	-121.6	96.6
14.3	15.3	-121.2	95.2
12.4	5.8	-121.4	108.2
5.8	8.6	-119.8	115.6
18.1	9.6	-121.6	100.4
13.4	19.1	-121.0	91.4
12.4	7.7	-121.2	103.2
9.6	19.1	-120.5	93.4
11.5	15.3	-120.9	96
7.7	4.8	-120.5	120

Table 3.9 shows that phase noise [min, max] = [-121.7,-117.3] and power [min, max] = [0.0914, 0.15956]. Neural network modeling was implemented in MATLAB. Out of twenty five random values, 80% of the experimental data was used for training the network while 20% of the data was used for testing the network. Table 3.10 presents a comparison between the model and simulation data.

Table 3.10

Comparison between the Model and Simulation data

Line Width (um)	Line Separation (um)	Phase Noise @1MHz offset		Power (W)	
		Sim.	NN Model	Sim.	NN Model
9.6	11.5	-120.6	-120.70	0.1006	0.1039
12.4	6.7	-121.3	-121.26	0.1056	0.1076
5.8	4.8	-119.9	-119.92	0.1282	0.1261
19.1	17.2	-121.5	-121.51	0.095	0.0932
4.8	8.6	-119.5	-119.41	0.1214	0.1279

NSGA II algorithm was implemented in MATLAB. Algorithm listing [27] from step 1 to 8 summarizes the optimization process.

Step 1: Create a random parent population P_0 of size N and set *t = 0, where t represents iterative step*

Step 2: Apply crossover and mutation to P_0 to create offspring population Q_0 of size N

Step 3: If the stopping criterion is satisfied, stop and return to P_t

Step 4: Set $R_t = P_t \cup Q_t$

Step 5: Using the fast non-dominated sorting algorithm, identify the non-dominated front F_1, F_2... Fr in R_t

Step 6: For i = 1… k do following steps:

Step 6.1: Calculate crowding distance of the solutions in F_i

Step 6.2: Create P_{t+1} as follows:

Case 1: If $|P_{t+1}| + |F_i| \leq N$, *then set* $P_{t+1} = P_{t+1} \cup F_i$

Case 2: If $|P_{t+1}| + |F_i| > N$, *then add the least crowded* $N - |P_{t+1}|$ *solutions from* F_i *to* P_{t+1}

Step 7: Use binary tournament selection based on the crowding distance to select parents from P_{t+1}. *Apply crossover and mutation to* P_{t+1} *to create offspring population* Q_{t+1} *of size N*

Step 8: Set t = t + 1, and go to Step 3

For the genetic algorithm:

Population size=20, Probability of crossover=0.9, Probability of mutation=0.85, Number of independent variables=2, Number of dependent variables=2.

Figure 3.17 shows the pareto optimal front of possible selections for transmission line width and spacing for low power and low phase noise without one objective having dominance over the other, which is also summarized in Table 3.11.

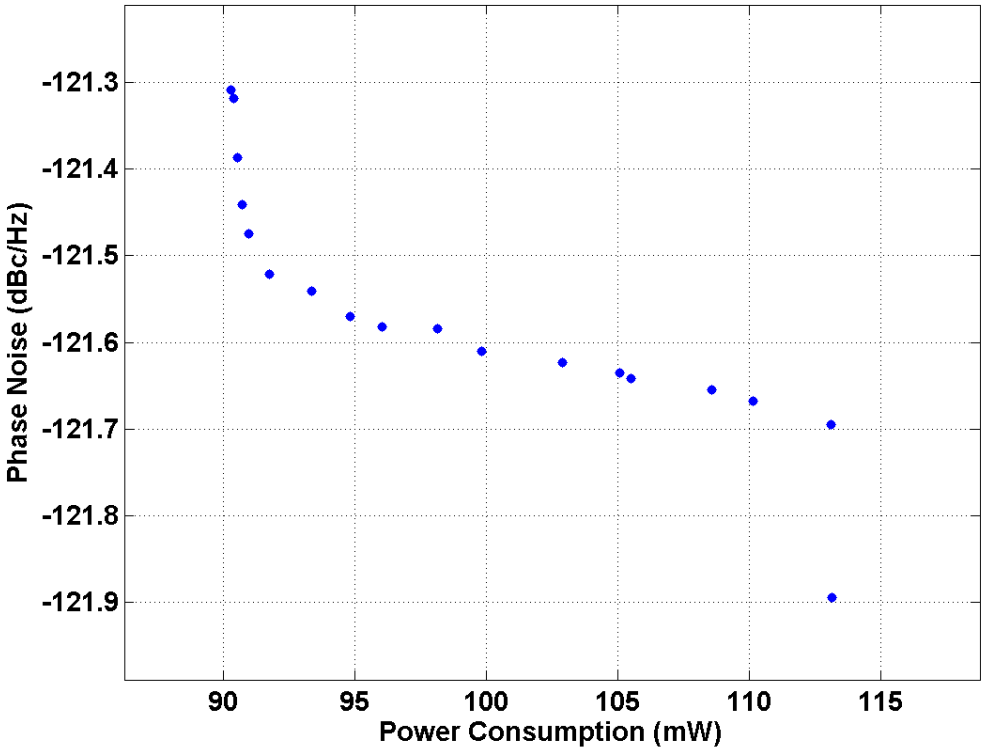


Figure 3.17. Pareto optimal front

Table 3.11

Possible Solutions for Width and Spacing

Line Width (um)	Line Spacing (um)	Power (mW)	Phase noise (dBc/Hz) @1MHz offset
15.323	20.000	91	-121.21
19.858	14.898	100	-121.61
17.591	19.150	91	-121.38
20.000	16.882	95	-121.58
15.323	19.150	91	-121.23

Table 3.11

Cont.

20.000	9.795	113	-121.69
19.150	10.362	111	-121.65
20.000	12.913	107	-121.65
19.858	13.055	106	-121.64
19.575	13.622	103	-121.62

By increasing the line width for instance, one reduces the resistance and power is reduced as a result. Less resistance also implies less contribution to phase noise. Since the modeling of power and phase noise is based on nominal conditions, sensitivity analysis is required for possible process variations. Sensitivity (corner analysis) of power and phase noise to process variation was performed on the ten possible solutions out of the twenty using Cadence Spectre. Table 3.11 shows the solutions and the corresponding optimized power and phase noise from genetic algorithm optimization. The algorithm is capable to searching for solutions for width and spacing within the defined physical constraints that gives low phase noise and power without one performance measure dominating the other. The range of frequencies for TT corner or nominal case is 3.85 GHz to 4.33 GHz for the ten possible solutions. Summarized in Table 3.12 is worst case percentage change from nominal of all measurements of interest for the seven possible process corners. The percentage change in frequency (f) for instance is given as:

$$\%\ change\ in\ f = \frac{\Delta f}{f_{nom}} \times 100\% \tag{3.53}$$

Table 3.12

Worst Case Percentage Changes from Nominal Solution

Process corner	Solution set	Worst case % change in frequency	Worst case % change in power	Worst case % change in Phase noise
SSF(1)-FFF(7)	1	0.78	10.17	0.45
SSF(1)-FFF(7)	2	0.48	10	0.33
SSF(1)-FFF(7)	3	0.25	9.88	0.49
SSF(1)-FFF(7)	4	0.49	10.04	0.33
SSF(1)-FFF(7)	5	0.52	10.09	0.41
SSF(1)-FFF(7)	6	0.23	9.84	0.33
SSF(1)-FFF(7)	7	0.23	9.62	0.25
SSF(1)-FFF(7)	8	0.47	9.99	0.41
SSF(1)-FFF(7)	9	0.48	9.70	0.49
SSF(1)-FFF(7)	10	0.24	10.05	0.33

Monte-Carlo simulations were run on all the ten possible solutions. Monte-Carlo simulation consists of 200 runs. Table 3.13 shows the average coefficient of variance (CV) of possible solutions which is given by:

$$CV = \frac{\sigma}{\mu} \times 100\% \tag{3.54}$$

where σ and μ are the standard deviation and mean of statistical results respectively.

Table 3.13

Average Coefficient of Variance

Solution set	Average CV (frequency)	Average CV (Phase noise)	Average CV (power)
1-10	1.2%	0.3%	1.7%

3.5 Amplification Stage Limitation

In this section, the frequency limiting factor through analysis and board level implementation of Rotary Traveling Wave Oscillator (RTWO) is presented. Relationship between the frequency limit and the amplification stage is established.

3.5.1 Relationship between frequency, CCIP and line delay. The transmission line of the RTWO serves as a filter whereas the inverter pair provides the needed compensation (amplification) for shunt and series losses. Once oscillation starts up, dynamics of wave propagation is based more on nonlinear factors than linear factors (small signal model), thus the large signal analysis is required. The clock period, T, is given approximately by:

$$T = \frac{2L}{V_p} \tag{3.55}$$

where V_p is expressed as:

$$V_p = \frac{1}{\sqrt{L_0 C_0}} \tag{3.56}$$

L_0 and C_0 are the inductance and capacitance per unit length of the line. The ×2 factor in equation 3.55 arises from the pulse requiring two complete laps for a single cycle. L is the physical length of the ring. Equation 3.55 implies a linear relationship between the period of

oscillation and the ring length. A plot of the relationship shows the non-linear dependence as the delay of the line becomes less significant in dictating the operation of the system.

To understand the time period-length relationship, the capacitive contributions from the transmission line and the inverter pair to oscillation period is analyzed separately. Assuming a linear function,

$$T = \frac{\delta T}{\delta L} L + T_0 \tag{3.57}$$

where T_0 is the time period of interception when L is approximately zero. From equation 3.55,

$$T = 2L\sqrt{L_0\left(C_{line} + \frac{NC_{inv}}{L}\right)} = 2\sqrt{L^2 \cdot L_0 C_{line} + N \cdot C_{inv} L} \tag{3.58}$$

From equation 3.47 the slope of the line is given by:

$$\frac{\delta T}{\delta L} = \frac{2L_0 C_{line} L + N.C_{inv}}{\sqrt{L^2 L_0 C_{line} + N.C_{inv} L}} \tag{3.59}$$

The interception point, T_0, is given by:

$$T_0 = T - \frac{\delta T}{\delta L} L \tag{3.60}$$

$$T_0 = 2\sqrt{L^2 \cdot L_0 C_{line} + N \cdot C_{inv} L} - \left(\frac{2L_0 C_{line} L + N.C_{inv}}{\sqrt{L^2 L_0 C_{line} + N.C_{inv} L}}\right) L \tag{3.61}$$

$$T_0 = \frac{N.C_{inv} L}{\sqrt{L^2 \cdot L_0 C_{line} + N \cdot C_{inv} L}} = \frac{2N.C_{inv} L}{T} \tag{3.62}$$

C_{line} is the capacitance contribution from the transmission line section. N is the number of sections which is equal to the number of amplifier stages (CCIPs). A plot of T versus L (ring length) is shown in Figure 3.18 based on the mathematical model. Figure 3.19 shows ADS simulation results of the oscillation frequency for different sizes of RTWO.

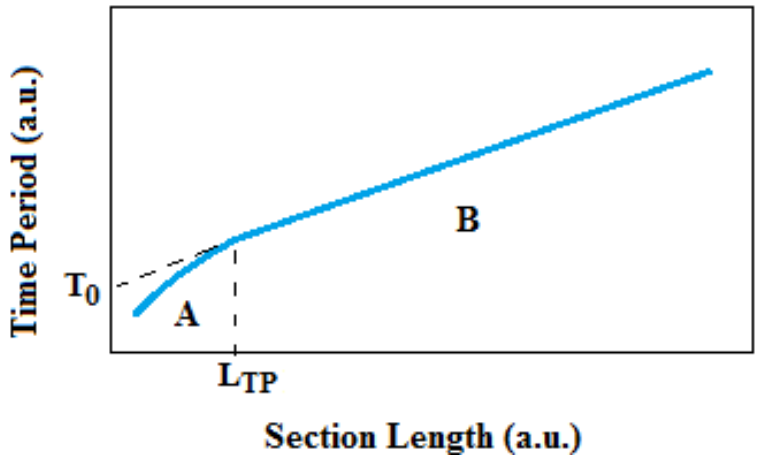


Figure 3.18. Analytical relationship between oscillation period and single lap length (L)

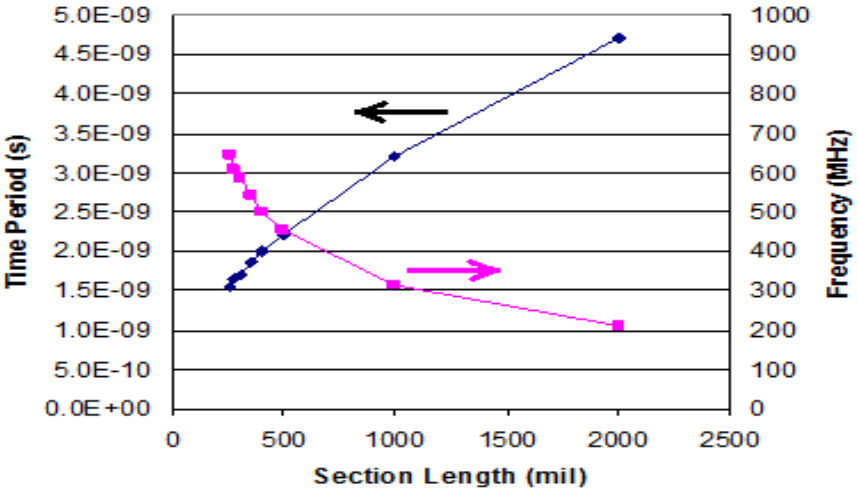


Figure 3.19. Oscillation period and frequency versus single lap length (L) – ADS simulation

It can be seen from the graphical relationship that, the curve deviate away from its linear progression as L approaches zero. L_{TP} is the length threshold where the curve switches from region B (linear function) to region A (non-linear function). In region B, propagation delay of the transmission line is dominant, thus the frequency of oscillation is dictated by the physical length of the transmission line. At L_{TP} the interaction between the propagation delay of the line (τ-line) and inverter pair (τ-inverter) becomes significant and marks the onset of inverter dominant oscillation. In region B, inverter pair switches fast enough to compensate for losses

presented by the line. The output is a near square wave as the inverter pair swings between its two latched states. As the length of the ring decreases to region A, the output waveform has less harmonic components with a slight degradation in peak to peak swing. This indicates that the slow inverter pair cannot recover all the signal strength before it switches back to its stable state. Designs for RTWO should avoid region A, thus it puts a limit on the high operating frequency achievable with certain CCIP characteristics.

3.5.2 Experimental results. To test above analysis, the RTWO is prototyped in Rogers' print circuit board with surface mount off-the-shelf components, including TI's SN74LVC3G04 triple invertor gates and Fairchild's NC7WZ16P6X dual buffers. To confirm the analysis presented above, various simulations and measurements were carried on the different RTWOs with different ring sizes and shapes. To accommodate the off-the-shelf invertor delay (~4nS), loading capacitors are used to slow down the phase speed and make RTWO have large effective electrical length to operate in region B (Figure 3.18). Figure 3.20 shows the fabricated RTWO ring structure with and without loading capacitors.

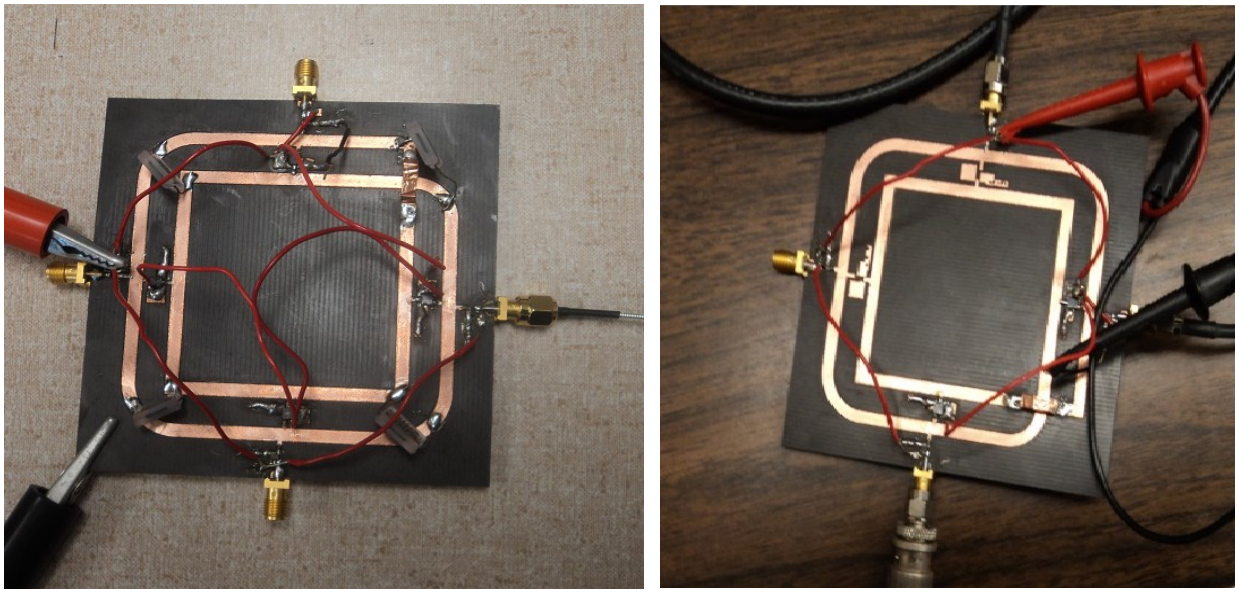


Figure 3.20. Fabricated RTWO with and without loading capacitors

The measured fundamental frequencies of RTWO with and without capacitive loading are 22.9MHz and 270 MHz respectively. Figure 3.21 and 22 show the phase noise of the RTWO with and without capacitive loading respectively.

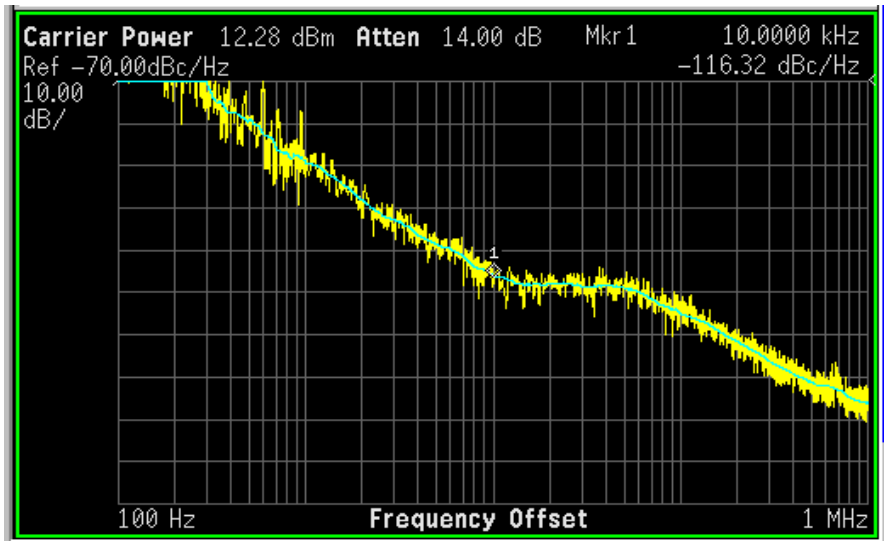


Figure 3.21. Measured phase of RTWO with capacitive loading

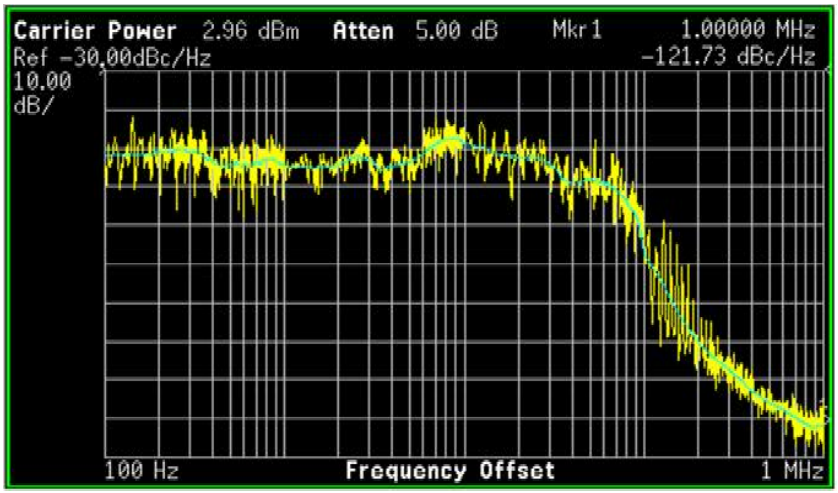


Figure 3.22. Measured phase of RTWO without capacitive loading

It can be observed that the RTWO without capacitive loading has high phase noise up to 50 KHz before it starts to drop. Due to frequency difference in both cases, the phase noise is compared at the same fractional offset instead of absolute frequency offset as shown in Table 3.14. It can be seen that RTWO without capacitive loading operates in region A (Figure 3.18) as

compared to the one with capacitive loading in region B (Figure 3.18). Phase noise measurements were taken using Agilent Spectrum Analyzer.

Table 3.14

Phase Noise Comparison with and without Loading Capacitors

Frequency fractional offset	Phase noise for RTWO with loading Capacitors	Phase noise for RTWO without loading Capacitors
0.01%	-100 dBc @2.3KHz	-55 dBc @27KHz
0.1%	-118 dBc @23KHz	-105 dBc @270KHz

The data shows that the quality of the oscillation signal is governed by the ratio of the line capacitance to the total capacitance of the cross coupled inverter pairs. Low capacitance ratio (C_{line}/C_{ccip}) will lead to signal instability and high phase noise.

3.6 EM Analysis

The RTWO by virtue of its structure has the potential to radiate energy. Of interest to us for electromagnetic interference (EMI) is the far field EM pattern. In this section, the study of EM far field is presented. The mechanism to effectively attenuating the backward wave propagation which helps to improve phase noise is also discussed. SONNET is used to simulate electromagnetic field produced by RTWO.

3.6.1 Backward wave propagation and attenuation. Backward propagating wave generation is inevitable due to the reflections from impedance mismatches. Thus it is worthwhile to investigate backward wave propagation in details. Figure 3.23 shows the circuit for the backward wave propagation analysis.

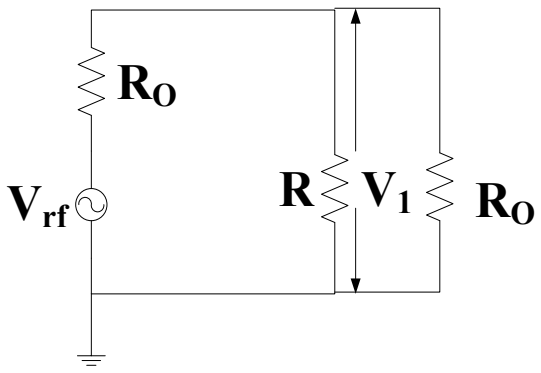


Figure 3.23. Circuit model for backward wave analysis

V_{rf} is the voltage source due to backward wave, R_o is the internal resistance of the voltage source, R is the shunt resistance presented by cross-coupled inverter pair (CCIP) seen by backward wave, and V_1 is the voltage across R. The wave power is given by the following relation:

$$P_{rf} = \frac{V_{rf}^2}{8R_0} \tag{3.63}$$

The power dissipated by the resistance of CCIP, P'_{rf}, as the backward wave propagates is deducted as following:

$$V_1 = \frac{R//R_0}{R_0 + R//R_0} V_{rf} = \frac{V_{rf}}{R_0/_R + 2} \tag{3.64}$$

$$P_{rf}{}' = \frac{{V_1}^2}{2R} = \left(\frac{1}{R_0/_R + 2} \right)^2 \times \frac{{V_{rf}}^2}{2R} \tag{3.65}$$

The ratio of power consumed by R to the power generated by the backward wave source is given by:

$$\frac{P_{rf}{}'}{P_{rf}} = \frac{4\left(R_0/R\right)}{\left(R_0/R + 2\right)^2} \tag{3.66}$$

From equation 3.66, it can be further deducted that the maximal ratio (50%) can be reached when $R_0=2R$. Since the backward wave is one of the primary sources of phase noise and disturbance, the on-resistance of CCIP should present about half of the line impedance value to minimize the disturbance. For forward traveling wave, CCIP amplifies the signal. However, backward traveling waves see a shunt ON resistance of CCIP. CCIP does not amplify the backward traveling wave.

3.6.2 Backward wave propagation – simulation and results. A square ring RTWO is designed and simulated using SONNET. The ring is excited using a single differential port to represent the backward propagating wave. Figure 3.24 shows the RTWO structure laid out with SONNET. For backward wave simulation, the CCIPs are represented in circuit by positive discrete resistances. The characteristic impedance of ring is 52 Ω.

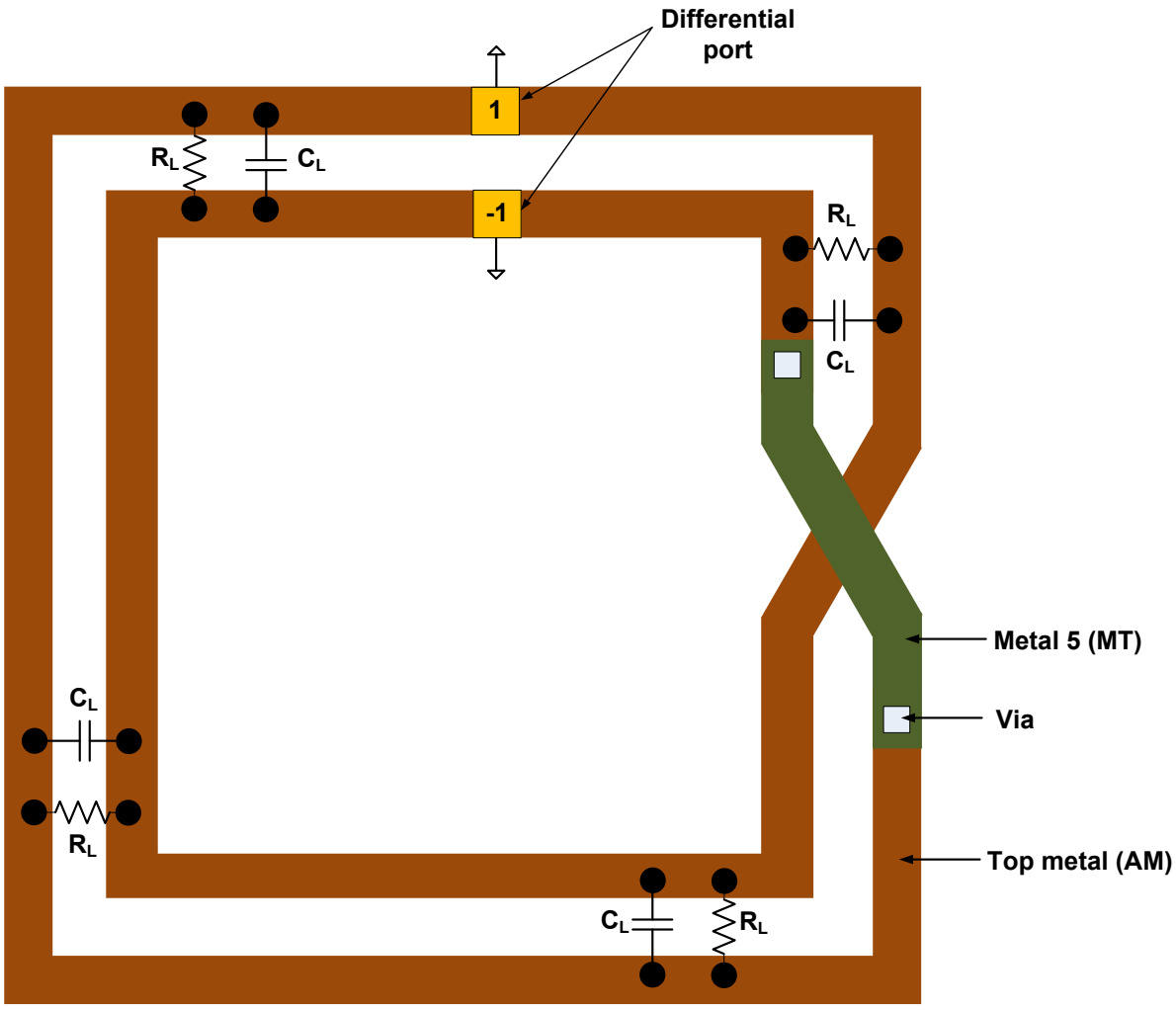


Figure 3.24. RTWO structure with distributed resistive and capacitive elements

C_L in Figure 3.24 represents external capacitive load and amplifier stage. R_L represents the equivalent resistance from amplifier stage either in the saturation or linear region. The ring is designed to naturally resonate at 2.4 GHz. Figure 3.25 shows the reflection coefficient (S11) for the on-resistance equal to 1Ω, 15 Ω, 25 Ω, 50 Ω and infinite. Figure 3.26 shows the EM field distribution around the ring.

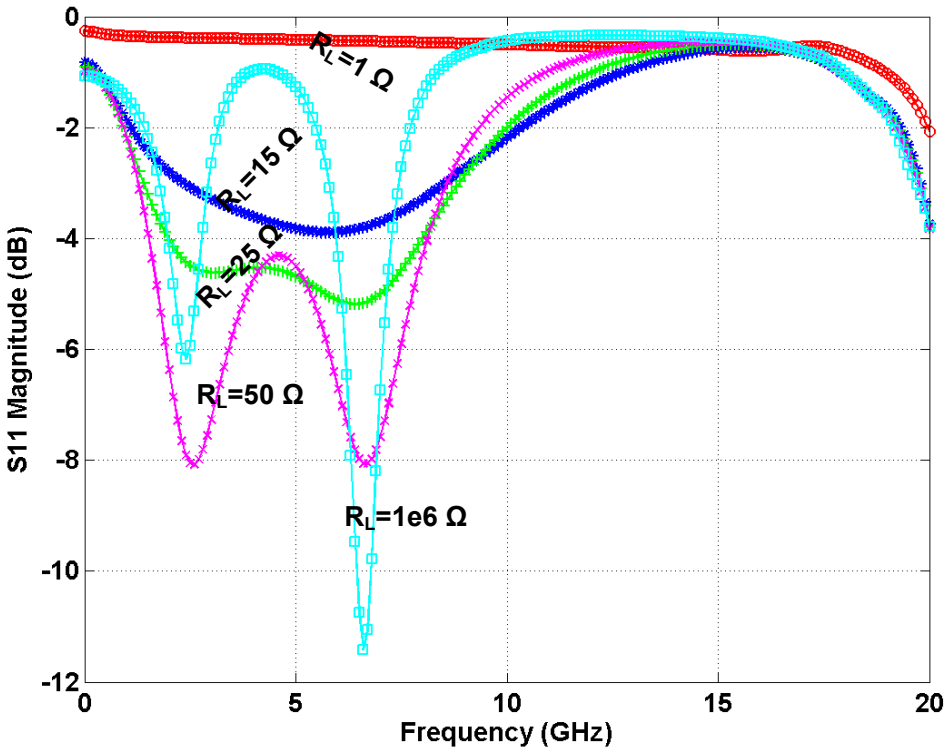


Figure 3.25. S11 for various ohmic shunt resistances

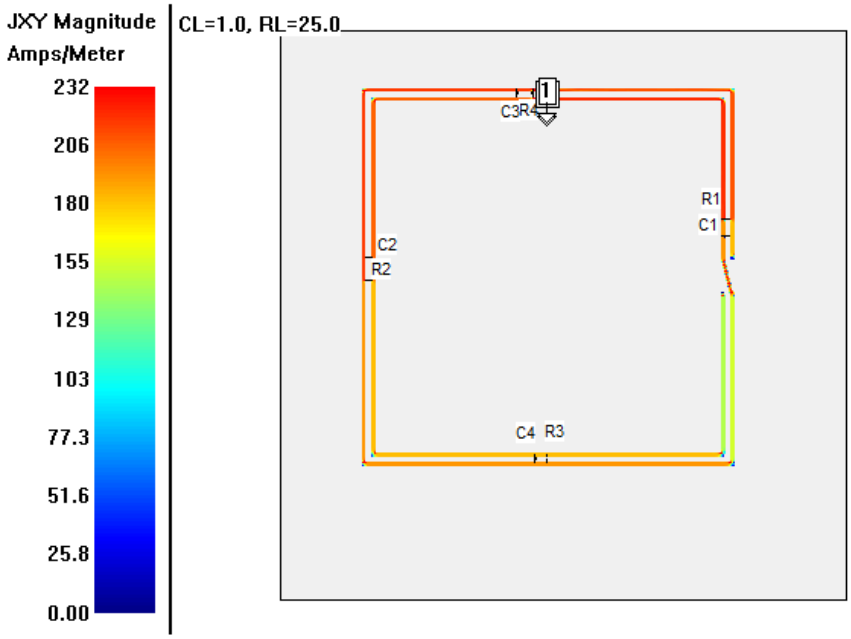


Figure 3.26. Current density at 2.4 GHz for R=25 Ω

RTWO with R=25 Ω presents a broad band low reflection coefficients, while the RTWO with high R values show narrow band resonance and the one with low R values reflect most power back. Under this condition, RTWO with R=25 Ω dissipates most power for a wide frequency range. The simulation results are consistent with the theoretical analysis of the previous section, i.e. the $R_0=2R$ gives the best power attenuation condition for the backward wave in RTWO. Since backward wave is primarily due to mismatches, it has a broad band nature and can best be attenuated under the above condition ($Z_0=2R$).

3.6.3 RTWO far field radiation pattern. In order to study the radiation behavior of RTWO, we compare the far field radiation pattern to that of a loop antenna. The loop antenna and RTWO are designed using the very top metal. Figure 3.27 shows the substrate used in the EM simulation.

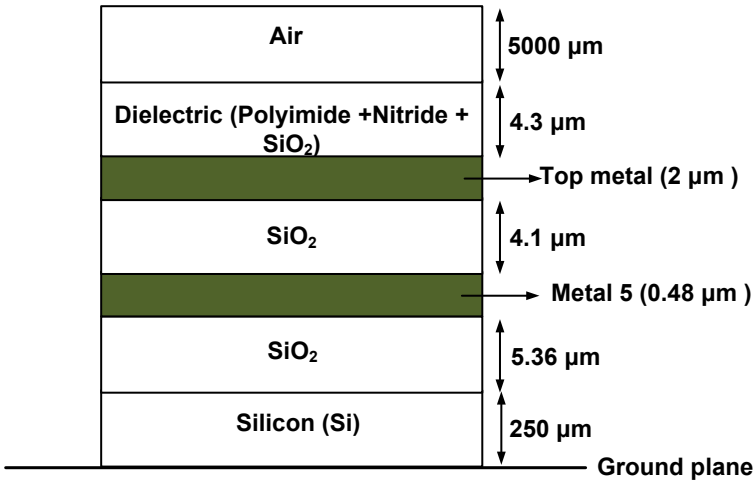


Figure 3.27. Silicon substrate, oxide, metal layers used in the EM simulation

Figure 3.28 and 3.29 show the layout of single loop antenna and RTWO antenna respectively. Layout area is 850-µm X 850-µm. Line width is 40 µm and spacing between lines is 80 µm. Figure 3.30 and 3.31 show the antenna gain of loop antenna and RTWO antenna respectively.

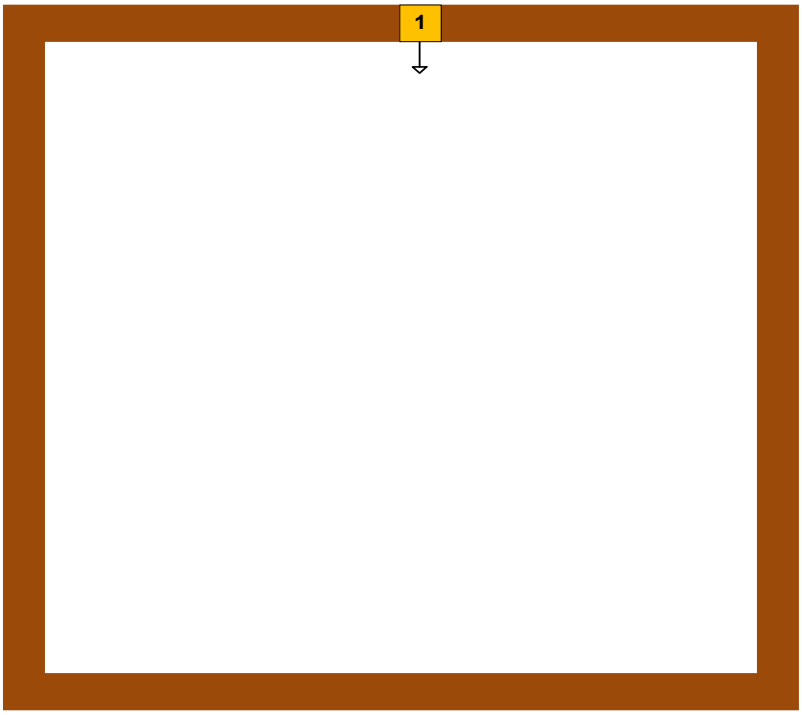


Figure 3.28. Loop antenna

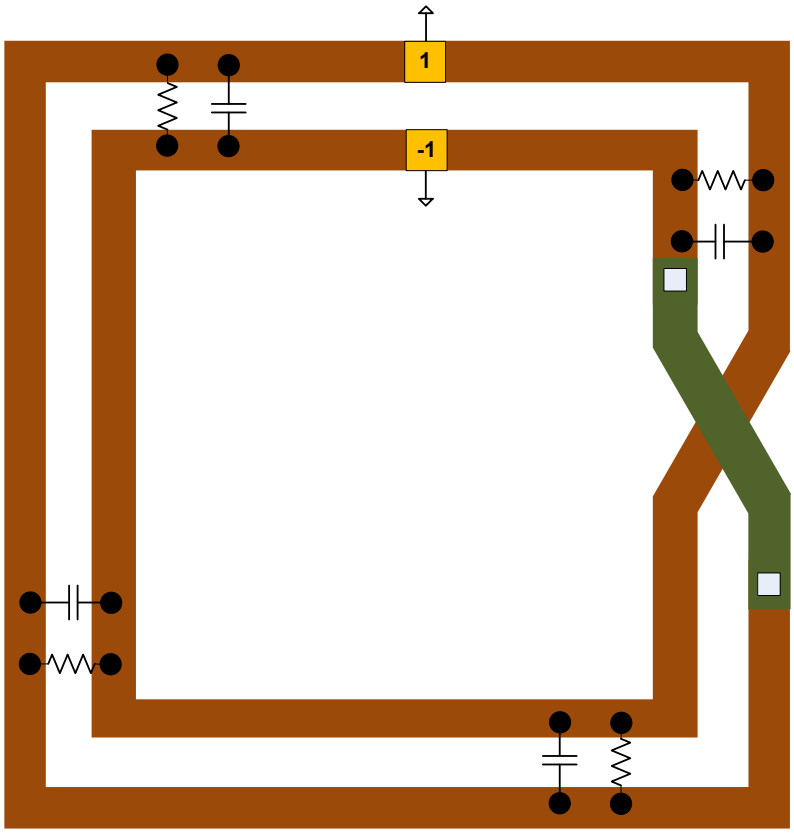


Figure 3.29. RTWO antenna

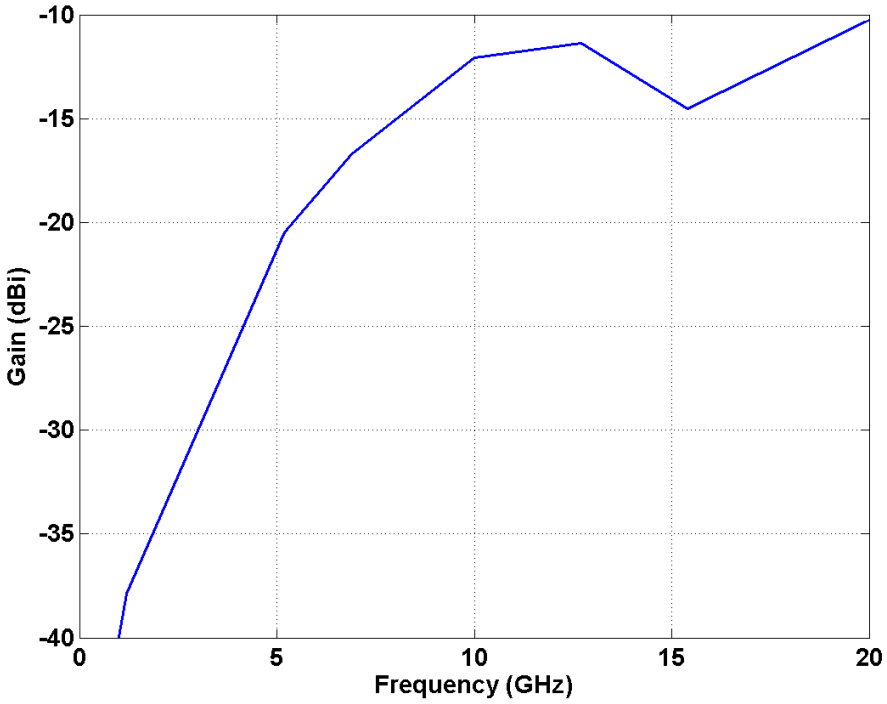


Figure 3.30. Loop antenna farfield plot

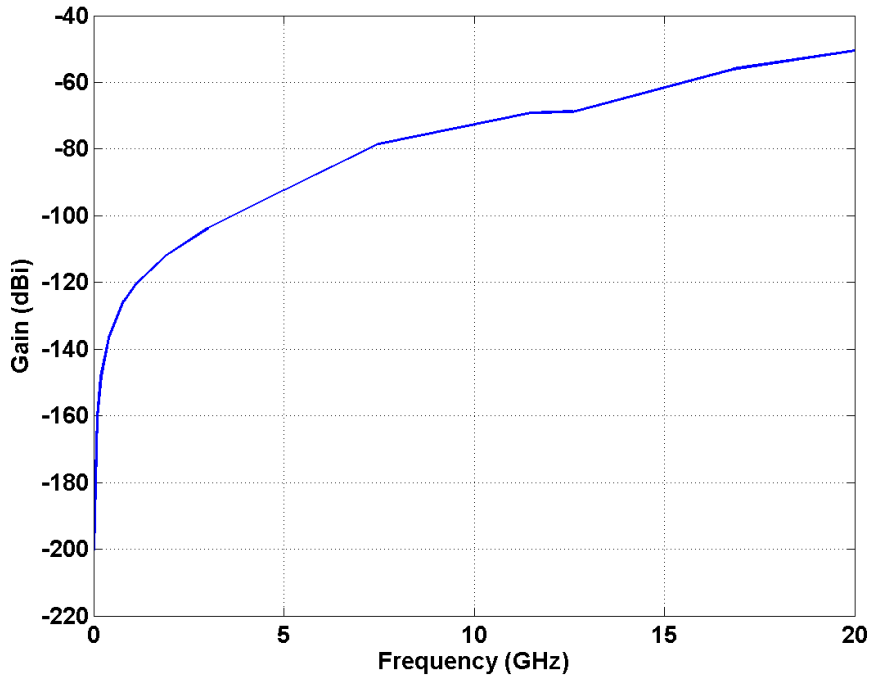


Figure 3.31. RTWO farfield plot for R=25 Ω

Figure 3.30 and Figure 3.31 clearly shows that far field radiation from RTWO is negligible. This is due to the differential excitation of the coupled transmission line where fields radiated from the coupled lines cancel each other.

CHAPTER 4

RTWO Design and Implementation

This chapter presents different designs and implementations of RTWO with novel features. Conventional CCIP is replaced with cross-connected N – and P – MOSFETS (CCNPP) that achieves low power and low phase noise RTWO implementation. Novel direction control approach is also presented. Parameters of RTWO design are verified by the prototype circuits implemented in 0.18 μm IBM RF CMOS process. Chip-on-board testing is used for silicon verification of the proposed RTWO circuits.

4.1 RTWO Implementation

The design and implementation of RTWO involved use of different software tools. Before schematic entry and subsequent layout, the transmission line is analyzed through EM simulation to extract the line parameters. Accuracy of the line parameter is essential in order to estimate the right operating frequency. Based on the objectives of this research different designs of RTWO were implemented. Table 4.1 lists the different designs with brief description and expected measurement results.

Table 4.1

RTWO Design Implementations

Design ID	Description	Measurement
R1	Octagonal RTWO with tuning – large ring	Frequency, power and phase noise
R2	Octagonal RTWO with tuning – small ring	Frequency, power and phase noise
R3	Meandered RTWO with tuning	Frequency, power and phase noise

Table 4.1

Cont.

R4	Octagonal RTWO with more CCIP stages, tuning – compared to R1	Power and phase noise
R5a	RTWO with conventional CCIP operating at the same frequency of R5b	Frequency, power and phase noise
R5b	RTWO with CCNPP – novel design for low power, low phase implementation	Frequency, power and phase noise
R6	RTWO for direction control using line offset	Frequency
R7	RTWO for direction control using CCIP with NAND gate	Frequency
Buffer	Broad band buffer for driving 50 Ω	Bandwidth, drive capability

RTWOs R1, R4, R3 and R4 were implemented with tuning capability. The coarse tuning control circuit is a 4 bit band switching array. Control circuit is typically implemented using MiM capacitors with switch logic. The effective loading capacitance with all the switches turned on is 4.6 pF. The dimension of RTWO (R1) and RTWO (R4) is approximately1-mm X 1-mm. The dimension of RTWO (R2) is approximately 0.65-mm X 0.65-mm. Implementation of RTWO (R1) and RTWO (R2) consists of eight sections of transmission line and CCIP. R1 and R2 section lengths are 460 μm and 300 μm respectively. RTWO (R4) has sixteen sections with a section length of 230 μm. The performance of RTWO (R4) is compared to RTWO (R1). An increase in the number of amplifier stages increases the harmonic content in the voltage. The

harmonic content also makes transition of the voltage waveform sharper, which helps to improve phase noise [5].

4.2 RTWO Design Components

4.2.1 Line Parameter Extraction. The design and implementation of RTWO leaves the designer with many options to choose from. Among these is the choice of transmission line implementation. Considerations in choosing metal layer and type of transmission line include attenuation, characteristic impedance and dimensions. The transmission line for the RTWO in this study was designed as a coupled microstrip line owing to the particularly useful characteristics such as easy implementation compared to other structures. The differential lines are typically fabricated on the top metal layer offering high quality factor [28]. A top conductor over dielectric, silicon substrate and ground plane, (metal-insulator-semiconductor-metal, MISM) is the structure in CMOS technology.

Interlayer dielectrics are multi-layer structure. The use of top metal layer minimizes the capacitance to the substrate. Another option other than MISM implementation profiles is the use of lower metal layer as a ground plane to shield the signal from the lossy semiconductor substrate, forming a metal-insulator-metal-semiconductor-metal (MIMSM) implementation profile.

Conventionally silicon-based integrated circuits have used aluminum conductors and silicon dioxide insulators between the conductors. Copper is an excellent electrical conductor but has some disadvantages in that it readily forms inter-metallic compounds with several semiconductors including silicon, and it has electro-migration problems. Copper with buffer layers of other metals is also being used [29].

The first step before RTWO design simulation is to extract the distributed RLGC parameter values of the line. EM simulators such as Ansoft HFSS and CST Microwave Studio have features that can easily generate the equivalent RLGC lumped parameters of the transmission line. An alternate solution is to obtain S-parameter data and curve fit it to an RLGC network. The later was used to derive parameter values. First step is to develop a substrate profile consistent with the metal stack and dielectric layers of the targeted CMOS technology. Figure 4.1 shows the substrate used for transmission line section layout. Section length is 300 µm. Line width and spacing is 10 µm and 20 µm respectively. Agilent ADS layout EDA is a 2.5D EM simulator that extracts S-parameters using the principle of method of moment (MoM).

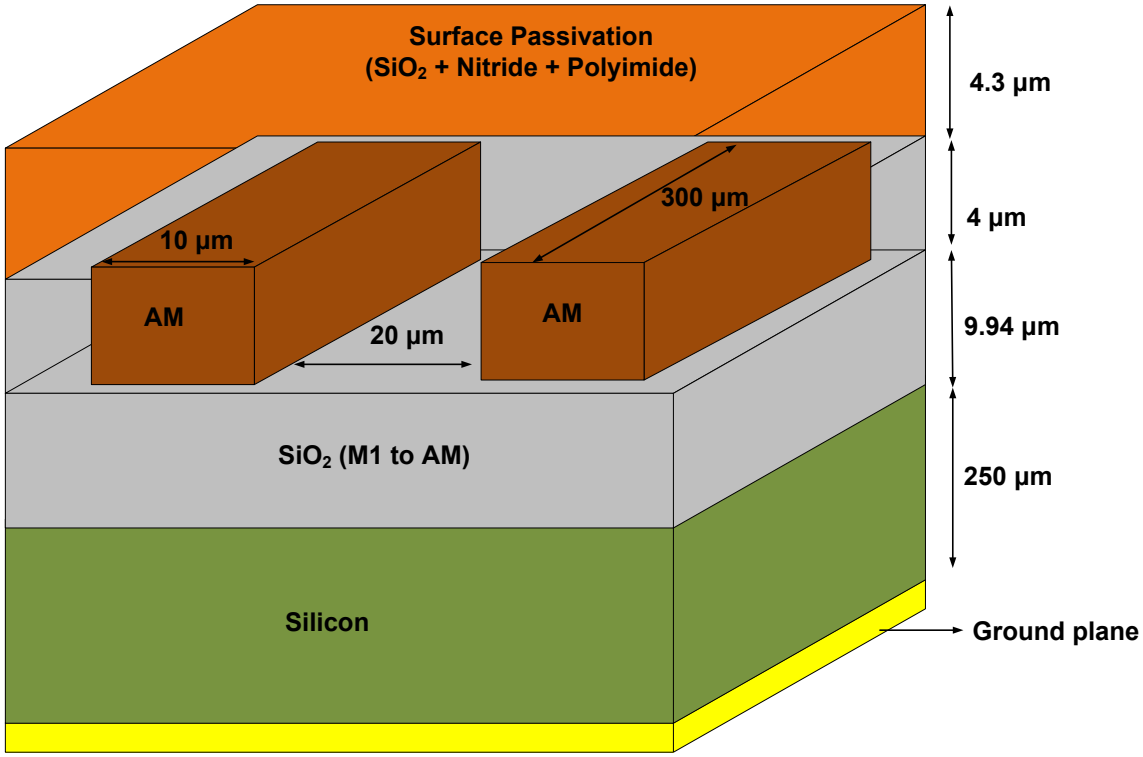


Figure 4.1. Silicon substrate, oxide, metal layers used in section layout

Figure 4.2 and 4.3 show the S-parameter results from ADS momentum simulation for reflection and transmission coefficients respectively.

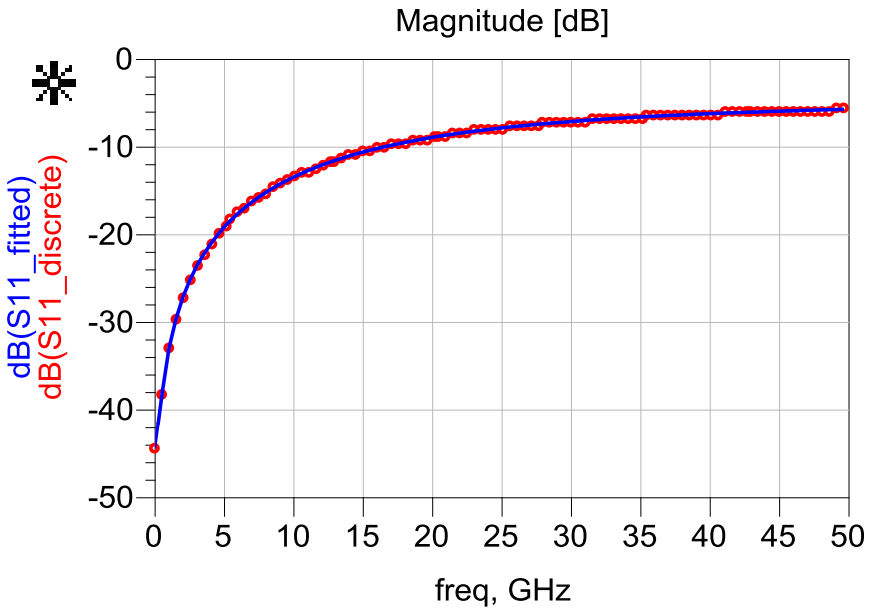


Figure 4.2. S-parameter data –Method of Moment (MoM)

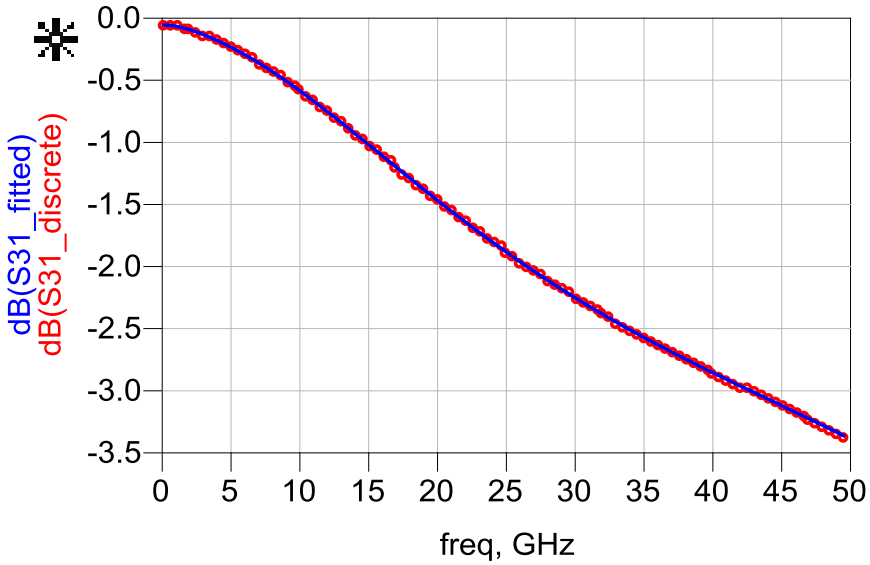


Figure 4.3. S-parameter data –Method of Moment (MoM)

S-parameters from MoM simulation is curve fit to ten sections of RLGC. Curve fitting involves an optimization of goal expressions that reduces the error between EM solution's S-parameters and the RLGC S-parameters. The optimization algorithm is a combination of least

Pth and gradient. The Least Pth uses the Quasi-Newton search method and finds a global solution whereas gradient finds a local solution. Increasing the number of RLGC sections improves the accuracy of approximating the distributed characteristics of the line to an RLGC network. As shown in Figure 4.4, the approximation error is about 1% at the frequency of interest (3.9 GHz). Figure 4.5 shows a close match between the S-parameters of RLGC model and EM solution on a smith chart.

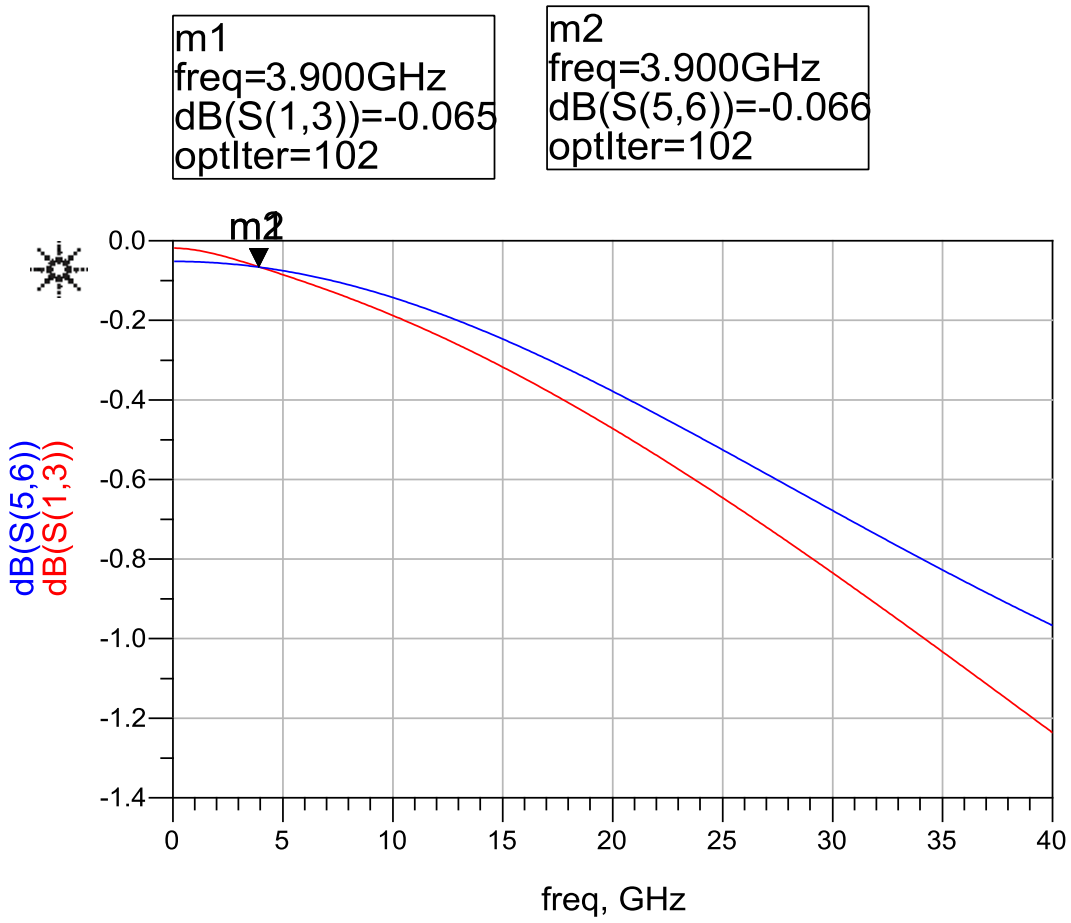


Figure 4.4. Curve fitting for extraction of RLGC line parameters – dB scale

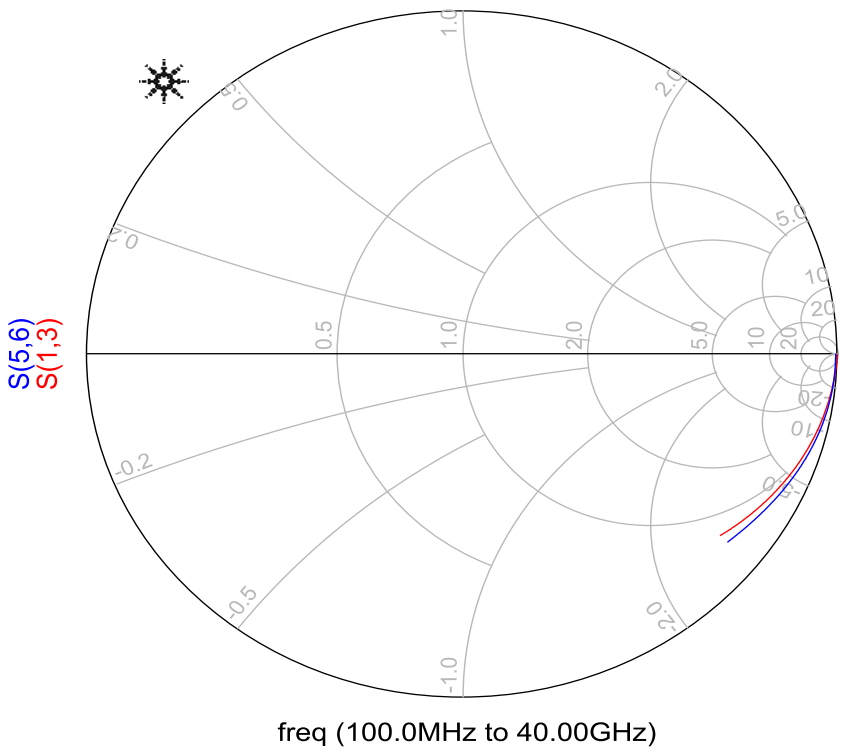


Figure 4.5. Curve fitting for extraction of RLGC line parameters – Smith chart

Table 4.2 lists the extracted parameters of the RLGC per unit length shown in Figure 4.6.

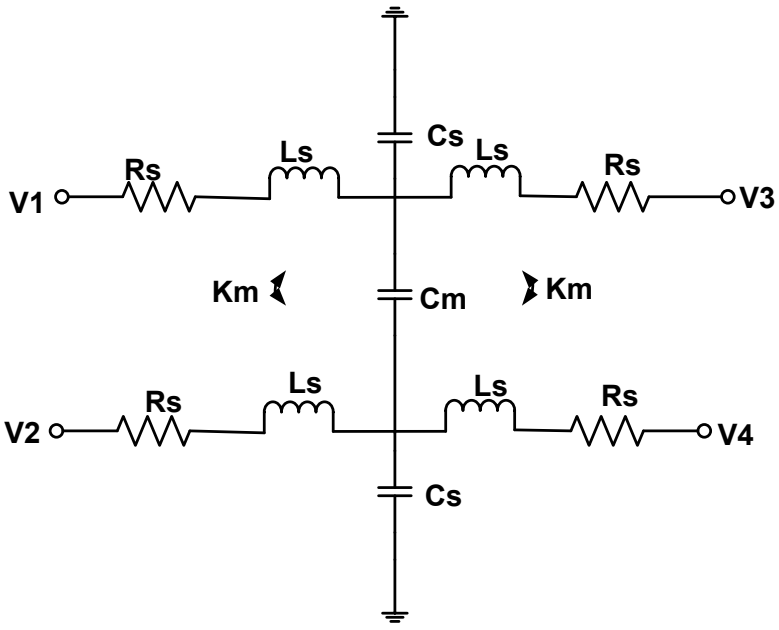


Figure 4.6. RLGC segment

Table 4.2

Normalized Extracted Parameters of Microstrip Line Segment

Line Parameters	
Rs (Ω/m)	966.66
Lm (nH/m)	390
Cs (pF/m)	51.67
Cm (pF/m)	33.52
Km	0.48

Characteristic impedance was calculated as 57 Ω.

4.2.2 Amplifier stage. The conventional CCIP was used for implementing RTWO circuits with the exception of RTWO (R5b). Figure 4.7 shows CCIP circuit.

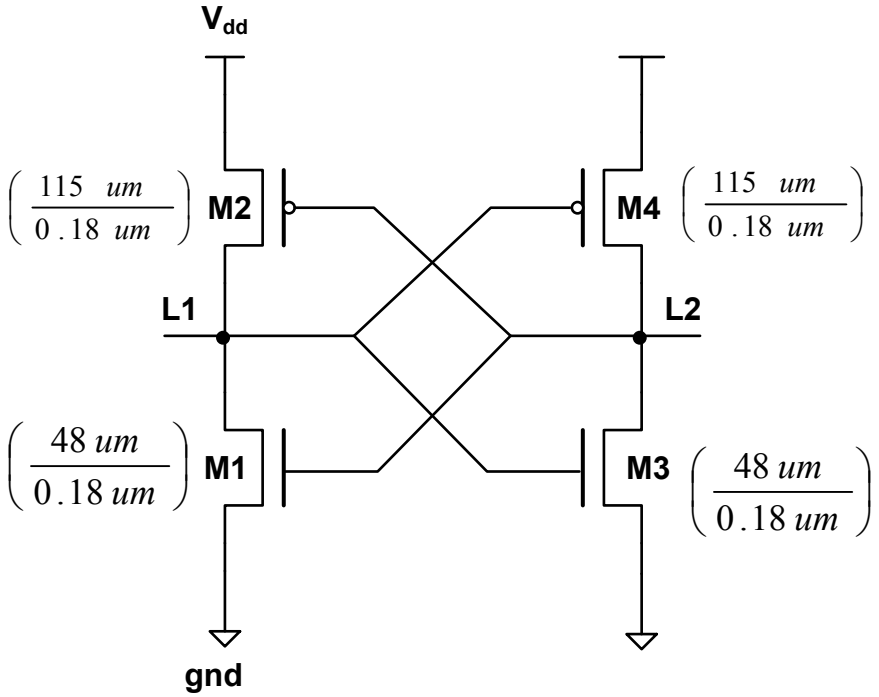


Figure 4.7. CCIP circuit

The total transconductance was calculated as 160 mS for RTWOs R1, R2, R3 and R4. The transconductance per each section for an eight section RTWO was 20 mS. The transistors were properly sized to guarantee oscillation.

4.3 Novel RTWO with CCNPP

Compared to traditional LC oscillators, one major drawback of RTWO is high power consumption. To minimize power consumption, a cross connected NMOS-PMOS pair (CCNPP) is proposed as the gain stage for the RTWO. The proposed concept is validated by X-band RTWOs using conventional and proposed gain stages. The proposed circuit consumes 30 mW with the phase noise of -98.2 dBc/Hz at 1MHz offset compared to 38 mW with the phase noise of -87.3 dBc/Hz for the conventional circuit. To operate both structures at the same frequency, much larger ring was used. Despite driving a larger ring, RTWO with CCNPP consumes less power.

In terms of power consumption, Benabdeljelil et al [30] compared an RTWO VCO and an LC VCO operating at 12 GHz. LC VCO consumed 8mW whereas RTWO VCO consumed 30mW (~ 4 times more power consumption). In [31] it was demonstrated that 80% of the power consumption in RTWO is generally attributed to losses in the transmission line using partial element equivalent circuit (PEEC) extraction. This approximation is consistent with cases where the time of flight of the transmission line is much larger than the propagation delay of the gain stage. For high frequency implementations such as mm-waves the gain stage tends to dominate the overall power consumption. The CCNPP implementation of the gain stage is ideal at such frequencies and design conditions. With this technique, we can reduce power consumption by 20% or more. Figure 4.8 shows two simulated RTWOs, one (A) with longer transmission line and the other (B) with a shorter transmission line.

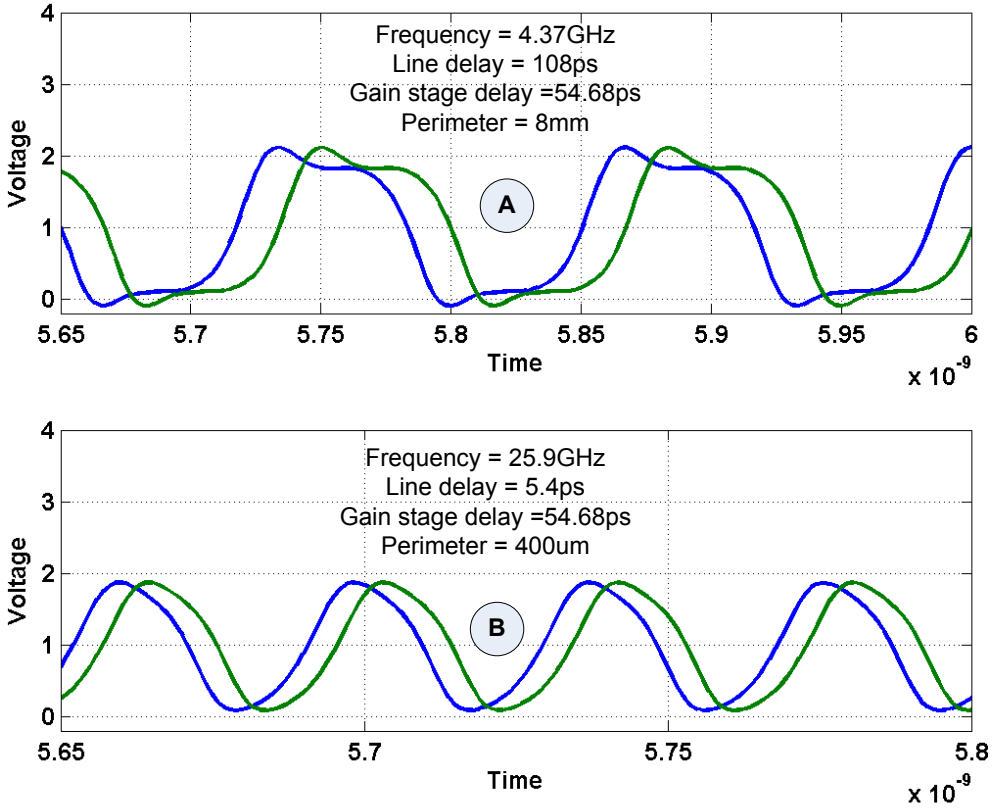
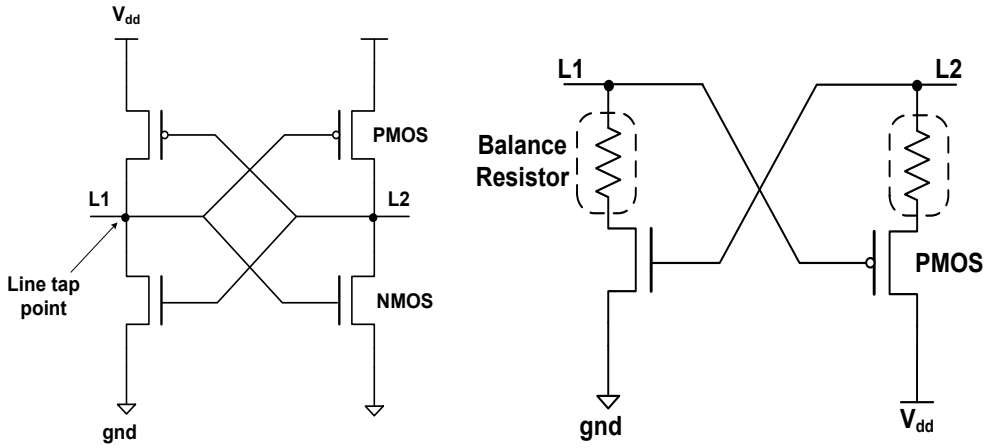


Figure 4.8. Simulated waveform comparison between two RTWOs (A) Line delay dominated oscillation (B) Gain stage delay dominated oscillation

Line delay of (A), 108 ps, is almost twice the gain stage delay, 54.68 ps. On the other hand, line delay of (B), 5.4 ps, is almost 10% of the gain stage delay (54.68 ps). RTWO (A) produces near square wave signals while RTWO (B) produces near sinusoidal signals. We intentionally used the same gain stage in both RTWOs. In practice one would use a gain stage with much less propagation delay for the RTWO (B).

4.3.1 Gain stage. The gain stage of most RTWOs reported in literature use the traditional CCIP as shown in Figure 4.9(a). Figure 4.9(b) shows the CCNPP implementation of the gain stage.



(a) (b)

Figure 4.9. (a) Traditional CCIP (b) CCNPP

CCNPP consists of single NMOS and PMOS transistors with balance resistors. The purpose of the balance resistor is to operate the gain stage in the current-limited mode as described in Wang, et al [32].

4.3.2 Analysis of power consumption. In Power consumption in RTWO is the sum of contributions from transmission line and CCIP. For large clock arrays, the line accounts for a greater percentage of power (PTline) and is expressed as [15]:

$$P_{Tline} = \frac{{V_{dd}}^2}{{Z_0}^2} \times R_{loop} \tag{4.1}$$

where V_{dd} is the supply voltage, R_{loop} is line resistance and Z_0 is the characteristic impedance of line. Gain stage power consumption typically has three components. Static power consumption is negligible. Dynamic power during switching is recycled and becomes transmission line energy, which is circulated in the closed electromagnetic path [1]. Dynamic short-circuit power cannot be ignored and is consumed when both NMOS and PMOS are on during switching. Assuming no large capacitive loading, this power (Psc) is expressed as:

$$P_{sc} = \frac{I_{peak} V_{dd} (t_r + t_f)}{T} \quad (4.2)$$

where I_{peak} is the saturation current of either PMOS or NMOS transistor, tr and tf is the rise and fall times and T is the period of the signal. Another power component arises when gain stage is in idle state. This is due to the ON resistance of NMOS and PMOS transistors [31] and is significant in estimating the overall power consumption.

4.3.3 Large Signal Analysis of the Gain Stages. Figure 4.10 shows one of the output line currents of a CCIP and CCNPP as a function of the line voltage. The plot validates the negative resistance behavior of both circuits within a range of the line voltage.

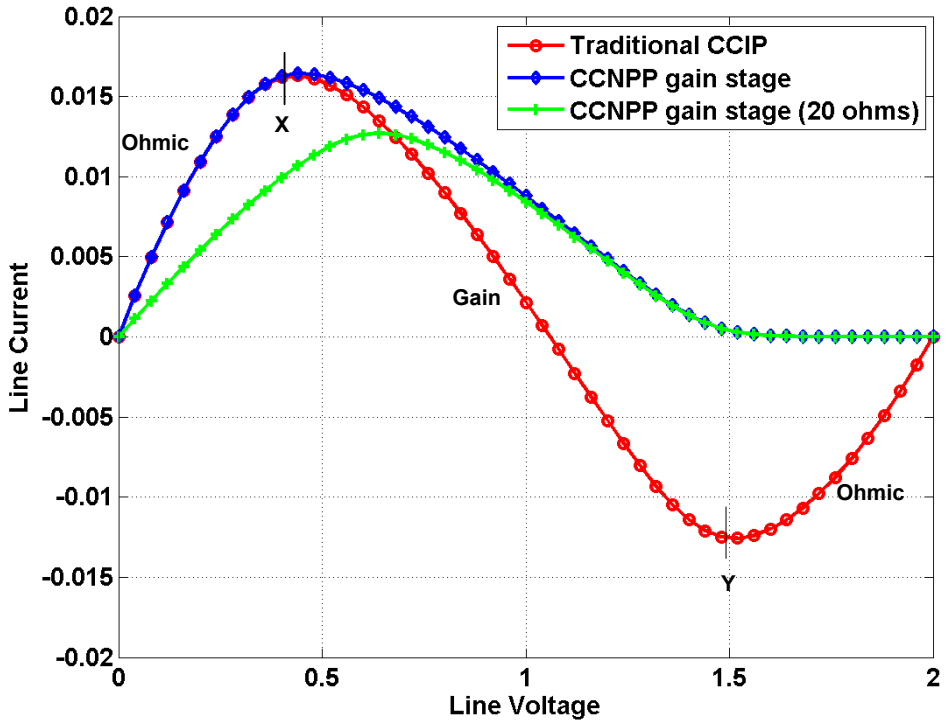


Figure 4.10. Large signal response of gain stage

As seen in Figure 4.10, the points marked X-Y represents the gain region or negative resistance region between 0.48 V to 1.5 V of the line voltage. Both traditional CCIP and CCNPP provide the necessary transconductance (*gm*) for amplification. After point Y or

switching, both circuits assume a relaxation state momentarily before heading towards the opposite rail. Whereas CCIP consumes current in this idle state (current changing from 12 mA to 0) the CCNPP gain stage consumes almost zero current. Power consumption due to ON resistance is reduced as a result. Additional savings arise from elimination of the short circuit current in the traditional CCIP.

4.3.4 Design implementation. Transmission lines were implemented using microstrip transmission lines on silicon substrate. The extracted line parameters are summarized in Table 4.3. To compare traditional and the proposed RTWOs identical transistor sizes were used in both circuits. To achieve the same operating frequency, we had to increase the transmission line length due to reduced parasitic capacitances of the proposed RTWO. NMOS transistors are 48 μm wide and 0.18 μm long. PMOS transistors are 115.2 μm wide and 0.18 μm long. Eight gain stages were distributed evenly around the line. Measurement results are discussed in Chapter 5.

Table 4.3

Extracted Parameters of Microstrip Line Segment

Traditional RTWO Design (R5a), section length = 110 μm		RTWO with CCNPP (R5b), section length = 200 μm	
Parameter	Value	Parameter	Value
R	0.214 Ω	R	0.404 Ω
L	96.588 pH	L	193.94 pH
G	50 uS	G	100 uS
C	11.416 fF	C	22.746 fF

4.4 Direction Control Design – External Control

The control of wave propagation direction in RTWO is important for applications in synchronous circuits and poly-phase mixer applications. Ideal RTWO structure is perfectly symmetric. The rotary direction is typically a result of imperfections in the RTWO structure introducing different resistance paths together with the initial power up state of the RTWO. Rotary direction can be clockwise or counterclockwise depending on the mismatches. This section presents novel circuit techniques for direction control of RTWO.

4.4.1 Proposed direction control circuits. Several schemes have been proposed for the rotary direction control, such as power up sequence of amplifier stages [15]. In the power up sequence technique, it is assumed that oscillation starts at the point of crossover of the coupled transmission line. The direction of wave propagation is controlled by setting different power-on times of CCIPs. When oscillation starts, the direction with low impedance is selected. With different power-on times, some of the CCIPs begin to work as negative resistance elements compensating for the energy loss before others. The buildup of negative resistance defines the direction of propagation. Figure 4.11 shows the proposed direction control circuit.

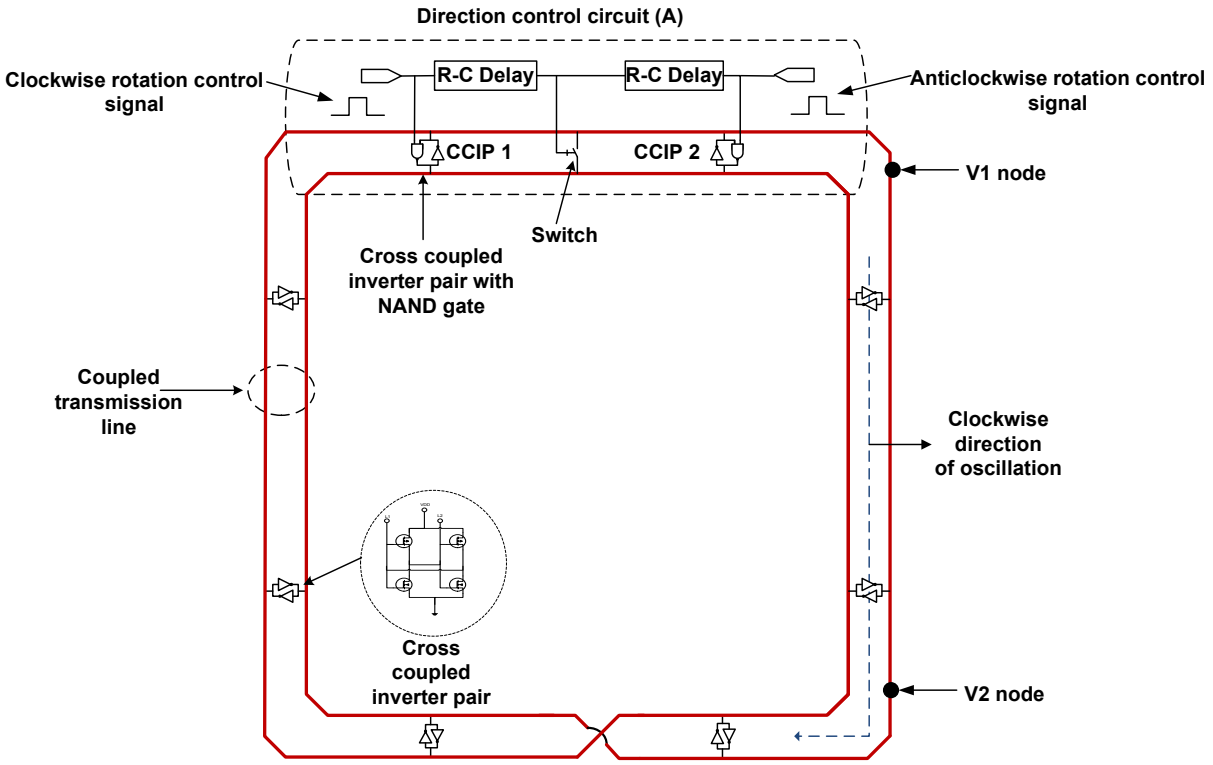


Figure 4.11. Proposed direction control circuit with external control signal

The technique consists of a control signal, typically a pulse, delay element, switch, and two cross-coupled inverters implemented with NAND gates labeled as CCIP1 and CCIP2. The switch is connected half way between CCIP1 and CCIP2 and is optimized to ensure that the phase it introduces after oscillation is negligible. A NAND gate behaves as an inverter if one of the input is stuck to logic 1, thus the negative resistance of CCIP1 sets in to amplify the signal and gets latched before CCIP2. The delay each R-C stage introduces is 185ps. Switch is turned on 185ps before oscillation begins to stabilize. The switch ensures maximum negative reflection to both forward and backward traveling wave momentarily creating a standing wave. As the switch gets turned off, the standing wave changes to a traveling wave. CCIP1 and CCIP2 behave as a normal CCIP in traveling wave mode. A latched state is level sensitive and an attempt by the equal backward energy to cause a further switching into the state to which they

have switched will be resisted due to self-locking directivity of the amplifier. The direction of oscillation is clockwise if CCIP1 control line is asserted first and would be anticlockwise if the control line of CCIP2 is asserted first. Compared to other direction control schemes, this technique offers fast startup and robust control of the wave rotary direction.

4.4.2 Simulation results. Figure 4.12 shows the various traveling modes, direction assert signal and external control signal. When control signal is high (2V), switch is turned off, which produces either clockwise or anticlockwise traveling wave.

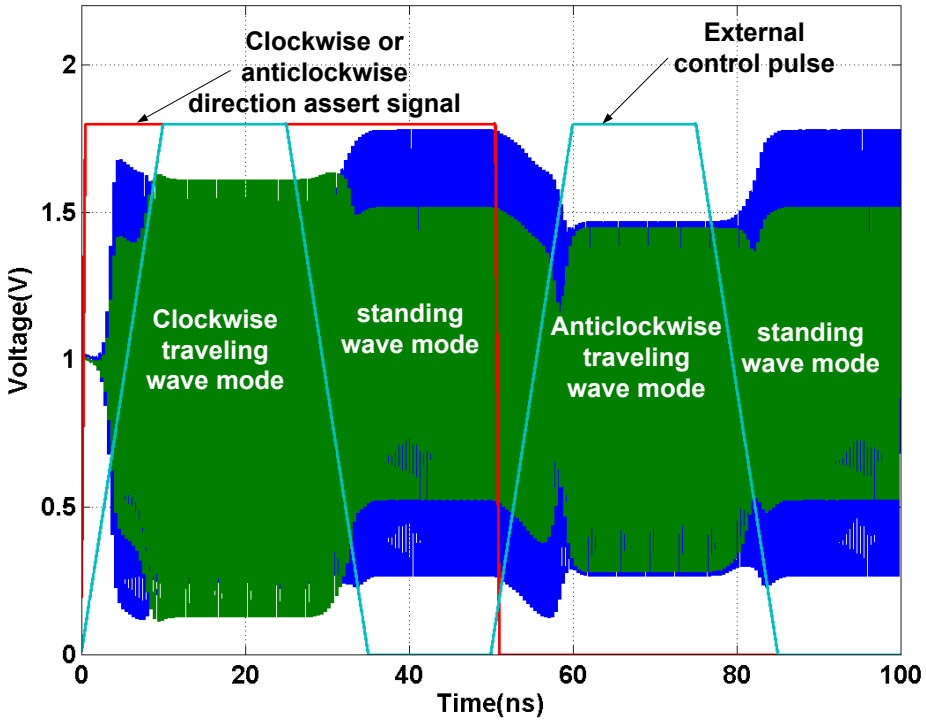


Figure 4.12. Direction control simulation with external logic

As the direction assert signal changes from high (2V) to low (0V), traveling mode changes from clockwise to anticlockwise as shown in Figure 4.13 and 4.14 respectively. Figure 4.15 shows the standing wave mode which is produced when external control signal switches from high to low.

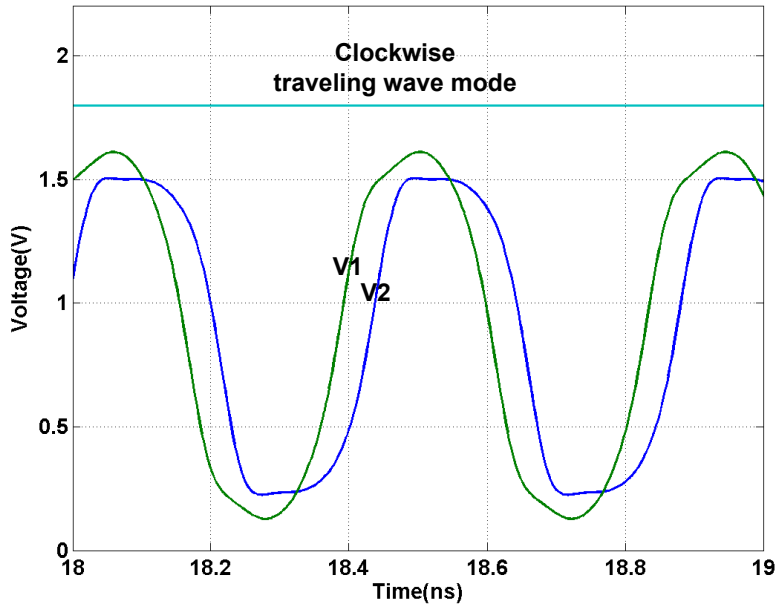


Figure 4.13. Clockwise traveling wave mode

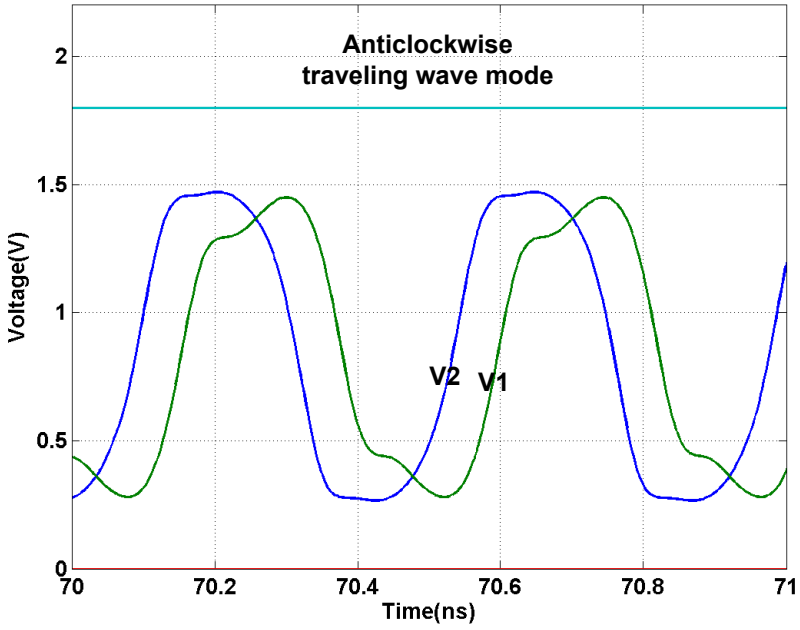


Figure 4.14. Anticlockwise traveling wave mode

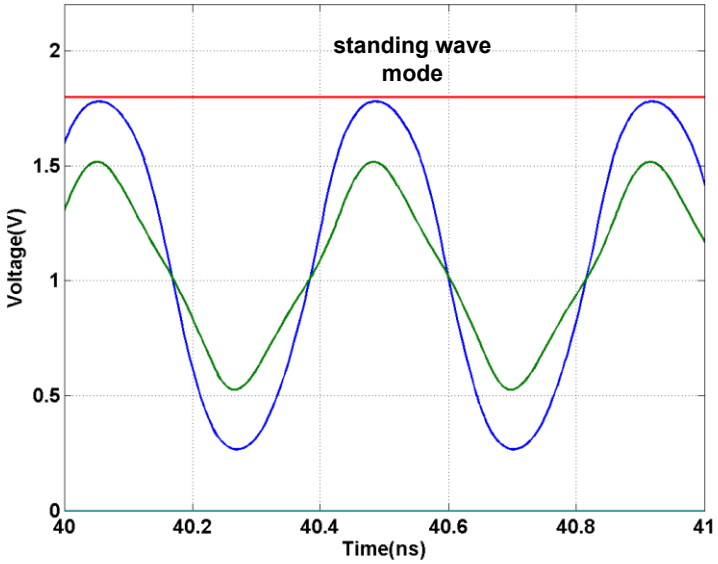


Figure 4.15. Standing wave mode

4.5 Direction Control Circuit Based on Transmission Line Offset

Figure 4.16 shows the proposed direction control circuit based on transmission line offset. Normally, the input of one inverter is electrically shorted to the output of the other whereas in the offset CCIP, input and output are connected through a short segment of a transmission line as shown in Figures 4.16 and 4.17.

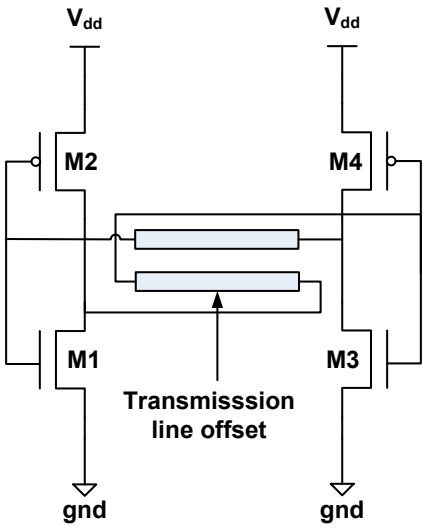


Figure 4.16. Offset CCIP for clockwise propagation

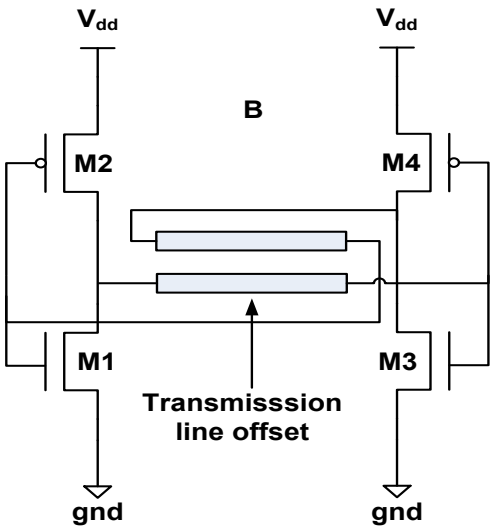


Figure 4.17. Offset CCIP for anticlockwise propagation

Figure 4.18 shows section of RTWO (R7) where offset is implemented. The selection of section is arbitrary. Figure 4.19 shows the block diagram for the complete circuit.

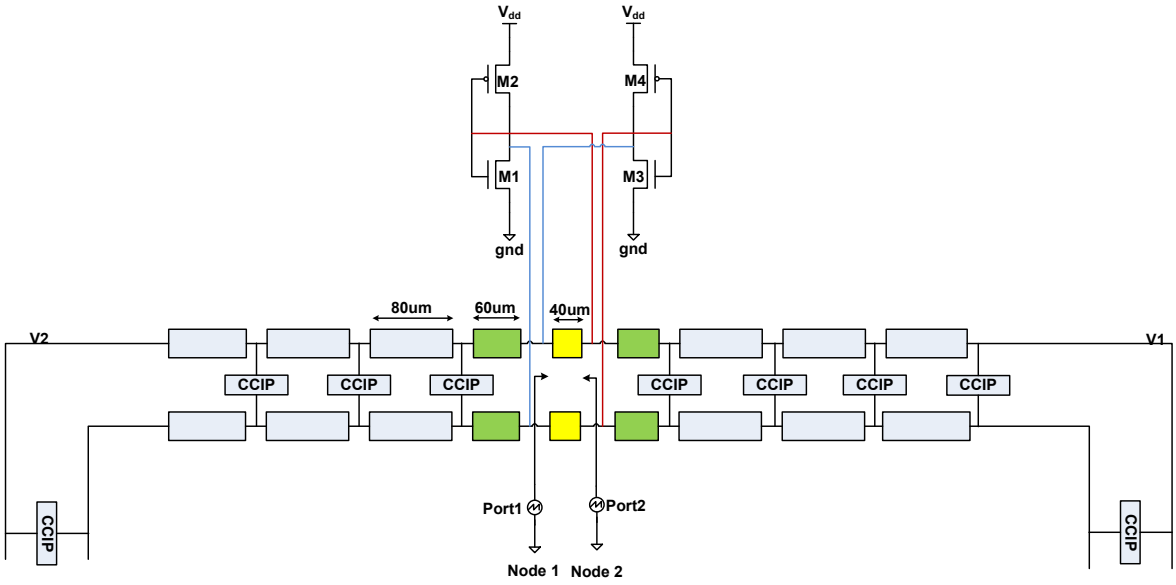


Figure 4.18. Section of block diagram where offset is implemented

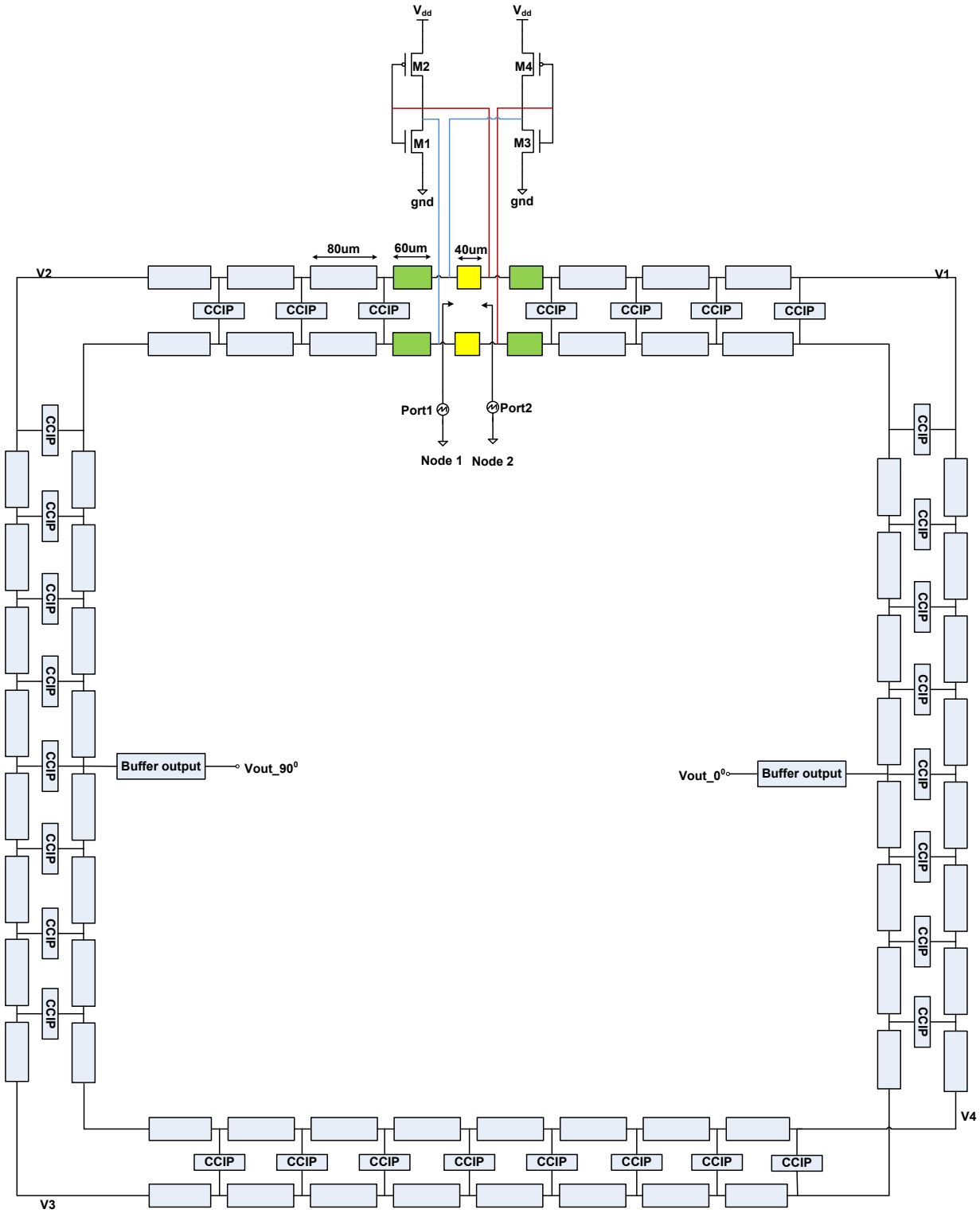


Figure 4.19. Schematic block diagram for offset direction control technique

The offset interconnect has distributed properties thus the voltage at node 1 is not electrically the same as node 2 but differ by a phase. Oscillation begins with noise which get filtered and amplified into steady state oscillation. The spectrum of white noise is flat whose frequency components range from that of radio waves to infrared radiation. To understand the impact of offset interconnects, the attenuation of a small signal injected at node 1 is compared to node 2. S-parameter simulation first linearizes the CCIP in gain mode. A periodic form is assumed. Port 1 and 2 injects small signals at nodes 1 and 2 respectively. Figure 4.20 compares S_{12} to S_{21} from DC to the calculated cutoff frequency of the offset interconnect for the schematic block diagram in Figure 4.19. The difference in attenuation is shown in Figure 4.21.

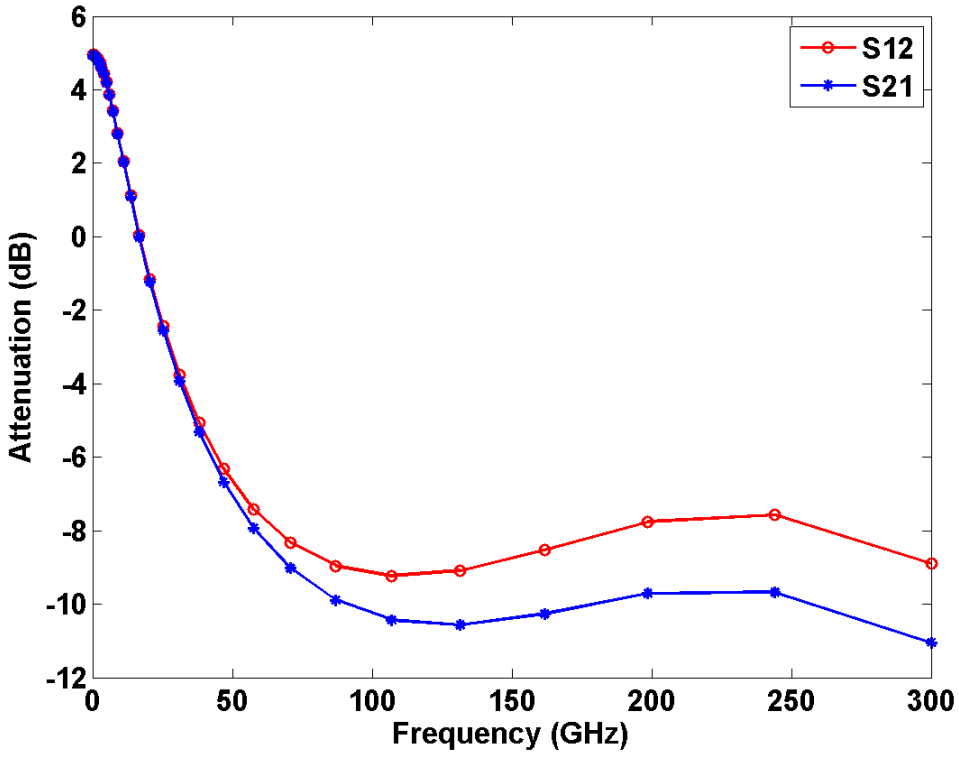


Figure 4.20. Offset CCIP S-parameter simulation

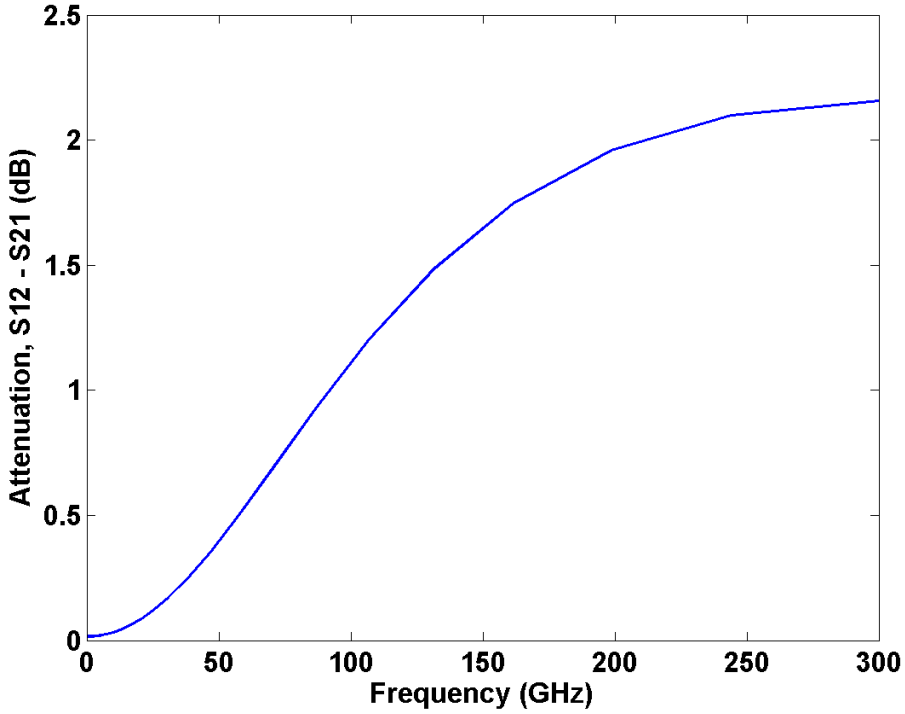


Figure 4.21. Attenuation difference between S_{12} and S_{21}, ($S_{12} - S_{21}$)

Figure 4.21 reveals that the power attenuation from node 2 to node 1 is smaller than from node 1 to node 2. Figure 4.22 shows the offset CCIP section annotated with the clockwise (CW) and anticlockwise (ACW) traveling waves.

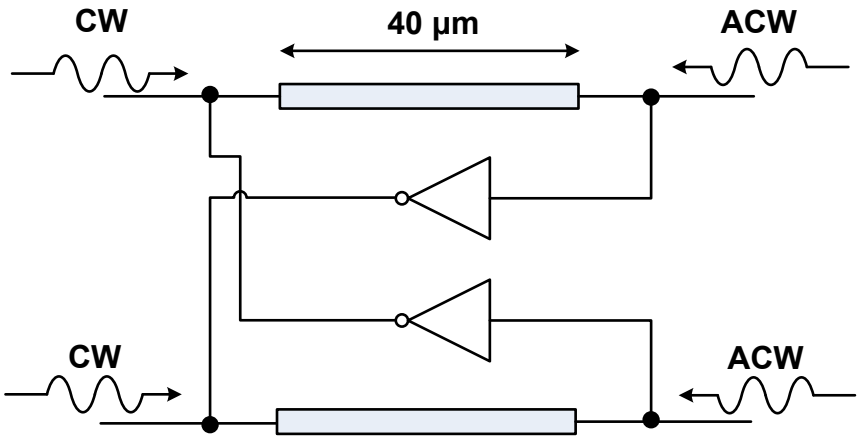


Figure 4.22. Offset CCIP with wave annotation

ACW traveling wave signal reaches the input of the inverter gates first and are amplified whereas CW signal reaches the output of the gates and are reflected. The direction is determined by the small signal that excites the input of the inverter first. The block diagram in Figure 4.19 implements wave propagation in the anticlockwise direction.

To observe the direction of wave propagation, clock nodes V_1, V_2, V_3 and V_4 were tapped. The offset CCIP in Figure 4.16 produces the waveform in Figure 4.23 whereas that in Figure 4.17 produces the waveform in Figure 4.24. The optimal length of the offset is determined by the degree to which it's able to overcome any mismatches and the phase difference it introduces. In this case, offset length was chosen as one-half (1/2) of the segment length. Maximum offset length is determined by the section length and should be such that the asymmetry it introduces is minimal.

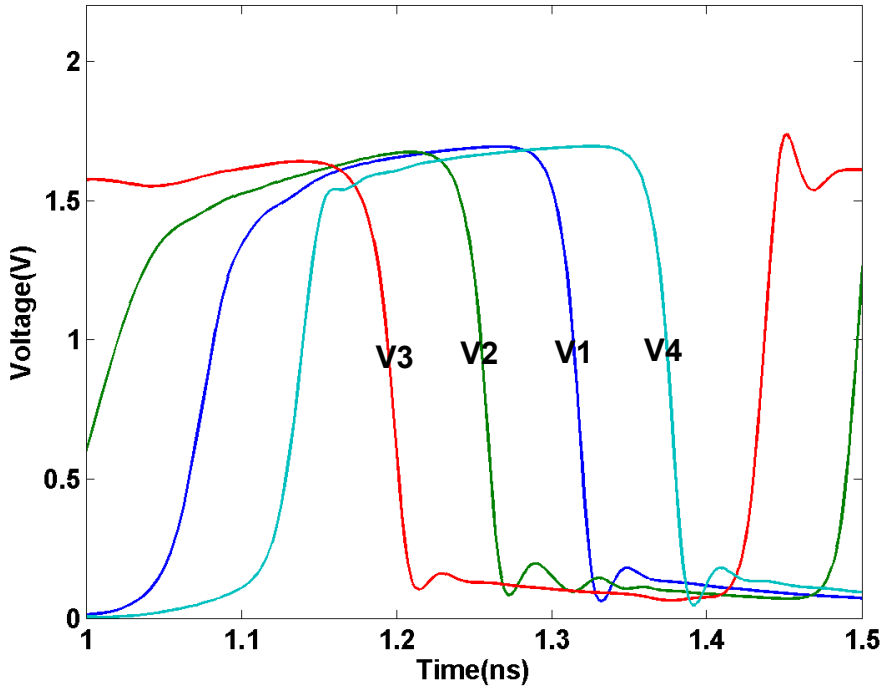


Figure 4.23. Clockwise Propagation

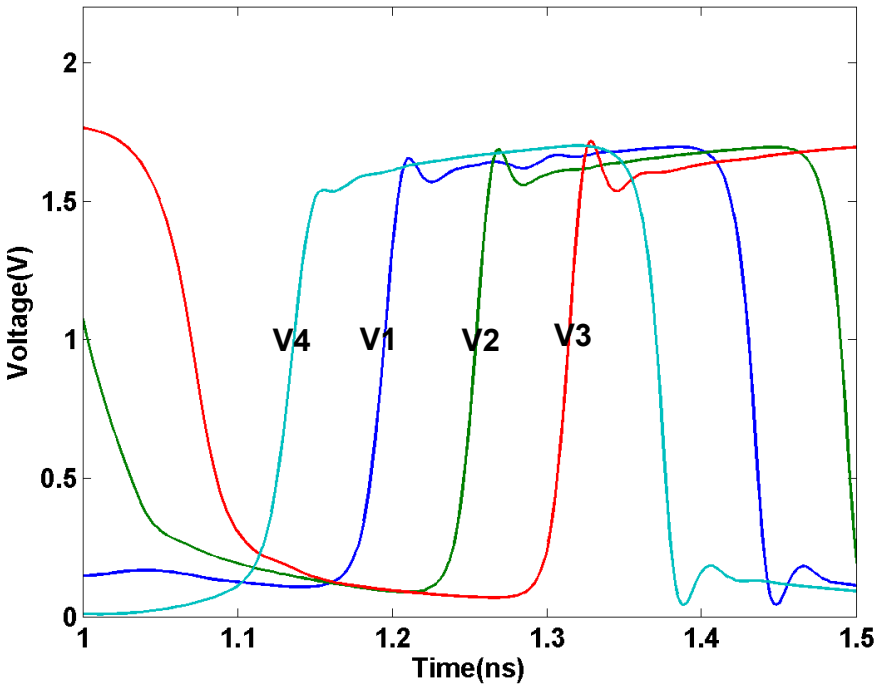


Figure 4.24. Anticlockwise Propagation

4.6 Buffer Design

Buffer is a fundamental building block in analog IC design circuit. If the analog circuit is intended to drive a small purely capacitive load, the output buffer is not used. For a 50 Ω or large capacitive load, a buffer is typically needed to drive the load. Output buffer have a large bias current which reduces the output resistance. Most output buffers have a high current and low voltage gain. With low voltage gain, most output buffers have wide bandwidth driving capability.

In this section we present a modified push-pull shunt feedback output amplifier by cascading it with a single stage current mode logic (CML) stage to extend the bandwidth to GHz range. Resistive load drive capability ranges from 50 to 80 Ω. Capacitive drive is not as good as resistive drive and ranges from 500 f to 1 pF. The bandwidth degrades as the capacitive load increases. Bandwidth extension techniques such as cascading of multiple amplifiers and

shunt peaking provides alternate solutions. Shunt peaking employs inductive elements that require large area [6]. Other designs include chain of tapered CML buffers by Payam et al [33]. Capacitive voltage divider technique is used to bias the second stage, thus the negative feedback amplifier stage does not require an explicit biasing circuit.

4.6.1 Push-Pull Amplifier with Feedback. Negative feedback has been proven to be useful in lowering the output resistance of a CMOS output stage. This technique is used in push-pull output amplifiers to complement the high power efficiency (~78.5%) by lowering the output resistance for maximum power transfer [34]. Figure 4.25 shows the push-pull amplifier circuit with resistive feedback.

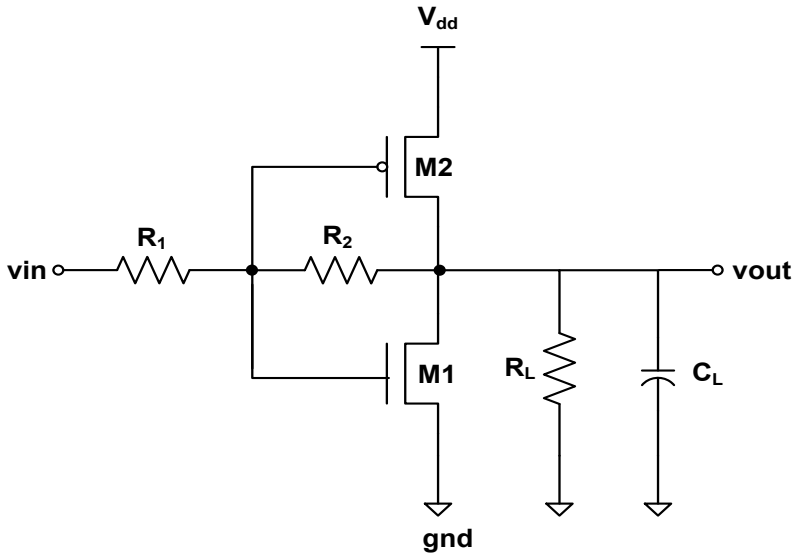


Figure 4.25. Push pull amplifier

The loop gain is given:

$$Loop\ gain \approx \frac{R_1}{R_1 + R_2}\left(\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_L}\right) \tag{4.3}$$

Output resistance is given by:

$$R_{out} = \frac{r_{ds1} \parallel r_{ds2}}{1 + \frac{R_1}{R_1+R_2}\left(\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+g_L}\right)} \tag{4.4}$$

Typically resistance R_2 is larger than R_1 (~2 times) so that the output signal swing is not maintained by the input signal. Figure 4.26 shows the simulated frequency response of a push pull with resistive feedback connected to 50 Ω load. -3dB bandwidth is 600 MHz.

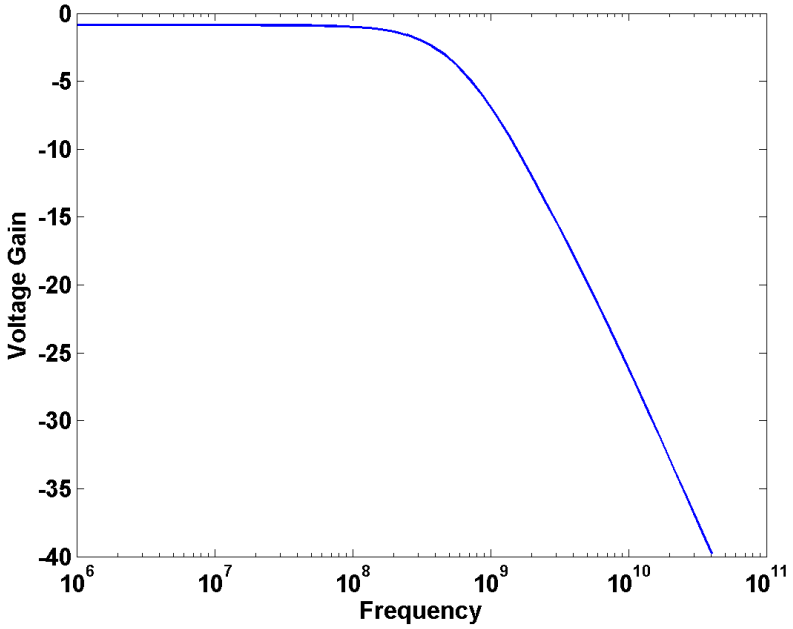


Figure 4.26. Simulated bandwidth

The shape of the bode plot in Figure 4.26 can be understood by finding the poles and zeros of the push pull amplifier [34]. The pole (p_1) and zero (z_1) is given by:

$$p_1 = -\frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L} \tag{4.5}$$

and

$$z_1 = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} \tag{4.6}$$

If $z_1 \gg |p_1|$ then:

$$\omega_{-3dB} = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L} \quad (4.7)$$

The position of the zero in the right half plane can by altered by the value of R_2 by moving it to the left hand plane for pole zero cancellation. Table 4.4 list the parameters of push pull amplifier that was used for simulation.

Table 4.4

Push Pull Amplifier Parameters

Specification	Value
V_{supply}	1.8 V
W/L_1 (NMOS)	96 µm/0.18 µm
W/L_2 (PMOS)	192 µm/0.18 µm
R_1	1 KΩ
R_2	2 KΩ
R_L	50 Ω
C_L	≈0pF

The calculated output resistance of push pull amplifier and push pull resistive feedback amplifier is 176 Ω and 33.34 Ω respectively.

4.6.2 Modified feedback amplifier. To extend the bandwidth we precede the push pull stage with a CML stage with miller capacitance (C_M). C_M capacitor introduces a zero which extends the bandwidth before roll-off. Amplifier stages are connected together through a coupling capacitor whose value determines the voltage swing at the input of the push pull stage. The coupling capacitor (C_c) shape the buffer into a band pass filter by introducing high impedance at low frequencies. Complete circuit is shown in Figure 4.27.

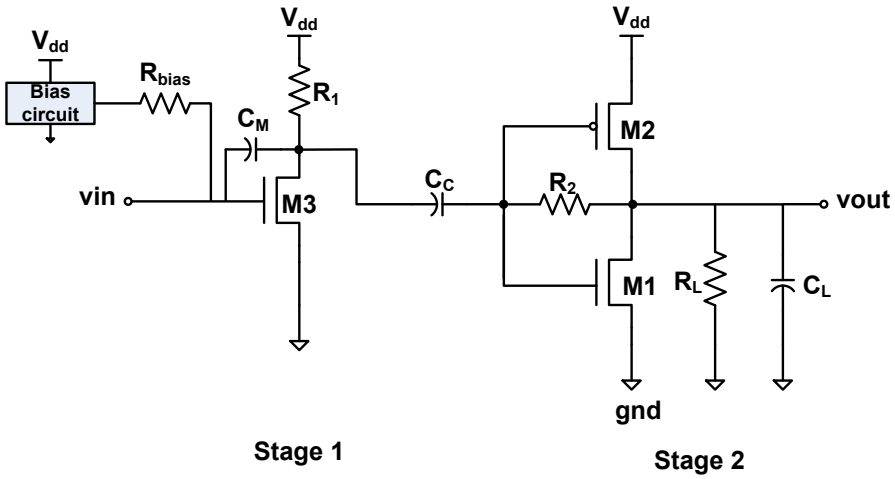


Figure 4.27. Complete single ended buffer circuit

Table 4.5 list the parameters of push pull amplifier that were used for simulation.

Table 4.5

Buffer Parameters for Complete Circuit

Specification	Value
V_{supply}	1.8 V
W/L_1 (NMOS)	96 um/0.18 um
W/L_2 (PMOS)	192 um/0.18 um
W/L_3 (NMOS)	4.8 um/0.18 um
R_{bias}	20 KΩ
R_1	1 KΩ
R_2	2 KΩ
R_L	50 Ω
C_C	5.3 pF
C_M	500 fF
C_L	≈ 0 pF

Figure 4.28 shows frequency response of push pull amplifier with coupling capacitor compared to the complete buffer circuit. Table 4.6 shows the simulated buffer performance.

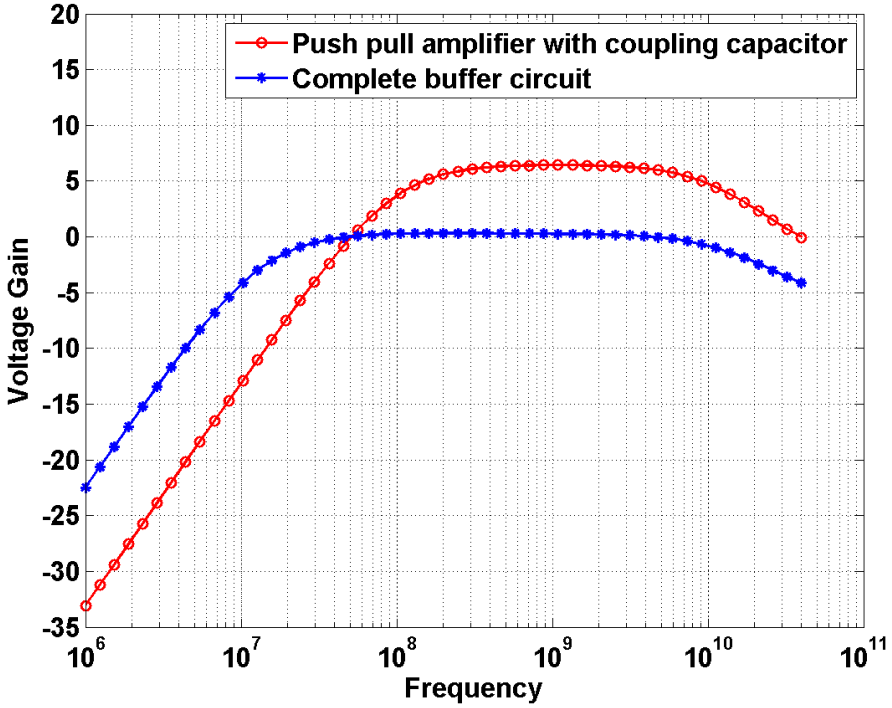


Figure 4.28. Bandwidth comparison between capacitor coupled push pull amplifier and buffer circuit

Table 4.6

Simulated Buffer Performance

Performance measures	
Voltage gain	≈ 0 dB
Current consumption	15 mA
Input capacitance	476.5 fF
Bandwidth	25 GHz
Output resistance	33.33 Ω

CHAPTER 5

Measurement Results

5.1 Fabricated Chip

The layout of the RTWO chip is shown in Figure 5.1. The RTWO designs and buffer circuit are highlighted.

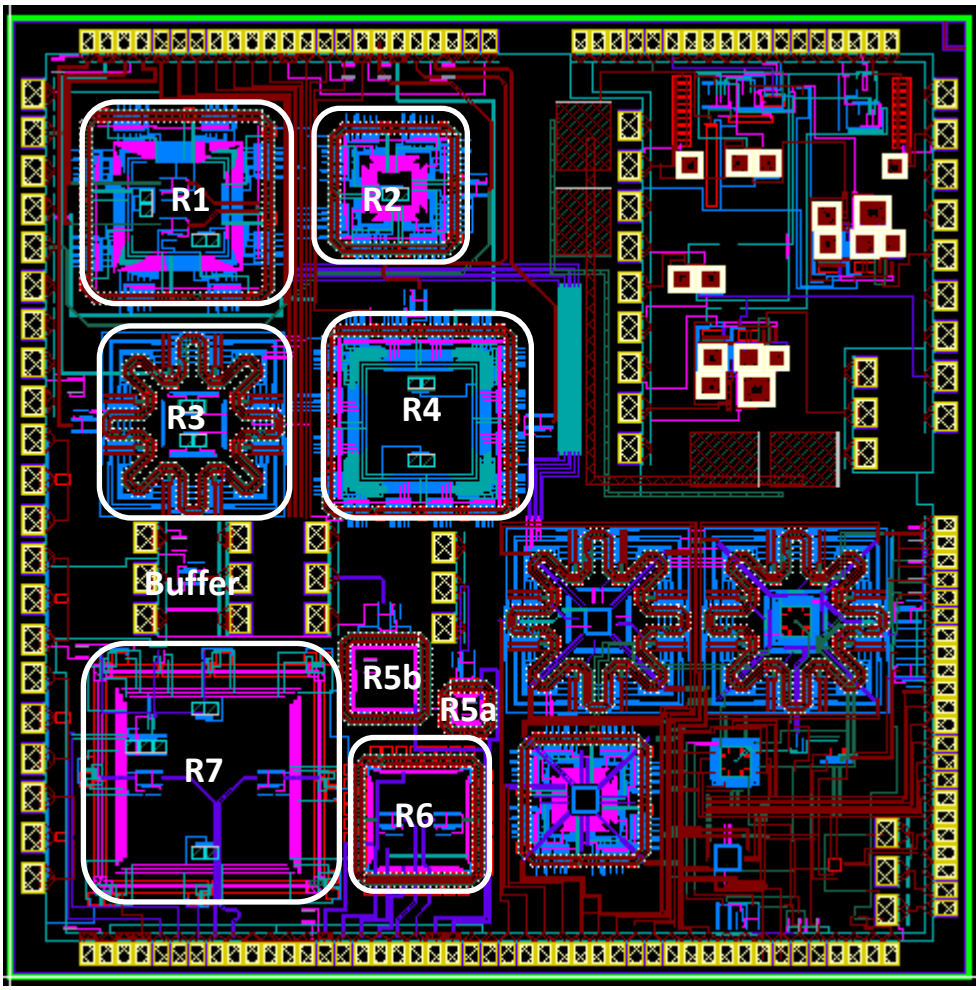


Figure 5.1. Layout view of the overall chip

Figure 5.2 shows the chip micrograph of the various RTWOs and buffer circuit which were implemented.

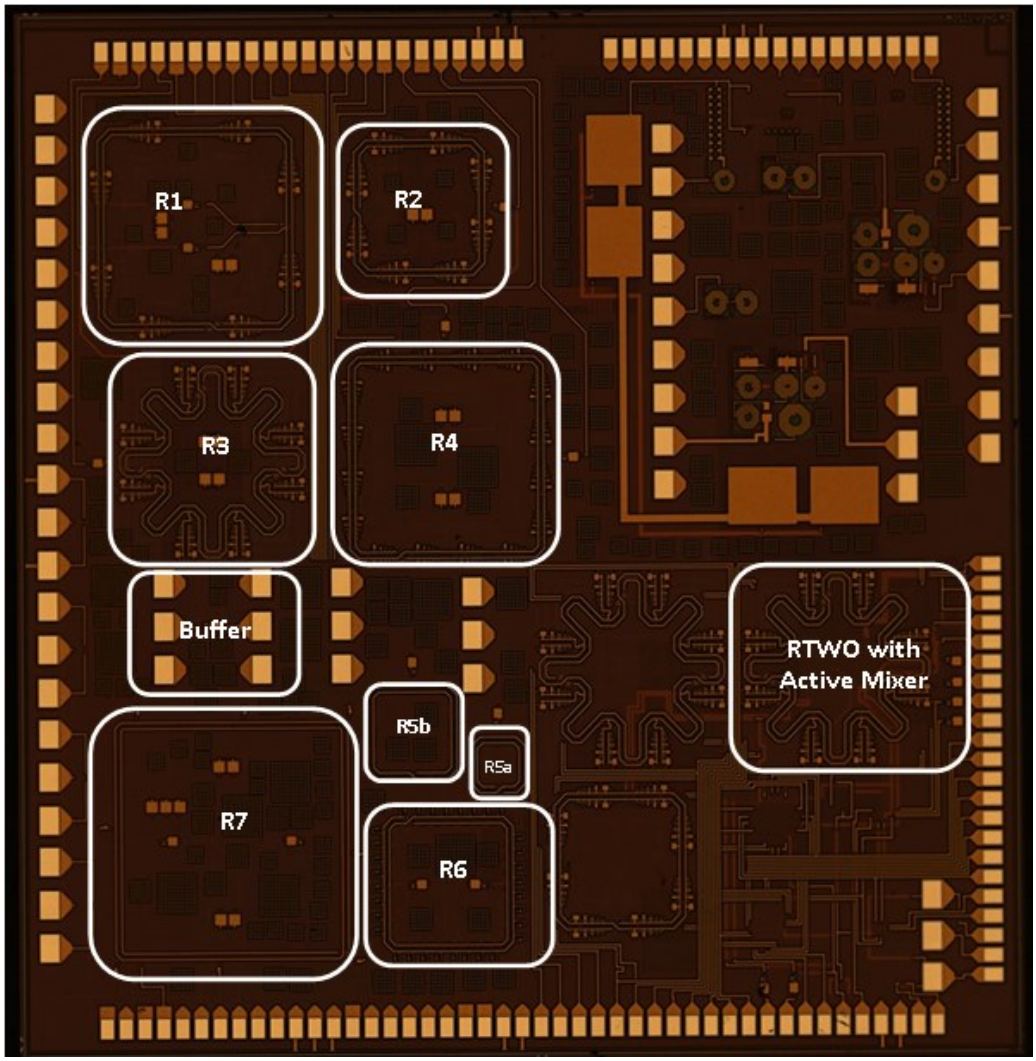


Figure 5.2. Chip micrograph

5.2 Chip Test Bench

The test board for the chip was designed using Altium PCB designer. A two-layer printed circuit board (PCB) was fabricated using Rogers 4350B laminate with a dielectric thickness of 62 mils for measurement. Rogers material is known to support high frequency applications compared to the popular FR4 dielectric. The test structure eliminates parasitics from packaging by directly wirebonding the bare die to the PCB popularly called Chip-on-Board (COB). For easy wirebonding and rework, electroless nickel immersion gold (ENIG) surface finish was selected. The conductive material is typically copper. Chip was attached to

PCB using conductive epoxy with no encapsulation for probing. One mil diameter aluminum bondwire was used. Figure 5.3 shows the device under test (DUT) using Cascade Microtech manual probe station with infinium GSG probe.

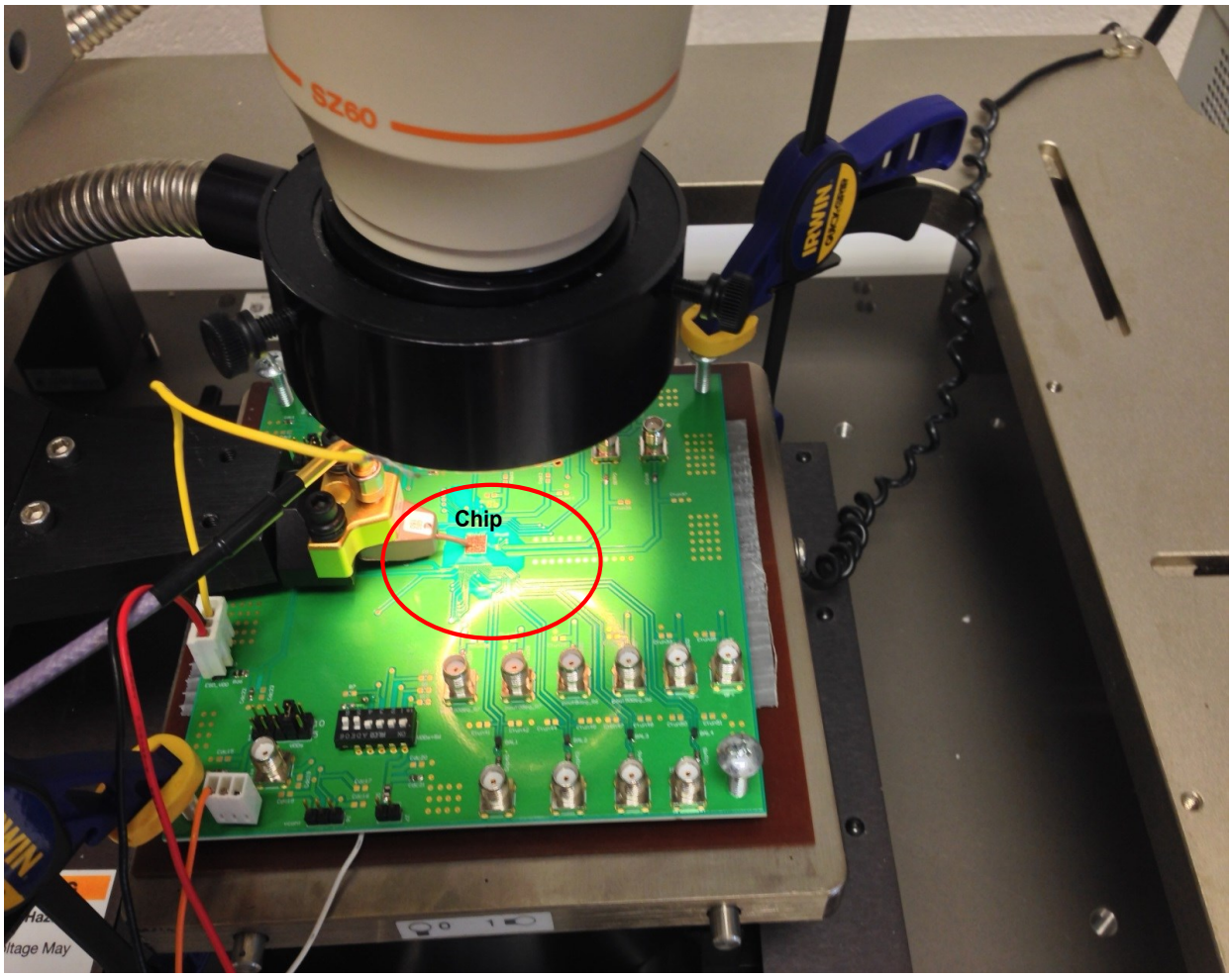


Figure 5.3. On-chip probing setup

5.3 Chip Performance Results

Table 5.1 lists the instruments for testing the chip. All measurements were conducted in the RF Microelectronics Lab at North Carolina A&T State University.

Table 5.1

Equipment list used for the measurement

Brand and Model	**Description**	**Specification**
Agilent N9310A	RF Signal Generator	9 KHz – 3 GHz
HP E3631A	DC Power Supply	Low Noise
Agilent DSO90254A	Oscilloscope	2.5 GHz
Agilent E4438C	ESG Vector Signal Generator	250KHz-6.0GHz
Agilent E4440A	PSA Series Spectrum Analyzer	3Hz-26.5GHz
Agilent N5242A	PNA – X Network Analyzer	10 MHz – 26.5 GHz

5.3.1 RTWO with tuning. Figure 5.4 and 5.5 compares the measured frequency tuning range and power level of RTWOs R1, R2, R3 and R4.

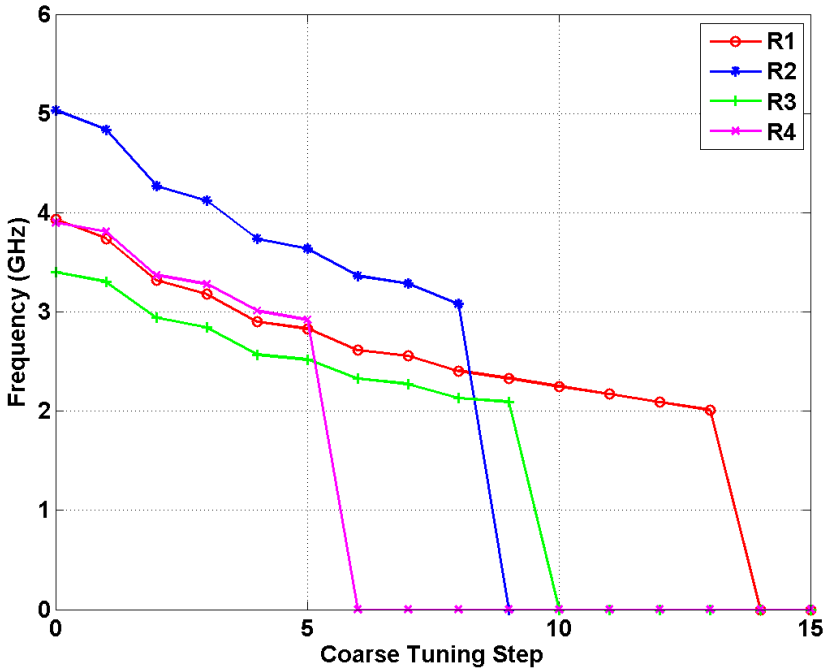


Figure 5.4. Frequency comparison of RTWO designs with tuning

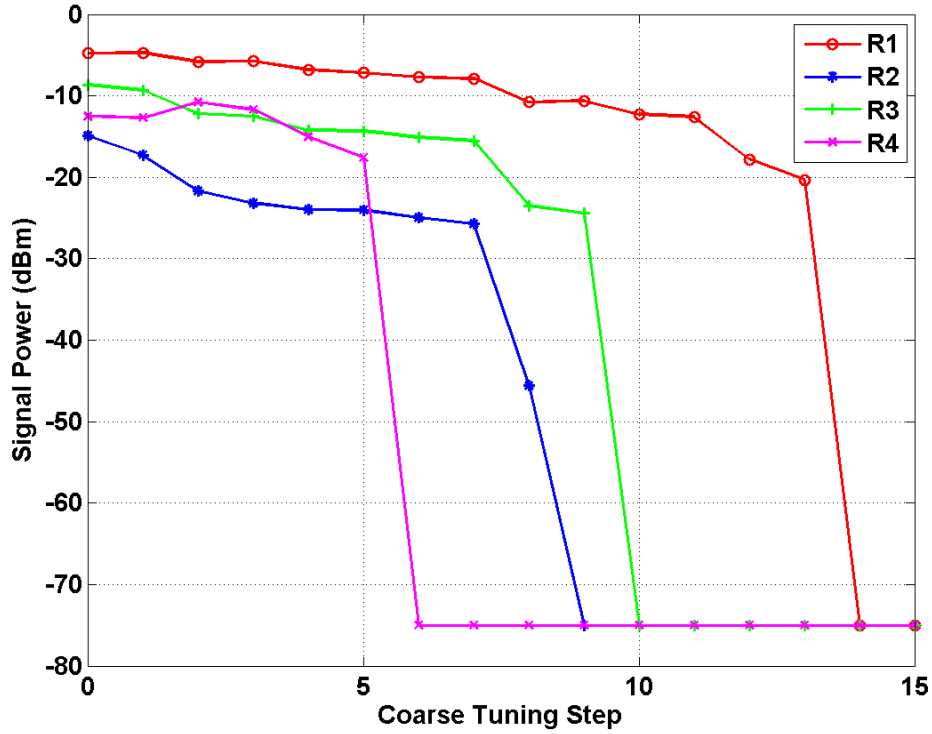


Figure 5.5. Signal power comparison of RTWO designs

Figure 5.6 shows a typical power spectrum measured for R1 for bits 0000 at the fundamental frequency. The targeted tuning range was 2 GHz – 4.5 GHz. RTWO (R1) tuning range measured from 2 GHz – 3.9 GHz which is close to the target.

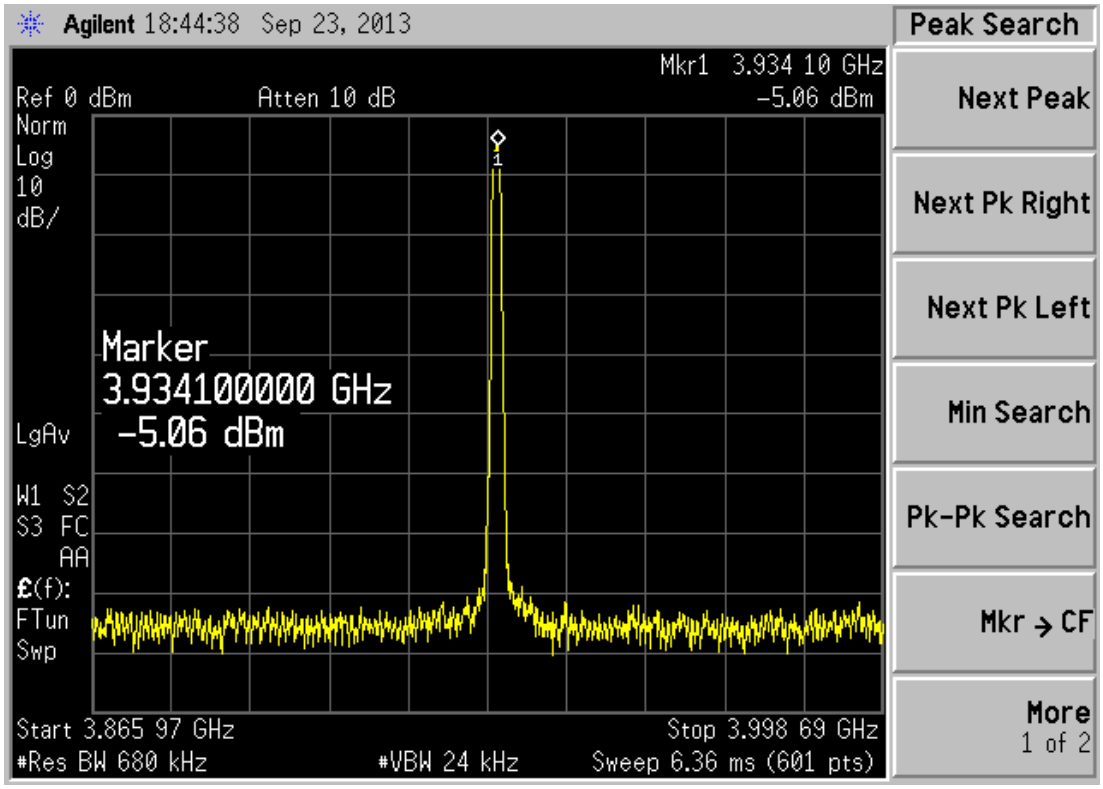


Figure 5.6. Typical power spectrum of RTWO (R1) at fundamental frequency

In order to observe the wide band nature of RTWO, the power spectrum was observed over a span of 26.5 GHz. Figure 5.7 shows the results of this measurement.

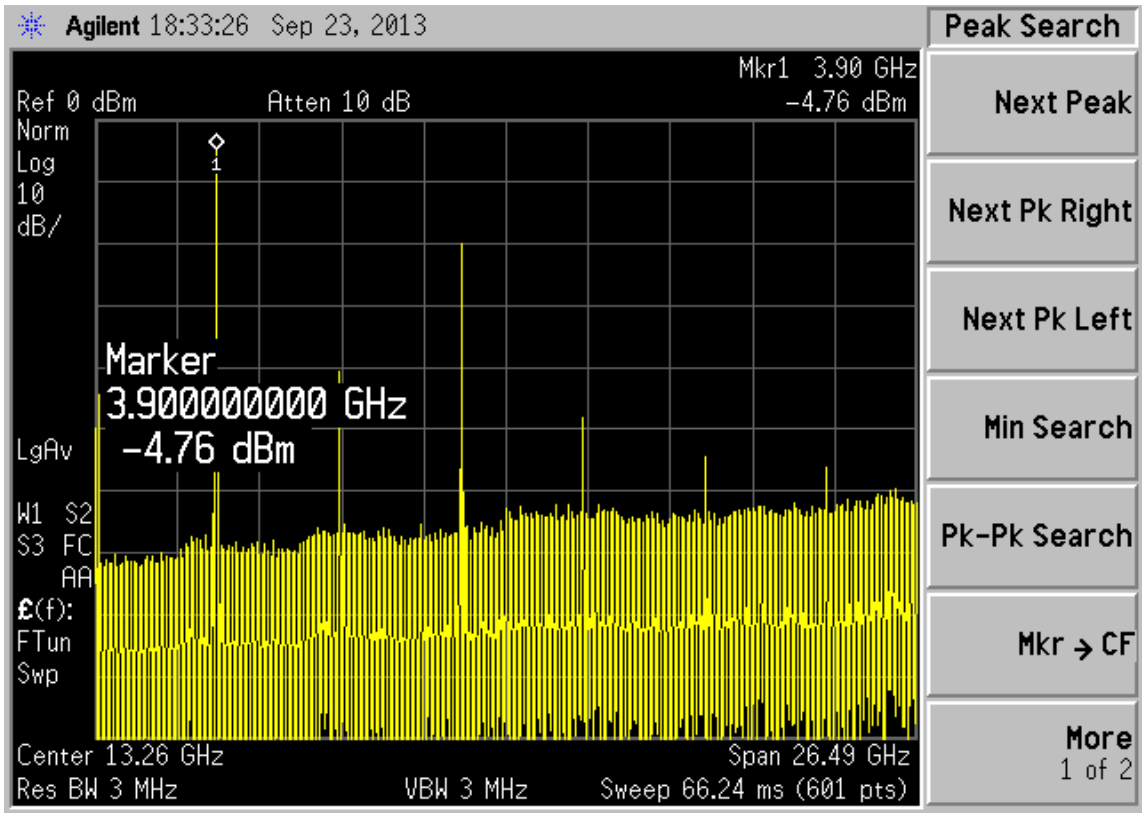


Figure 5.7. Typical power spectrum – wide band

Figure 5.8 shows the phase noise spectrum measured for R1 for bits 0000 at the fundamental frequency. The phase noise at 1 MHz offset was -122.61 dBc/Hz. This is comparable to phase noise in LC oscillators which are known to be low.

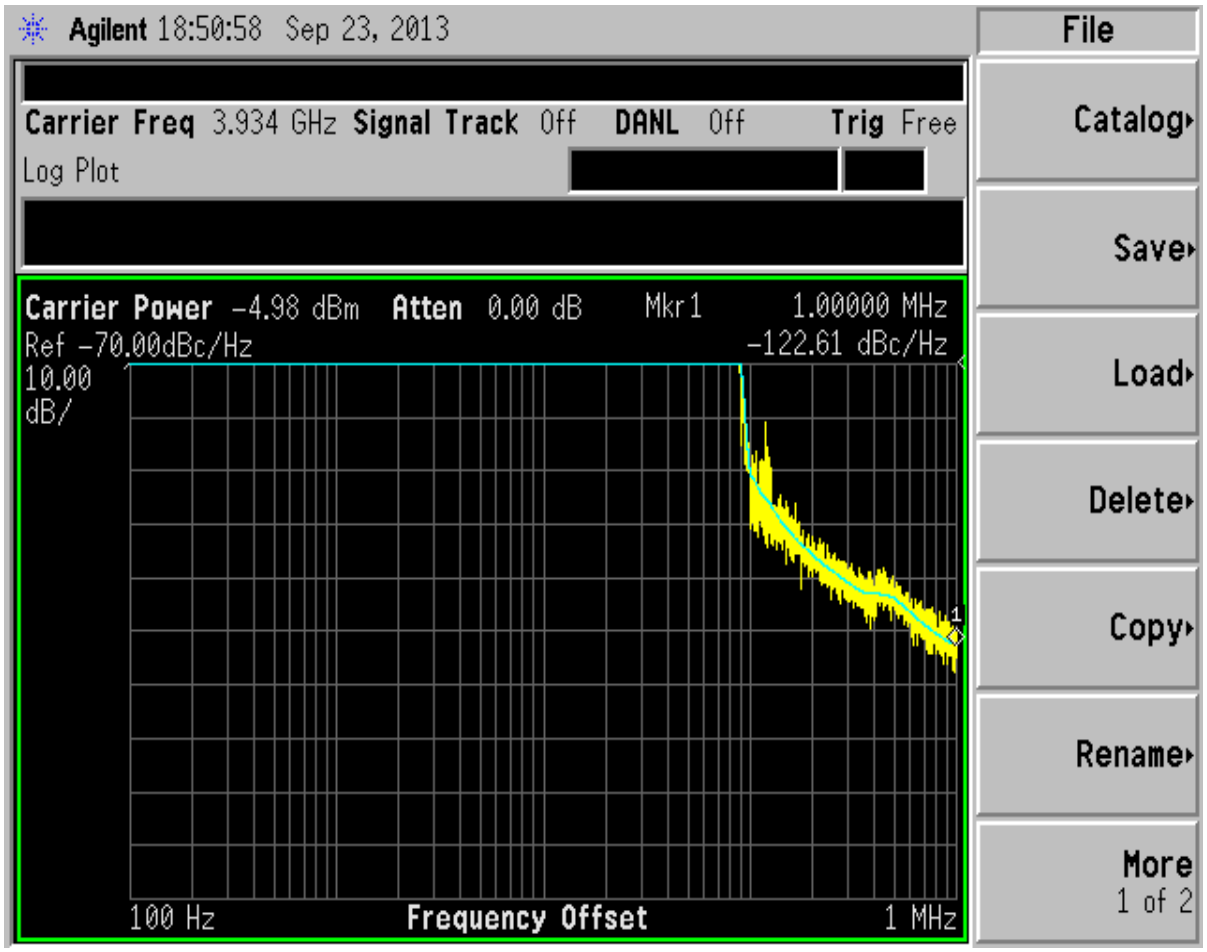


Figure 5.8. Phase noise spectrum for RTWO (R1)

The figure of merit (FOM) which is used to depict the performance of oscillator is defined as:

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{Dc}}{1\ mW}\right) \qquad (5.1)$$

where $L\{\Delta f\}$ is the phase noise the offset frequency Δf from carrier frequency of f_o and P_{Dc} is the power consumption in mW. Measured frequency and Figure of Merit (FOM) comparison is summarized in Table 5.2 and 5.3.The meandered RTWO structure (R3) compares to R1 but with a reduced layout area. The tradeoff is a reduction in signal power due to additional signal attenuation at the bending edges.

Table 5.2

Chip Performance Comparison – Oscillation Frequency

	Frequency (GHz)	
	Measured	Simulated
R1	3.93	4.05
R2	5.03	5.12
R3	3.4	3.7
R4	3.9	4.03

Table 5.3

Chip Performance Comparison - FOM

	FOM (dBc/Hz)	
	Measured	Simulated
R1	-177.12	-178.98
R2	-176.62	-179.11
R3	-176.48	-178.57
R4	-180.25	-181.96

To compare measurement results to simulation, extracted parasitics needs to be included in simulation. One important parasitic is the ground inductance which can be factored by replacing it with the equivalent resistance at the frequency of oscillation.

5.3.2 Novel RTWO with CCNPP. A comparison of frequency and power level between RTWO with conventional CCIP and CCNPP is shown in Figure 5.9.

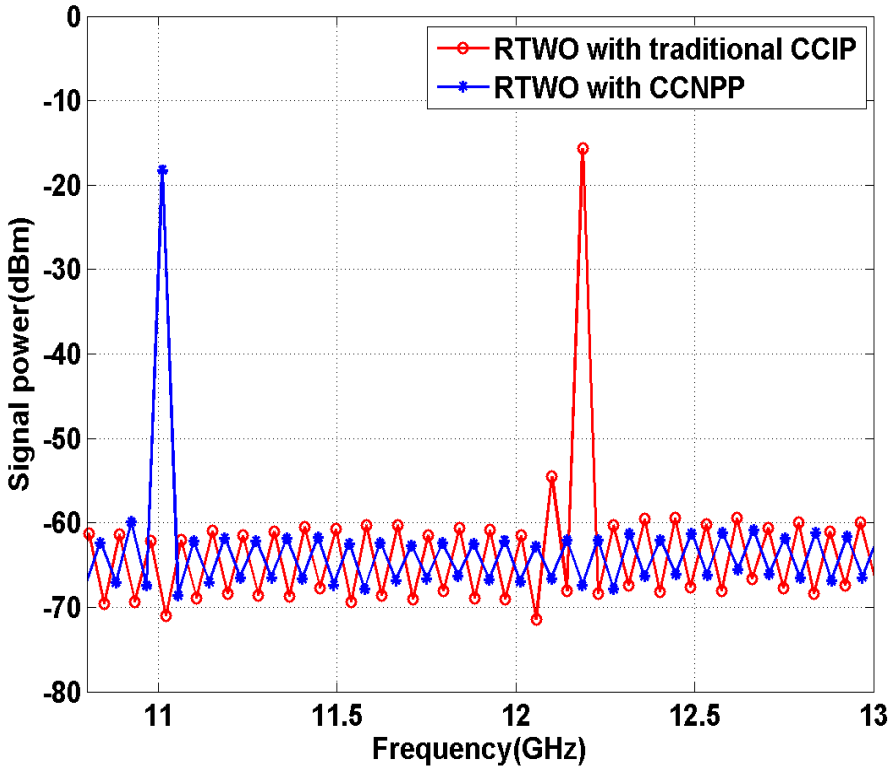


Figure 5.9. Power spectrum of RTWO (R5b) – Measured

Figure 5.9 shows the power spectrum of the two RTWOs being compared with loses from the output buffer and cables de-embedded. The difference in frequency is due to parasitics and process variations. Tuning elements are not included and both RTWOs are free running oscillators. Table 5.4 summarizes the measured results of performance measures.

Table 5.4

Performance Comparison of RTWO with CCIP and RTWO with CCNPP

RTWO with traditional CCIP		**RTWO with half-circuit CCIP (CCNPP)**	
Frequency (GHz)	12.2	Frequency (GHz)	11.03
Power consumption (mW)	38	Power consumption (mW)	30
Signal power (dBm)	-16.28	Signal power (dBm)	-17.21
PN @ 1 MHz (dBc/Hz)	-87.26	PN @ 1 MHz (dBc/Hz)	-98.24

Post layout simulation shows an excellent agreement for power saving, 22% in power reduction in simulation compared to 21% in measured results. Although proposed half circuit gain stage is driving twice the line parasitcs, it still achieves power savings. Simulation frequency was 11.9 GHz for both circuits. Using the same line segment length as traditional RTWO, proposed RTWO operates at 17.2 GHz. Figure 5.10 shows the phase noise spectrum for RTWO with CCNPP amplifier stage.

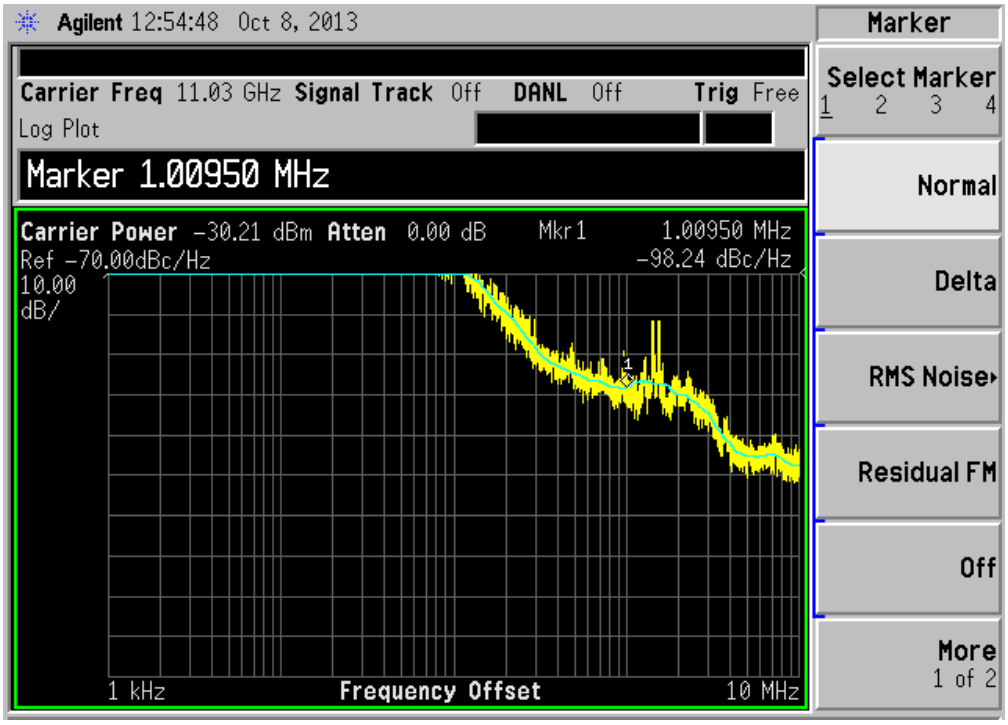


Figure 5.10. X-band phase noise spectrum

5.3.3 Direction control logic. Two direction control techniques were proposed. Figure 5.11, 5.12, 5.13 show voltage waveform from two tapped nodes for the technique with external control. A 20 MHz external control pulse was generated to test the various traveling modes. The clockwise or anticlockwise direction assert signal was set manually from the test PCB board. Measured results show traveling and standing wave modes. Traveling and standing wave modes are consistent with simulation results. RTWO operates at 1.99 GHz and consumed 58 mA of

current. Direction control was not observed in measurement as predicted by simulation. A probable cause is the low voltage swing that was observed for most of the RTWO designs implemented. A high voltage swing is critical for this technique to work.

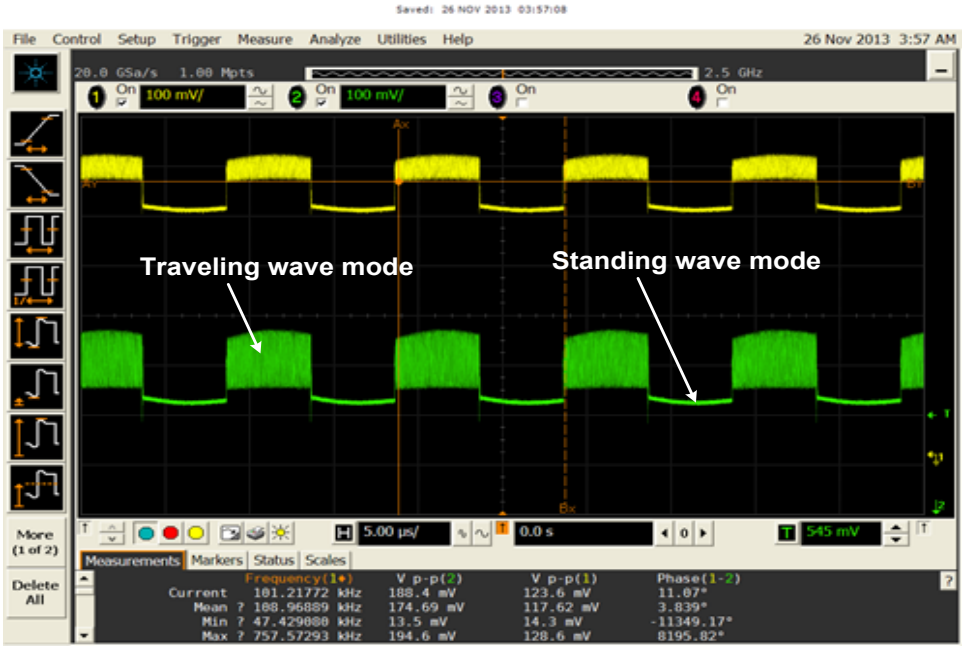


Figure 5.11. Waveform from two tapped nodes of RTWO (R7)

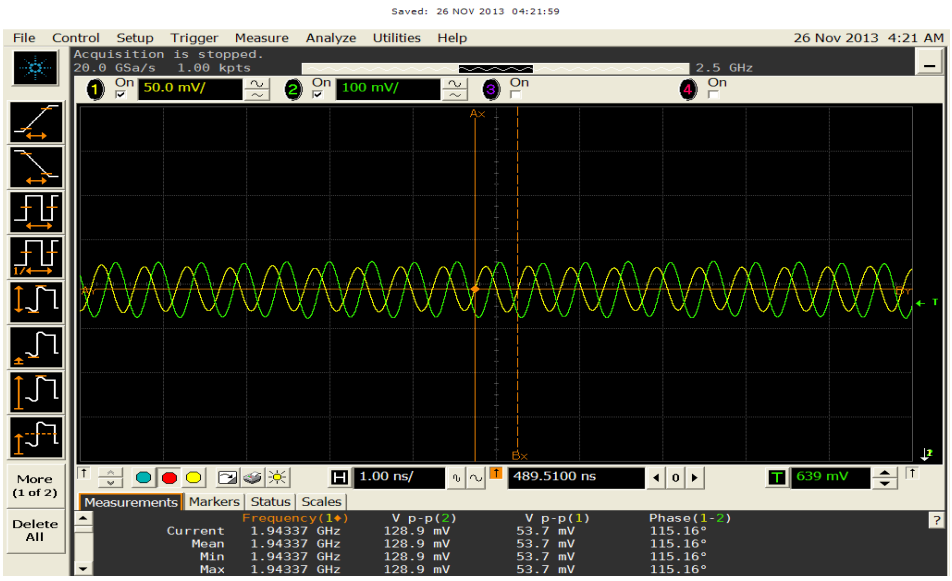


Figure 5.12. Traveling wave mode of RTWO (R7) – Magnified

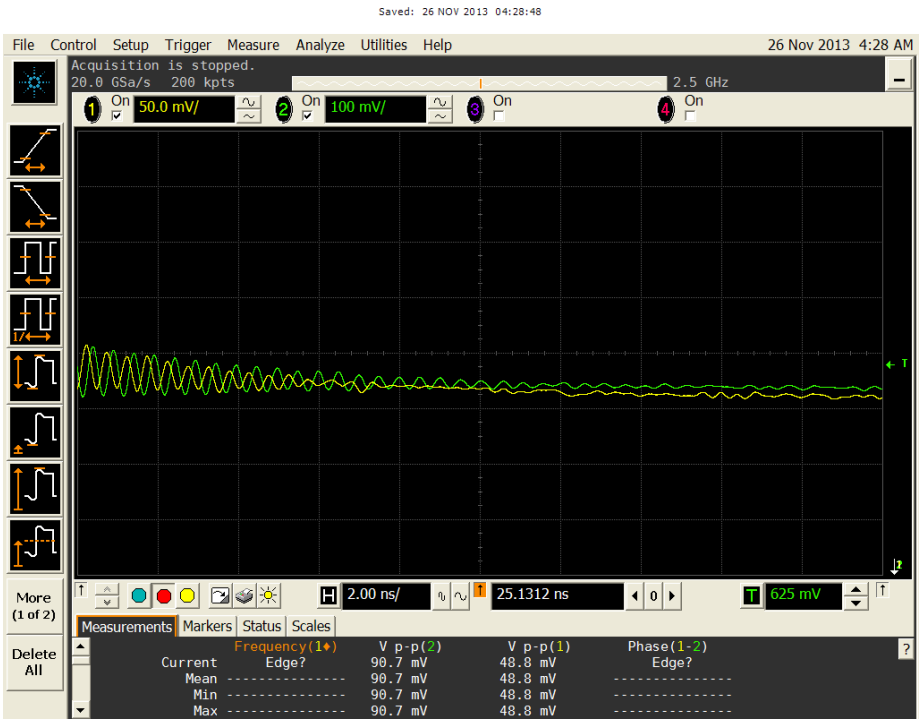


Figure 5.13. Standing wave mode of RTWO (R7) – Magnified

The second proposed direction control circuit is based on transmission line offset. RTWO with anticlockwise wave rotation was designed and implemented. Figure 5.14 shows the measured waveform from two tapped node with a predicted phase of 90^0. The negative phase indicates signal at Vout_90^0 is advanced relative to Vout_0^0 which agrees with simulation results. Low amplitude in measurement is attributed to the parasitic ground inductance which limits the swing on the line, as well as losses due to package and PCB parasitics.

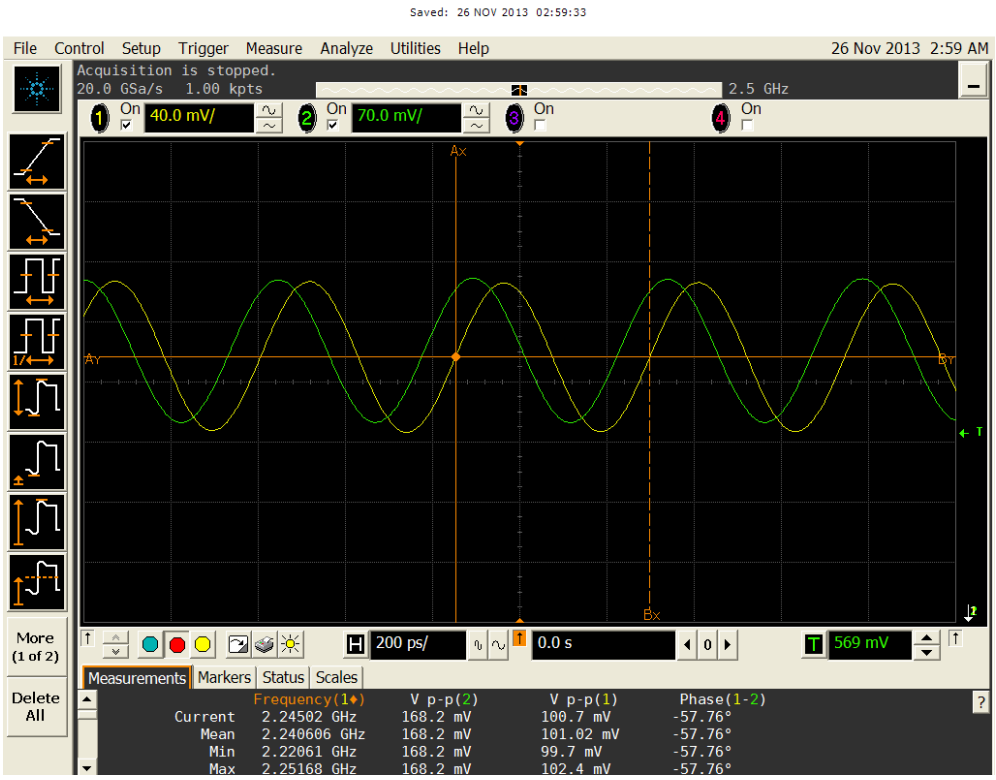


Figure 5.14. Traveling wave mode of RTWO (R6)

Simulated RTWO frequency was 2.09 GHz compared to 2.24 GHz measured value. Phase difference was measured to be 58^0 compared to 90^0 in simulation. This discrepancy is due to the mismatches of the signal paths from chip to oscilloscope.

5.3.4 Buffer circuit. Buffer was tested by measuring the power gain for a 0 dBm input power at different frequencies. Frequency range is 3.4 GHz to 13 GHz. Figure 5.15 shows a comparison between measured and simulated power gain of buffer.

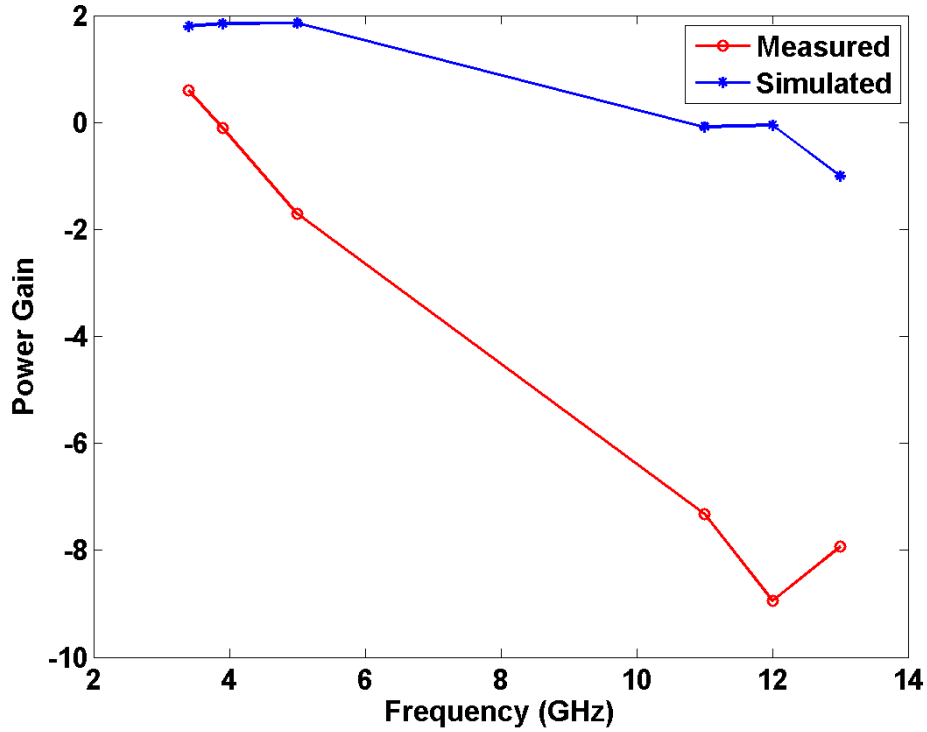


Figure 5.15. Simulated and measured power gain (dB) comparison

The measured current consumption is 8mA compared to 15mA simulated which explains the difference in power gain shown in Figure 5.15.

CHAPTER 6

Conclusion and Future Research

Rotary travelling wave oscillator has become an alternate solution for clock generation in application where distribution of clock signal with minimum skew is a key factor. Wide range of applications require continued improvement and advances in CMOS RTWO design. Low phase noise and low power consumption dominate design requirements. The objective of this research was to address some of the problems of RTWO design including high power consumption, uncertainty of propagation direction and optimization of RTWO design parameters.

The drive for process technology scaling is to reduce power and increase operating frequency. A novel cross connected NMOS-PMOS (CCNPP) with balance resistor was proposed and implemented as an alternative to CCIP. With CCNPP as the gain stage RTWO achieves low power operation, operating at a higher frequency compared to RTWO with CCIP.

Propagation direction in RTWO is primarily accomplished through least resistance path in the RTWO structure. Direction is random and will not be desirable in synchronous and poly-phase mixer applications where accurate phases of the signal are necessary. Typical direction control techniques require an external circuit that preempts defined direction and reverses wave propagation. Such circuit adds to the current budget and may not be best for power constrained applications. An offset technique which involves connecting one of the CCIPs through a section of transmission line was proposed and implemented. Measurement results confirmed that this technique works well introducing negligible asymmetry. Another proposed technique that uses an external direction control signal and CCIP implemented using NAND gate was designed and implemented. Whereas the simulation results predicted direction control, measurement results

were inconsistent with the simulation. A probable cause is the low voltage swing that was observed for most of the RTWO designs implemented. We suspect that ground bounce due to layout issues may have caused low signal swing.

Techniques to improve RTWO performance were also verified through design and implementation of different structures. To do this different RTWO designs with varying structures in terms of ring size, meandering, and number of CCIPs were implemented. Noticeably, it was verified that increasing the number of sections improves phase noise. The wide band tuning capabilities of RTWO was ascertained with one RTWO design measuring about 2 GHz tuning range (2 GHz to 3.9 GHz).

We derived closed form expressions for the time constant and propagation delay of CCIP. It will be of interest to explore this technique in the future to speed up the CCIP which helps to increase RTWO frequency.

RTWO design is a multi-objective, multi-parameter design problem. In this work, an optimization process using genetic algorithm and neural networks is developed to help the designer with selecting transmission line parameters that reduces both power consumption and phase noise without one objective dominating the other. The effect of the gain stage was not optimized but can be included as a variable in future work.

A buffer circuit that combines the advantages of push pull amplifier and current mode logic amplifier with miller feedback was implemented. The two stage buffer circuit achieves a simulated wide tuning range up to 25 GHz and high power efficiency. A single ended buffer topology was implemented and such designs are susceptible to substrate noise. For future work, a differential version can be implemented and characterized. Major contributions of this work include; (i) Implementation of a novel RTWO based on cross connected NMOS and PMOS

pairs (CCNPP), (ii) Implementation of a novel direction control technique based on “offset CCIP” section, (iii) RTWO design optimization based on Genetic Algorithms and Neural Network, and (iv) Implementation of a compact two stage CMOS buffer for driving 50 Ω load.

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