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Computational Modeling Of A Graphene Based Field-Effect Transistor

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Computational Modeling of a Graphene based Field-Effect Transistor

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Biographical Sketch

Pedro Nicodemo Cintron-Tirado was born and raised in the U.S. Virgin Islands. After graduating from high school, Pedro received two scholarships and pursued a Bachelor of Science in Electrical Engineering. After graduating in May 2010 from North Carolina A&T State University, Pedro accepted a job as an Electronic Warfare Engineer with the Naval Undersea Warfare Center (NUWC) Division Newport, where he excelled and later became Subject Matter Expert/Project Lead on several areas. After working at NUWC for three years, Pedro received authorization to take leave without pay to complete his Master degree at North Carolina A&T State University. Pedro worked as a research and teaching assistant while pursuing his Master degree.

Dedication

I would like to dedicate this research to my advisor Dr. Xie and my committee members, Dr. Dogan and Dr. Lee along with the Electrical and Computer Engineering department.

Acknowledgements

First, I would like to thank GOD because he makes all things possible in this world. I want to acknowledge everyone that has encouraged me to pursue my Master degree and has believed in my potential. I would like to thank my mother Marcia Tirado Cintron for consistently being my backbone and my support system since the day I was born. Another, important figure in my life is my father in law Julio Avila, who has constantly been very supportive of my decisions in my life. I would like to give thanks to my aunts Olga, Magnolia, Hilda, Victoria, and Jackeyln Tirado. I would like to thank my brother Lewis Clemencia for being there for me when I needed him the most.

I would like to thank the Electrical Engineering department the opportunity to study at North Carolina A&T State University. I would like to thank Dr. Xie, Dr. Gong Gu from the University of Tennessee, and NSF (National Science Foundation) for their financial support. I would like to thank Dr. Kelly and Dr. Kim for the assistance and advice that were offered during my graduate career. I have learned numerous lessons while pursuing my Master degree which have been a humbling experience. The experience I am taking away is to become a self learner and there is no limit to how much one person can learn. These experiences are also applicable outside of the educational realm and help in the work force as well. I would like to thank my job at the Naval Undersea Warfare center Division Newport for granting me leave without pay to pursue my Master degree while holding my job until I returned. Furthermore, I want to thank my friends for the numerous group sessions that we attended while reviewing for our classes. It has been a long journey, but I did not complete this journey alone. The support system that A&T offers is very helpful and has helped to propel me to finish my Master degree.

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Abstract

With every passing day, the demand for devices that have higher operating speeds increases. Currently, silicon's transistor size is limited and it has become difficult to obtain similar performance as compared to previous transistors. The silicon transistor design has changed from a planar geometry to an FINFET design, which allows dimensions to be scaled further while achieving similar performance. Even with this change in geometry, silicon will reach its scalable limit. With such a high demand for faster operational devices, the limitation of silicon will only be able to support the next generation transistors, and then a new type of transistor will be needed. Here is where the GBFET will have the potential to be next in line for chip makers to use in their design. The attractive feature of this transistor is its high performance, which exceeds that of current silicon transistors.

Through steady evolution, the simulation of physics based research has become more acceptable. This is due to the ability that simulations offer to produce a sense of confidence that an idea has the capability to work. For this thesis, COMSOL is used to simulate a graphene based Field-Effect Transistor (GBFET) to demonstrate the ability that this design can work and what performance can be expected. Within COMSOL there exists a semiconductor module that allows the user to characterize the electron concentration, hole concentration, electric potential, and other important factors needed to determine performance. This makes COMSOL a good fit for the simulation of the graphene based transistor.

CHAPTER 1

Introduction

Today, consumers are always looking for devices that offer fast and convenient features to assist with their everyday lives. *Figure 1* displays an updated version of Moore's law where the demands for smaller transistors are predicted [1]. Most items that provide a convenience to consumers are high speed electronic devices. Therefore, to satisfy growing consumer demand for faster and more convenient technology, creative alternatives must be explored. The current technology is less and less able to meet the growing demand, and so there is a great need for a new technology to emerge.

Using graphene, a new design of a transistor is being simulated in COMSOL to overcome the limitations of using silicon. Silicon has been used in transistor design since it was first discovered as a semiconductor in 1940. Challenges that are being faced with using silicon are apparent when scaling the transistor size to a smaller dimension without losing its performance integrity; another limitation is the carrier mobility of silicon. Graphene, however, has some very attractive features that electrical and mechanical engineers can take advantage of, such as high carrier mobility at a smaller dimension (therefore, scaling is not an issue) [2]. Graphene is also one of the strongest materials to be discovered. Its 0.142 nm long carbon bonds make it stronger than structural steel and lighter than a single piece of paper [3].

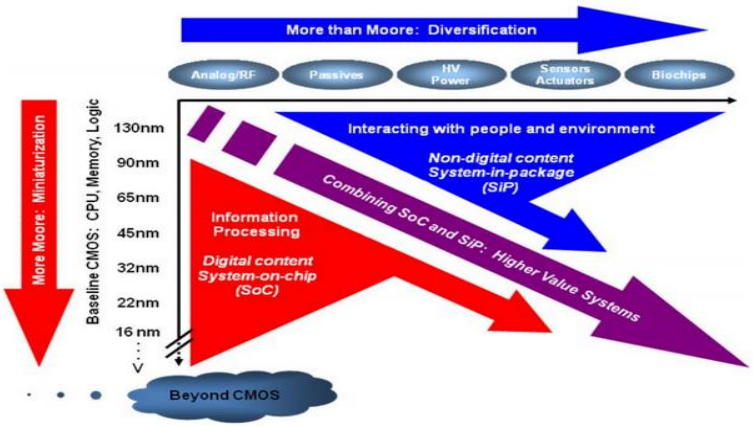

Figure 1 Moore's law 2012 [1]

1.1 Silicon

Silicon is the 14th element on the periodic table of elements, which means that it has four valence electrons. Pure silicon actually is an insulator which means it is not a very effective conductor. Since silicon has four valence electrons, silicon can easily be bound to other atoms to increase the number of electrons or holes, which makes it a very excellent semiconductor [4]. Silicon is rarely found in nature in its purest form and is mostly found as a silicon dioxide, which is a valid insulator. The ability to dope silicon with more electrons or holes gives an engineer/scientist a lot of flexibility when designing devices for distinct applications [5]. Since the discovery of silicon as a semiconductor in 1940, it has been used as in many different applications while maintaining the lead in semiconductor devices even at this more advanced era. Silicon is widely used in many areas such as analog circuits, RF applications, and digital logic circuits, etc. This is due to the high on/off ratio that dope silicon transistor offers that provides such flexibility. Though silicon is a great material, it is now becoming limited due to the finite thickness that chip makers are able to achieve while maintaining performance integrity. Additionally, the material and processing of the silicon is considerably cheap as compared to

other materials. Thus, the hunt has started for the next new material to take the stage as the following leader in the semiconductor arena.

1.2 Graphene

Graphene is semi metal and is also a crystal that's composed of single layer carbon atoms (or atom thick) that are bonded together in a hexagonal lattice. Graphene is thin and to some scientists, it's considered 2 dimensional [2]. The lattice structure of graphene has a honeycomb shape which makes an excellent conductor of heat and electricity (see *Figure 2* and *Figure 3*) [2]. The honeycomb lattice structure of graphene allows for additional manipulation of the electron for virtually lossless and very fast transistor operation. This is due to the 2D nature of graphene, which causes the electrons to behave as if they have no mass. This is why the electrons inside graphene are governed by the first-order Fermi Dirac equation [2]. Furthermore, electrons in graphene can travel large distances without being scattered due to collisions with impurities inside the material. This feature of graphene offers the potential of high-frequency functionality, which is essential to high speed operation.

Graphene offers the promise to fulfill the needs of the ever growing need for faster operational devices as an alternative to silicon. One of the most attractive features is the ability it has to maintain electrostatic integrity and high carrier velocity at scaled dimensions at near room temperature. With the high carrier mobility that graphene offers it promises higher cutoff frequencies, which are dependent on the carrier mobility [6]. With this unique property graphene offer's the potential for devices that are operational in the Terahertz region which is still an untouched band. In terms of fast operation, graphene can achieve a high mobility of 120,000 $cm^2/V*s$ at near room temperature. Furthermore, another attractive feature is the high saturation velocity that graphene offers. This feature ultimately determines the limitation on high speed

operation through a material. It is also an excellent conductor of electricity because of the lack of an energy band gap.

Due to the zero band gap of graphene it is usually called a semi-metal which makes it very sensitive to small change due to external applications such as an electric field, doping, and deformation (this characteristic is very attractive in application such as sensors). A challenge about using graphene is due to the lack of band gap (see *Figure 4*) of the material which can be a great benefit depending on its application. As a result of this, the on/off ratio of the transistor is not as effective as other comparable silicon transistors this is due to the zero band gap which causes a small amount leakage current across the terminals. This research is investigating the co-integration of silicon and graphene, the on/off ratio can be improved with or without creating a band gap for graphene and manipulated to be used in a large number of applications [6]. This is accomplished through the use of a unique doping profile in the silicon substrate to shift the characteristics of the graphene as a controller. Technically the GBFET does not have an off state, but there is a state when the conductivity is minimal.

Even with a limited on/off ratio, a GBFET would be of great use in applications such as analog circuits and RF applications, but for now would be difficult to implement in logic applications. The intention of this work is to integrate graphene into current silicon transistor manufacturing processes. This integration will gain superior performance while taking advantage of current silicon manufacturing process and reducing the cost to produce such a different transistor. The cost saving is in the ability to reuse the same equipment and processes currently being used to make silicon transistors versus creating a new a new manufacturing process. In equation 1, V_F is 2.5×10^6 m/s the Fermi velocity inside the graphene material and W is the thickness of a single layer graphene is 0.335 nm for all the models here on out [7].

$$n = p = \frac{2}{W\pi h_{vf}} \sum_M \int_{E_m}^{\infty} \frac{E}{\sqrt{E^2 - E_m^2}} \frac{dE}{1+\exp\left(\frac{E-E_{FG}}{kT}\right)} \quad (1)$$

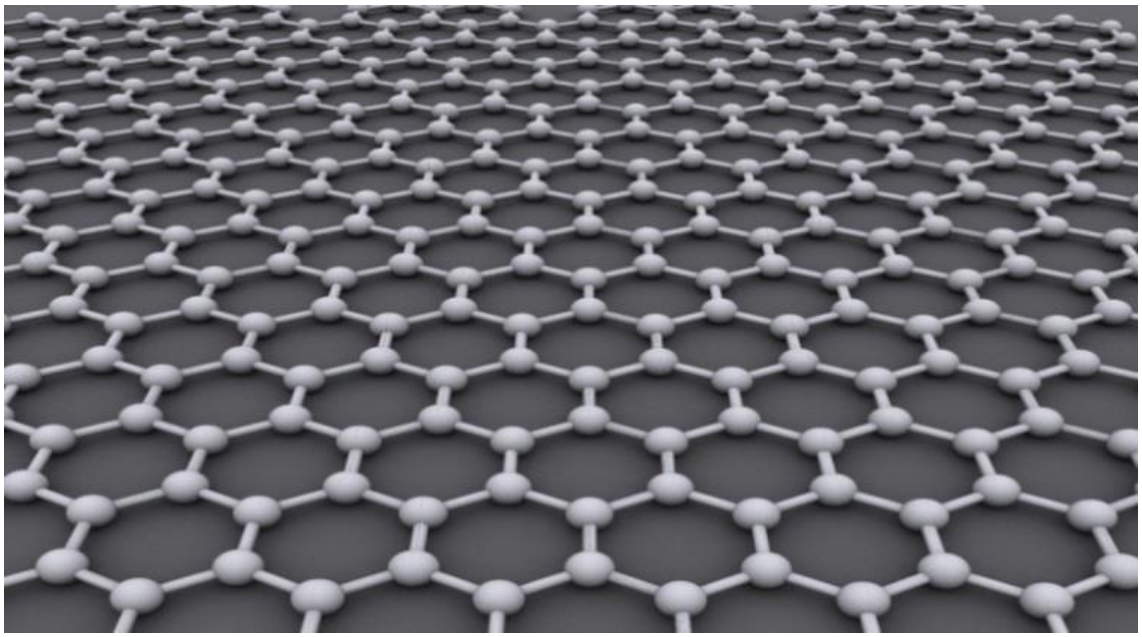

Figure 2 Graphene lattice structure [8]

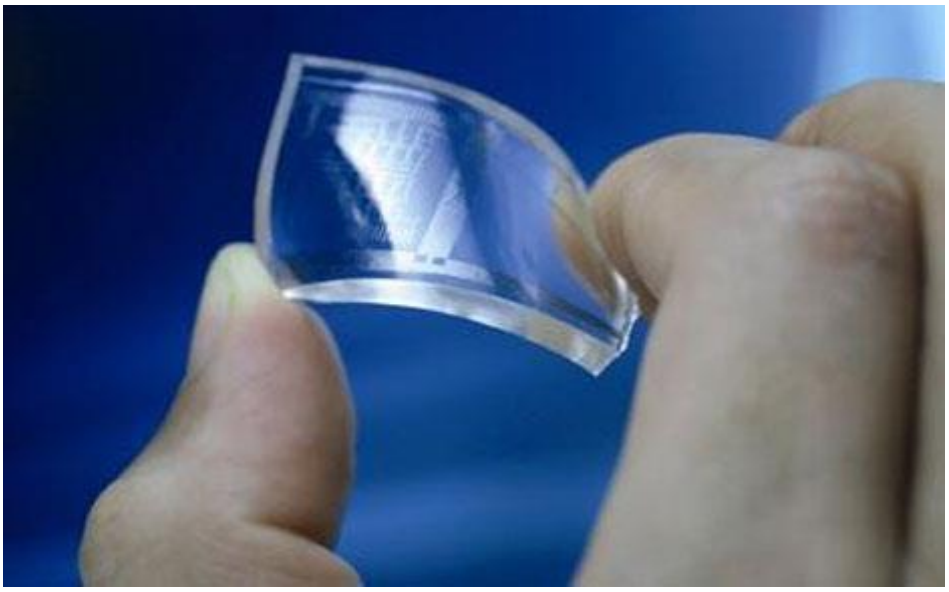

Figure 3 Graphene on flexible substrate [8]

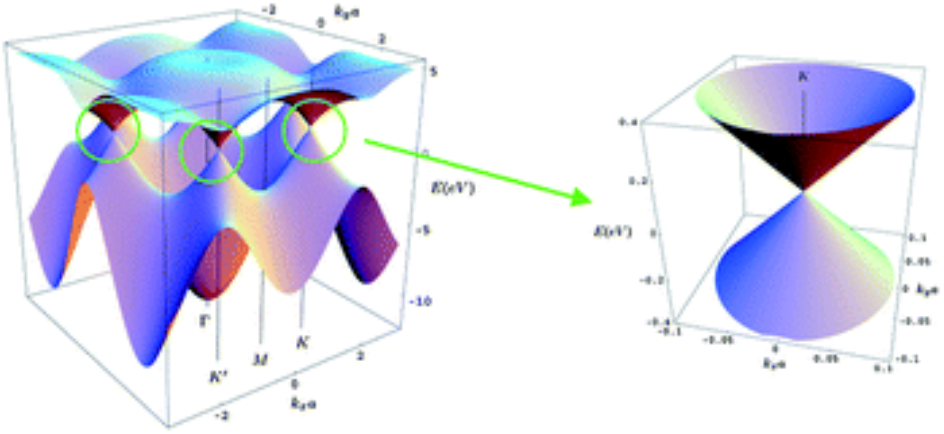

Figure 4 Band gap of graphene [3]

CHAPTER 2

Why COMSOL?

COMSOL is very powerful multi-physics software that allows users to simulate almost anything that can be imagined. This software comes with numerous complete packages known as modules with many preset physics parameters that can be used in many different areas. COMSOL comes with a list of powerful complex solvers that give way to in depth computations. Also, included are a few different advanced meshing options for higher resolution when performing complex simulations [9].

2.1 COMSOL

As technology progresses, it is becoming very time-consuming and costly when determining new research ideas for potential use. With the evolution of technology, computer-based simulations are becoming more accepted in our scientific society. Simulations can conserve time, and also significantly save on the cost of research and development. However, the main benefit is the confidence that simulations can provide to investors before investing into an idea. Another benefit to computer-based simulations are that fewer assumptions are made as compared to performing hand calculation [10]. Due to the ability that COMSOL grants by interconnecting with the other physics module, a better approximation can be computed instead of making an assumption. COMSOL does include a mathematics, and differential equation package which a user can input all the equations and parameters manually [9].

In this case, the Semiconductor module is being used due to the extensive research that has been completed by COMSOL on the theory, meshes, and complex solvers. The Semiconductor module combines the drift diffusion equations module, enhanced capabilities for

modeling electrostatics, and an electrical circuit's interface to solve for the different parameters of the transistor and thus the term "Multi-Physics". For the ease of geometry creation, a model can be generated in auto CAD (Computer-Aided Design) and be imported into the COMSOL Software [11]. However, if at all possible, a simple structure is preferred to minimize computational issues. When using the semiconductor module, the user will notice that there are numerous parameters that are computed such as electron concentration, hole concentration, electric potential, current concentration, terminal current, and space charge density, etc. COMSOL can calculate an extensive list of important parameters in zero, one, two and three dimensions, which make it a good fit for this analysis [12].

2.2 COMSOL Analysis

Initially, this project was simulated using MATLAB as proof of concept for the National Science Foundation (NSF) contract which generated favorable results. Next, COMSOL was used because of the advanced complex solvers that were already available for better performance times and better accuracy. To ensure COMSOL results were comparable, identical dimensions were used in the COMSOL model to obtain similar results as in the MATLAB simulation. In COMSOL, silicon is a predefined material which can be imported with all the semiconductor properties needed for an advanced simulation. This is not the case for the graphene material. A new material was created in the material library and was added to the model. When it is added to the module, COMSOL highlights all the required fields that are needed for the simulation.

The basic parameters that are needed to run a simple simulation in the COMSOL semiconductor module are relative permittivity, band gap, electron affinity, electron/hole mobility, and electron/hole density of states [12]. For this model, Fermi Dirac's carrier statistic was used for the entire transistor model, which includes the silicon material. COMSOL includes

predefined equations in the semiconductor module which are explained in the user manual and are applicable to almost all semiconductor simulations. However, in this case, the electron concentration equation had to be too modified to reflect to reflect the massless behavior of electrons in graphene. See equations below displays the mathematics and COMSOL the electron/hole concentration for silicon [12].

$$\boldsymbol{n = \frac{1}{4}\left(\frac{2_m}{\pi h^2}\right)^{3/2} \frac{2}{\pi^{1/2}} \int_0^{\infty} \frac{W^{1/2}}{1+exp[(W+E_c-E_f)/(k_B T)]} dW} \quad (2)$$

$$p = \frac{1}{4}\left(\frac{2_{mh}}{\pi h^2}\right)^{3/2} \frac{2}{\pi^{1/2}} \int_0^{\infty} \frac{W_h^{1/2}}{1+exp[(W_h+E_f-E_c)/(k_B T)]} dW_h \quad (3)$$

For the silicon material, equations 2 and 3 were used to compute the electrons and hole's concentration in the silicon material which was used for the substrate and the gate. The semiconductor module has three dependent variables that are solved through an iterative process these are electric potential, electron, and hole concentration. Refer to equation 4 to observe how the electric potential was computed. There are numerous other parameters that are computed in the background that can be used in calculations and analysis of the device's performance. As part of the module, COMSOL includes a doping feature that allows uniform or customized doping profiles [12].

$$\nabla(\varepsilon_f \nabla V) = q(n - p + N_A^- - N_D^+) \quad (4)$$

$$N_d^+ - N_a^- + p - n = 0 \quad (5)$$

Using the parameters in the equations listed above, COMSOL uses an extensive iterative process which solves for dependent variables until the previous values are roughly the same as the new values. When the new value is approximately the same as the old values, the model has converged. Equation 5 displays the formula to determine the equilibrium of the carrier concentrations. Additionally, COMSOL can perform a parameter sweep, which allows the user to characterize the device without having to run many simulations with different parameter's value [12]. This feature was used to perform a sweep at the gate and at the drain to determine saturation points and carrier concentration behavior. Though there are many convenient built-in functions in COMSOL, the knowledge that was used was reviewed to ensure each feature produced results that were comparable to the simulations which were computed in MATLAB.

COMSOL recommends using their inherent thin insulator gate in place of an actual gate and oxide which visibly appears in the simulation only as a contact [12]. This feature allows the user to configure the gate voltage, metal work function, oxide thickness, and oxide relative permittivity. This feature is very helpful because it significantly reduces the number of mesh points, which saves on computational time. However, this feature was not used in the transistor simulation because of the unique design of the GBFET with respect to how the contacts were being utilized. Additionally, the thin insulator gate was not used because the potential could not be observed through the gate and the oxide making it difficult to compare to the MATLAB results. Physical structures were created for both the gate and the oxide, which were incorporated into the semiconductor modules. Initially, an attempt was made by using silicon dioxide as a semiconductor with a band gap of 9 V to cope with semiconductor module, this did not work due to convergence issues with the model. The issue was corrected using a feature called charge conservation, which allows a user to compute the electric potential through a material [12].

Silicon should not display any conducting abilities and should only propagate electric potential through the material making this feature a good fit. The equation that was used to calculate the potential through the silicon dioxide is given below [12].

$$E = -\nabla V \tag{6}$$

COMSOL recommends using ohmic contacts which act as an ideal contact for simulating transistors. The following are equations that were used to compute the electric potential, hole/electron concentration, and the Fermi energy while applying an ohmic contact. This contact is easy to use by selecting the boundary of a domain as the contact. The equation's COMSOL uses are listed below [12]:

$$V = V_a + \frac{k_B T}{q}\operatorname{arcsinh}\left(\frac{N_D - N_A}{2n_i}\right) - X - \left(\frac{\frac{E_g}{2q - k_B T}}{2q * \ln\left(\frac{N_V}{N_C}\right)}\right) \tag{7}$$

$$n = p = \frac{1}{2}(N_d^+ - N_a^-) + \frac{1}{2}\sqrt{[(N_d^+} - N_a^-)^2 + \Delta\gamma_n\gamma_p n_{i,eff}] \tag{8}$$

$$\Delta E_f = \frac{k_B}{2q}\left(T * \ln\left(\frac{N_V T}{N_C T}\right) - T_0 * \ln\left(\frac{N_V T_0}{N_C T_0}\right)\right) + x^0 T_0 - X^0 T + \frac{1}{2q}(E_g^0(T_0 - E_g^0 T) \tag{9}$$

An ohmic contact is generally used for heavily doped materials. The contacts in this simulation are composed of copper and are not selected as part of the semiconductor which assumes that it is an ideal contact. The gate of the structure is comprised of silicon, which is heavily doped with n type, which is known as a poly silicon gate.

COMSOL has created a doping tool to facilitate the doping process. In this tool, the user can identify the material that is to be doped along with the doping intensity, direction, and depth. This feature can be used to create unique doping profiles while still retaining the ability to apply a Gaussian doping distribution [12].

2.3 COMSOL Setup

In COMSOL, first a structure must be created that best represents what the user is trying to simulate. How the structure is designed helps with creating a mesh for more accurate results. In this case, a simplified form of a transistor was built to simulate the GBFET versus the typical design of a MOSFET transistor (See *Figure 5*) [11].

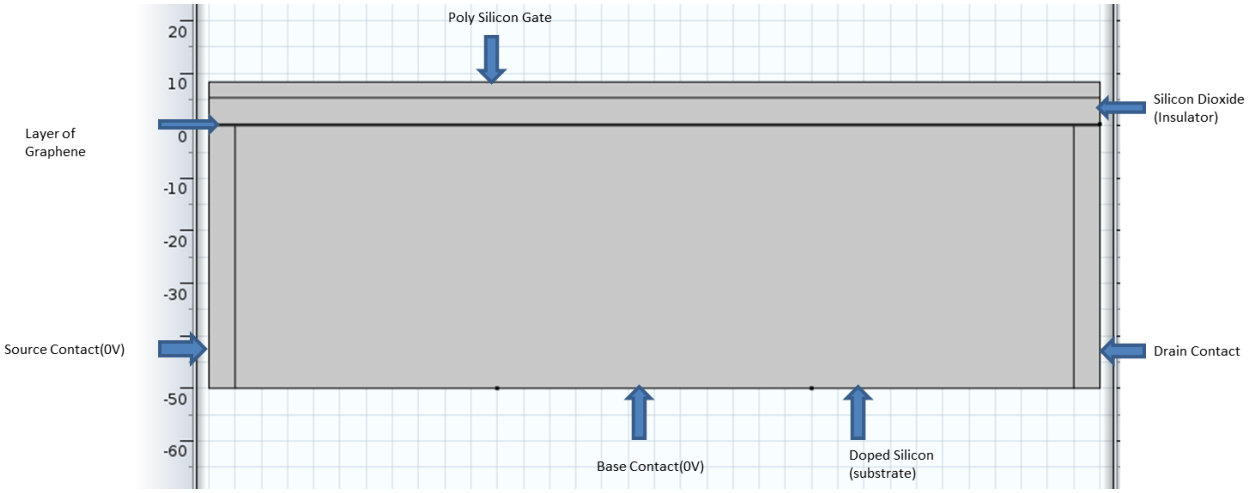

Figure 5 Simple structure

2.4 COMSOL Mesh

COMSOL offers a few meshing options such as triangular, quad, and mapped meshes. When it comes to a 2-dimensional analysis, COMSOL recommends a triangular mesh to be used for faster convergence and more accurate results. The mesh is a very sensitive parameter in COMSOL that can change drastically if not used correctly [12].

In the transistor design using a coarse mesh is not desired because the mesh points can be too large where the triangles itself can be seen in the surface plots (see *Figure 6*). This causes a bad approximation of the mesh points that are next to each other. But one benefit of

using a coarse mesh is the short computation time of 2 minutes (6,997 mesh points approximately), this is beneficial when a fast result is needed. When a more accurate result is needed a more uniform dense mesh is recommended, this uniform dense mesh increases the computational time to 30 minutes (see *Figure 7*). The increased computational time is due to the increase in mesh points which for a uniform dense mesh is approximately 10,266 points. The big drawback of using a denser mesh is the lack of resources when it comes to computing extremely fine meshes. For some extreme uniform mesh cases where the mesh size is too small simulation times can take up 24 hours (approximately 60,000 mesh points).

The greatest challenge in simulating the characteristics of the transistor is determining an appropriate mesh size. For the most accurate results, each mesh triangle would have to be the same size as an electron. This presents a problem because according to the classical theory, the radius of an electron is $2.8179*10^{-15}$m. The computational time for a mesh point that small is incalculable to determine how long COMSOL would take to produce a result. A method to reduce the computational time is by varying the size of mesh in different parts of the transistor where having a dense mesh may not be as imperative as in other areas (see *Figure 8*). Using this the computation time is reduced to 16 hours which is approximately 22,911 mesh points. For example, having a dense mesh in the graphene layer and a fine mesh in the other components provides an equivalent accuracy or greater accuracy while decreasing the computation time. The substrate is an area where a dense mesh is not as imperative as compared to other areas and a less dense mesh can be used to save on computational time. The process of calculating a sufficient mesh size is an iterative process which is simulated until there is no significant change in the results.

An additional feature that assists with the result accuracy is the tolerance factor of the simulation; this determines how close the previous results are in comparison to the new results. The results can be improved by reducing the tolerance factor to very small factors, but this can also increase your computational time. For a pictorial representation of the mesh points against computational time and memory usage, see *Figure 9* and *Figure 10*. The smaller the number of mesh points the less resources are needed and the computational time is decreased.

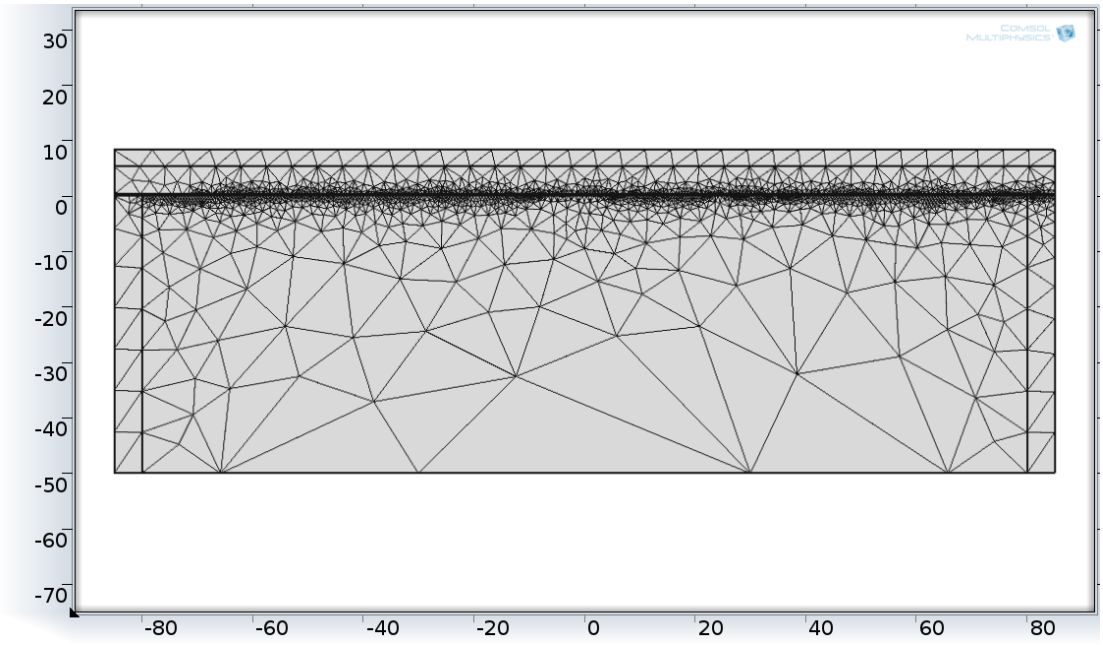

Figure 6 Coarse mesh

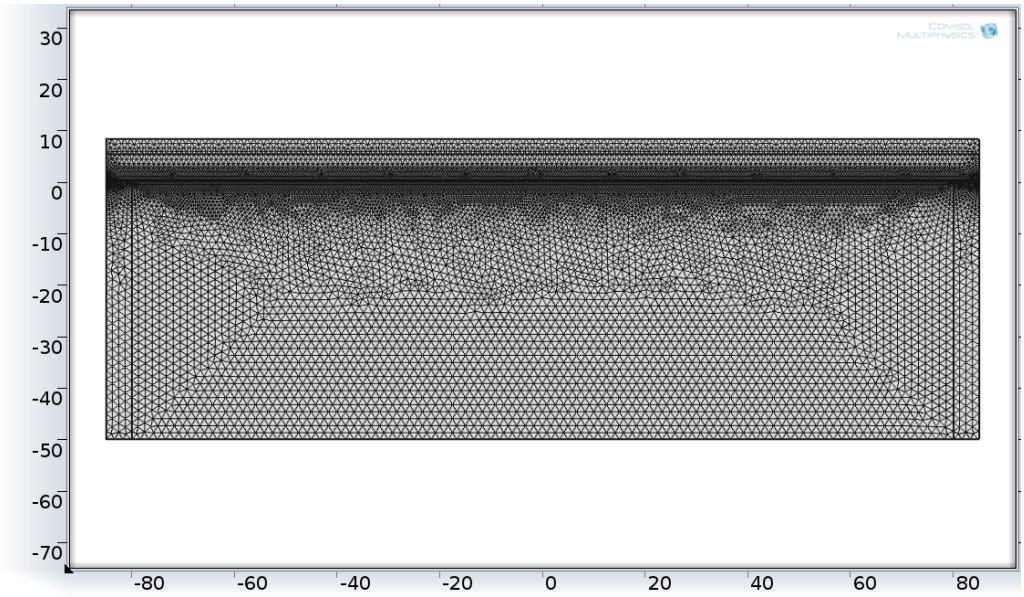

Figure 7 Dense mesh

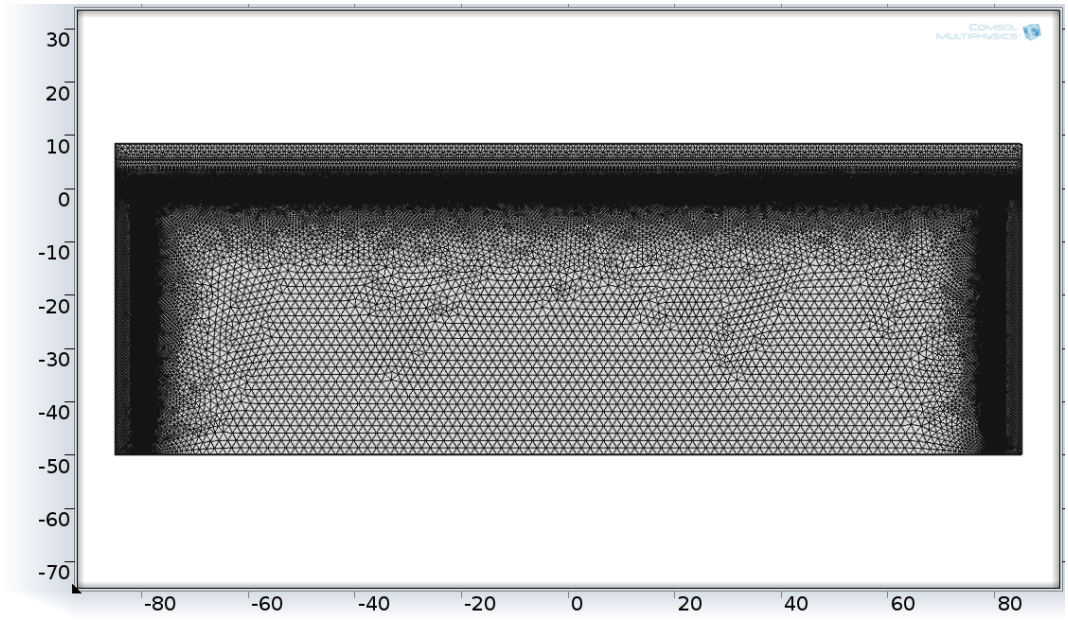

Figure 8 Varied mesh sizes

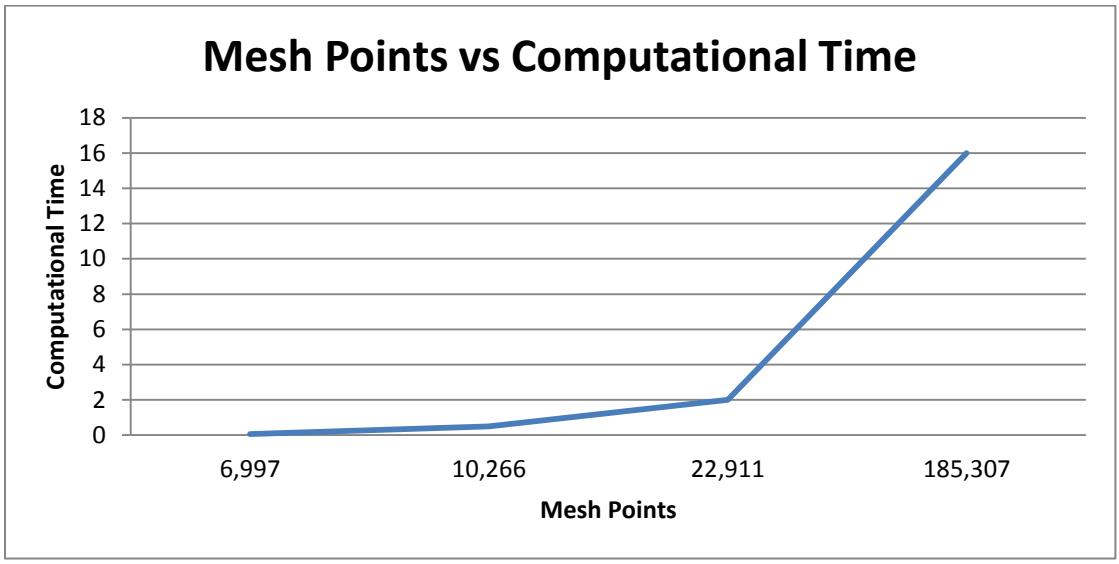

Figure 9 Mesh points vs computational time

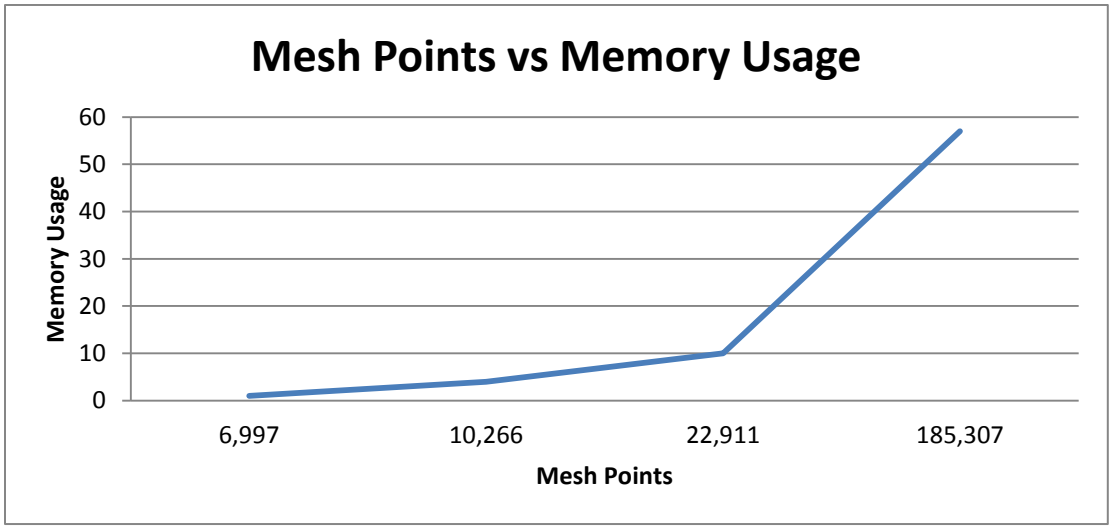

Figure 10 Mesh points vs memory usage

CHAPTER 3

GBFET Analysis without Substrate

Initially, an analysis was performed on the GBFET without the substrate. This analysis is necessary to determine how the carrier densities are affected inside the graphene layers alone and also to serve as a comparison to the MATLAB results.

3.1 Electric Potential

COMSOL computes the electric potential using the electrostatics module which links to the semiconductor module. COMSOL assumes the FERMI level is set to zero this is due to the substrate and graphene having an electric potential of 0 V. When comparing the potential plots from both MATLAB and COMSOL, there is a difference in the assumption of what the FERMI level is set to. In the MATLAB, the FERMI level is set to approximately infinity. In COMSOL, the Fermi and the electron affinity are used to determine the potential in the material which is displayed as a negative number. The electric potential can be easily confused with the energy in the material due to the Fermi level. The electron affinity is directly related to the work function of the material which dictates how much electric potential is needed to attract electrons inside the material to the surface. The gate used in these models is a poly silicon gate which is a composed of silicon, which is heavily doped with electrons. By doping the gate the FERMI level has shifted more towards the conduction band making the gate more conductive. This also affects the electric potential plot by causing a shift in the potential of 0.5 V. Below is a sample plot of the electric potential:

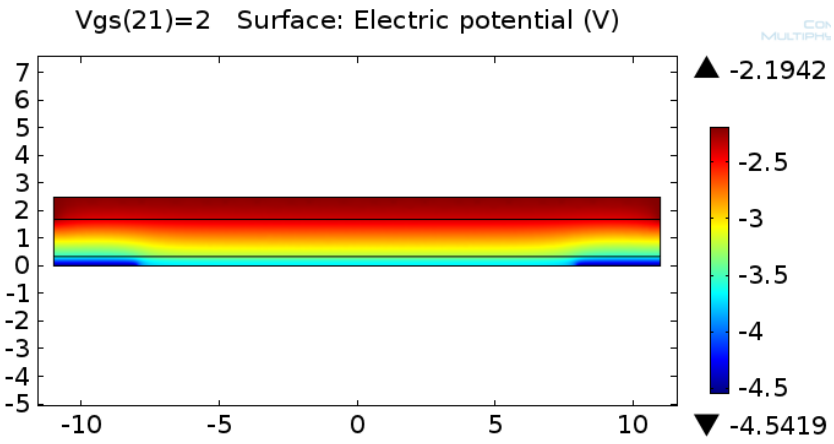

Figure 11 Sample electric potential

In the structure, the top layer is the gate with a potential of 2 V applied to the gate. Next, there is an oxide layer and last is the graphene layer. In this layer, there are two contacts in the furthest corners of the layer with equal potential of 0 V applied. In this model, the electron affinity of the graphene is 4.55 V and as stated the Fermi level is set to 0V.

3.2 Initial Baseline Analysis

First in the experimentation, a 2D model which consists of the gate, silicon oxide, and a small Graphene layer is being used (see Figure 13). In this simplified model, an accurate characterization of the graphene layer can be observed, which also can be used to compare with the MATLAB results (Figure 12). According to the MATLAB results the estimate electron concentration is 6.39E20 1/cm3 which is comparable to the COMSOL results. This is important to ensure the COMSOL results are reasonable in terms of accuracy.

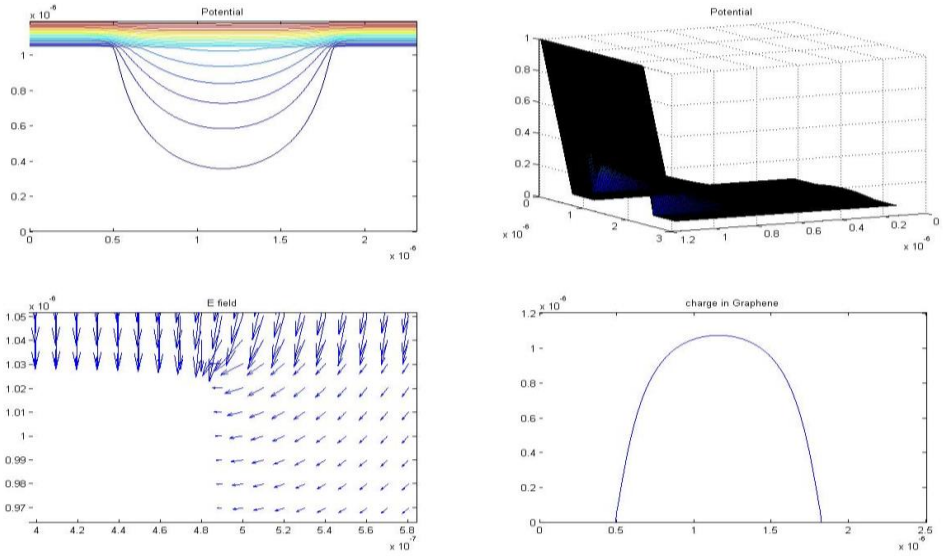

Figure 12 MATLAB results

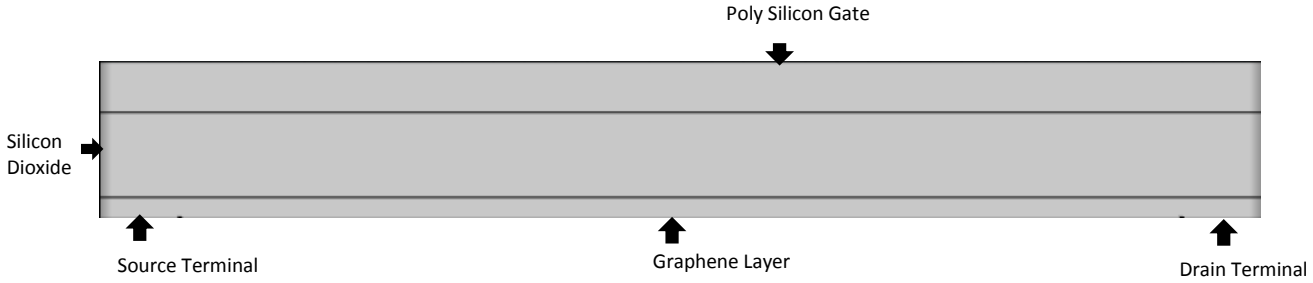

Figure 13 Structure of the gate, ilicon oxide, and graphene

Figure 13 displays the structure that was used in COMSOL to observe the behavior of the carrier concentration. Using this simplified model, the electron and hole concentration can be observed to determine if COMSOL is performing the accurate simulations. In this analysis, the potential that's applied to the source and drain are kept constant at 0 V for consistency and a sweep is performed at the gate. The mesh that was used is a triangular mesh which is significantly smaller in the graphene layer. See *Figure 14* to observe the distribution of the mesh points in this model. The graphene layer requires a larger amount of mesh points to have a better approximation of the carrier concentration due to the smaller dimensions of the layer.

Furthermore, it is imperative because the terminals are located on the graphene layer this produces more accurate results.

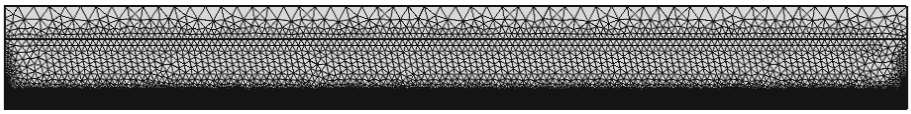

Figure 14 Distribution of mesh

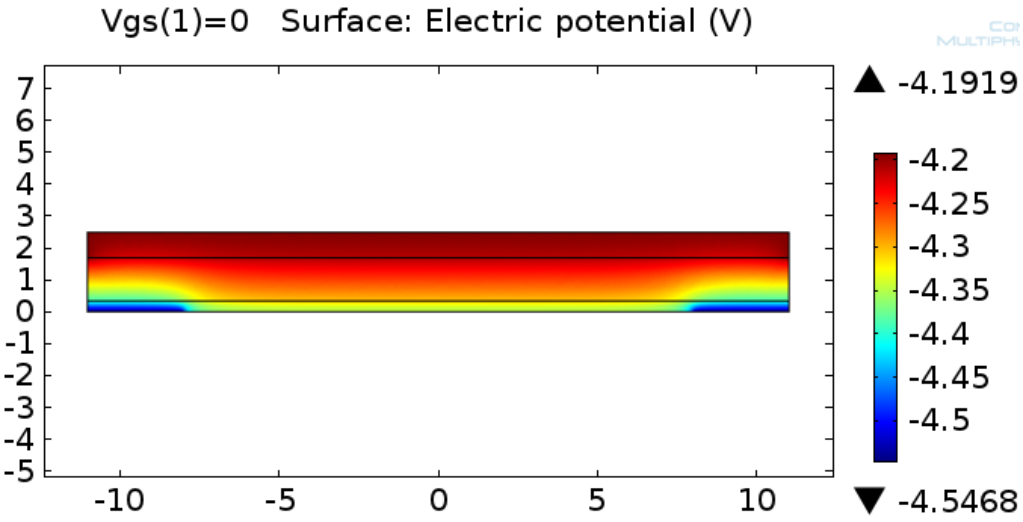

Figure 15 Electric potential Vgs=0 V with no substrate

In *Figure 15*, this plot displays the electric potential across the structure with equal potential of 0 V applied at the terminals and gate. Observe the potential is greater at the gate due to the doping profile and the electron affinity of the gate in comparison to that of the graphene layer. This is caused by the different electron affinity which for silicon is 4.05 V and for graphene is 4.55 V. Next, a 1 V potential is applied to the gate which changes the potential distribution plot. See *Figure 16*, to observe how the potential propagates through the gate, oxide, and the graphene layer.

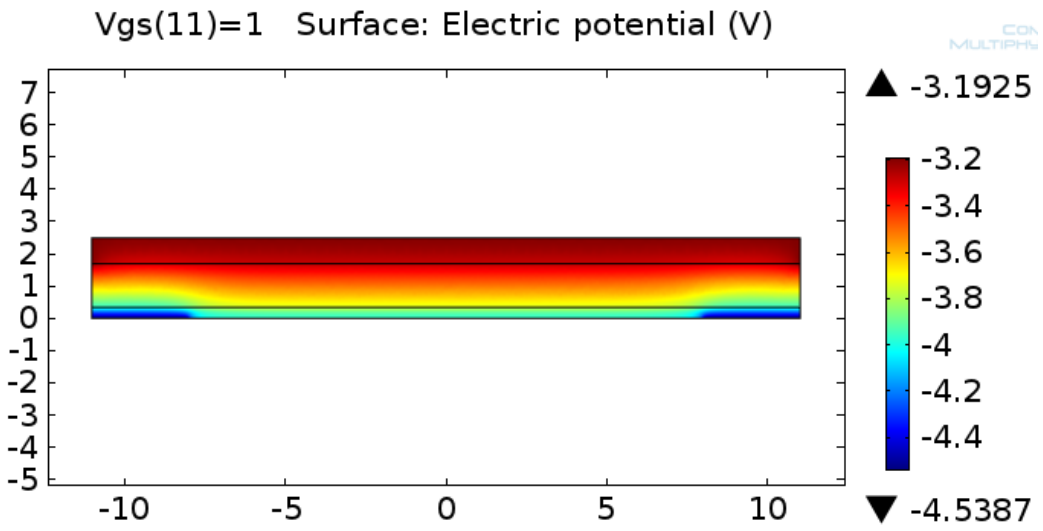

Figure 16 Electric potential Vgs=1 V with no substrate

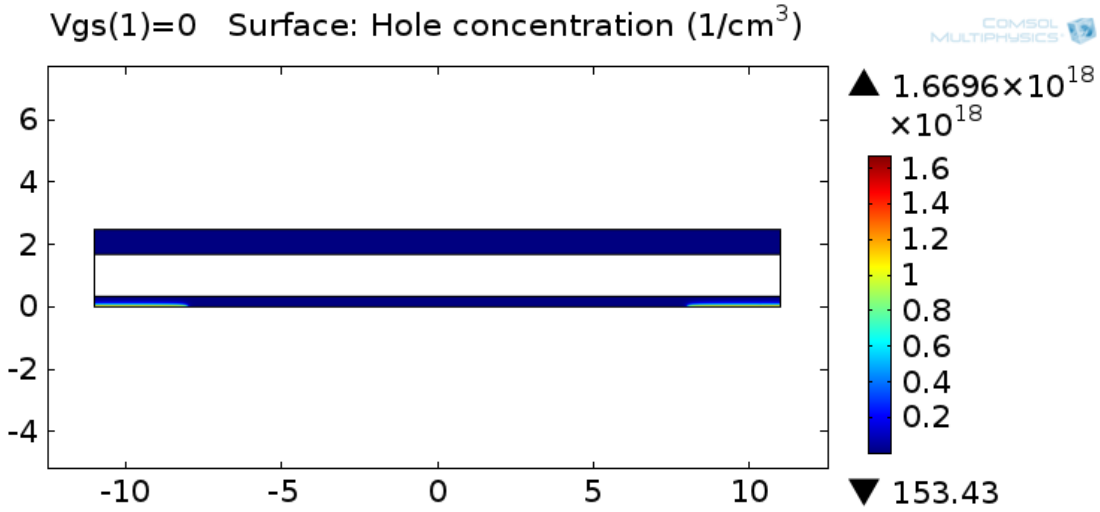

Figure 17 Hole concentration at Vgs=0 with no substrate

Figure 17 displays the hole concentration of the structure with the same potential conditions as before. As anticipated the hole concentration in the graphene layer is higher due to the 0 V potential that is applied.

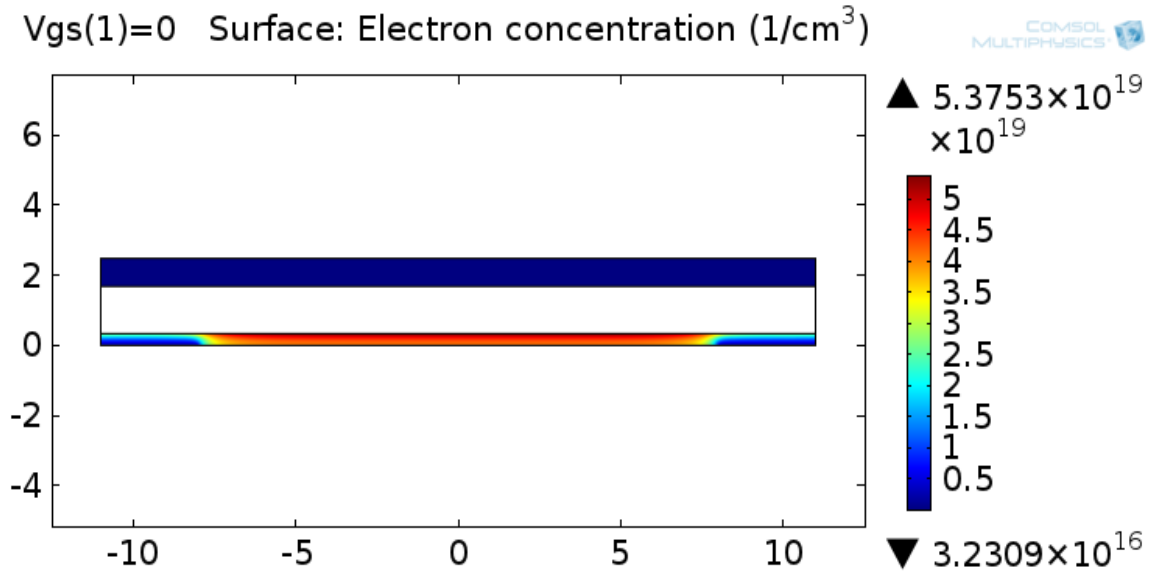

Figure 18 Electron concentration at Vgs=0 with no substrate

Figure 18 displays the electron concentration behavior in the structure with the same conditions as stated above. Furthermore, as expected, the electron concentration is not as dense in the middle of the graphene layer due to the potential of the gate. By applying a greater potential at the gate the electron concentration will change, and it will become denser in the center of the graphene layer. Electrons according to the basic theory are attracted to a higher potential, and holes are attracted to lower potential. This is displayed in the next analysis that is performed with a 1 V potential applied to the gate. See *Figure 19* and *Figure 20*, these figures depict a smaller hole concentration and a greater electron concentration inside the graphene layer. There should be no electron or hole concentration inside of the oxide layer because it is an insulator which means it has no carrier mobility nor the density of states [13].

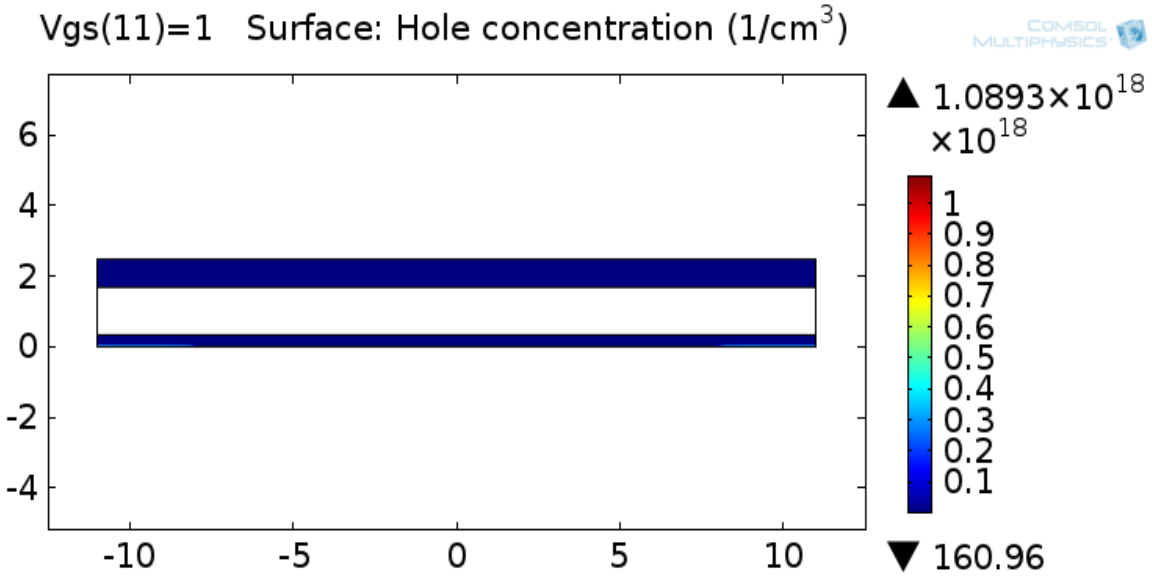

Figure 19 Hole concentration at Vgs=1 V with no substrate

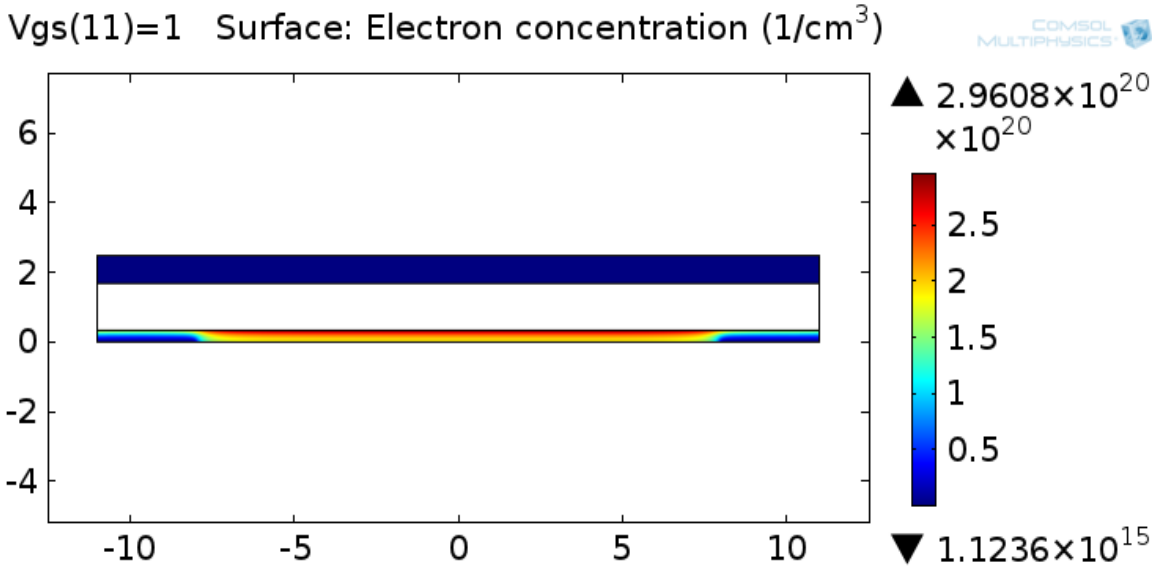

Figure 20 Electron concentration at Vgs=1 V with no substrate

3.3 Energy Bands

Important parameters that COMSOL calculates is the energies throughout the structure as a part of the module. The following equations depict how the energy of the valence, and conduction band were computed in COMSOL. Additionally, the total energy of the electrons and holes were computed with respect to the band edge [12].

$$E_C = -q(V + X) \tag{10}$$

$$E_V = -q(V + x + E_g) \tag{11}$$

$$E(k, r) = E_C(r) + W(k, r) \tag{12}$$

$$E_h(k, r) = E_v(r) + W_h(k, r) \tag{13}$$

In practical simulation, the energy in the structure is subject to change within a space. Therefore, it becomes imperative to define the energies with respect to reference energy [14]. COMSOL simplifies this boundary condition by making the reference energy the same as the Fermi level energy. Furthermore, it is important to note that in COMSOL, the temperature is used to determine the equilibrium Fermi's level energy. The energy diagram is easily computed for this structure because it lacks a depletion region and no energy band bending is anticipated. The Energy Band data is plotted by using a cut line through the middle of the structure. Thus, the plot displays the energy versus the length of the cut line from left to right (see Figure 21). COMSOL approximates the energy bands and the Fermi levels of the materials in the structure. When an equal potential is applied to the gate, source, and drain, the Fermi levels of the electron, and holes should be approximately equal. This simulation does not include the effects of band gap narrowing due to external stimulations such as temperature. As expected the energy band gap of silicon is 1.1 eV and for graphene is 0 eV. In Figure 22, this observation is displayed and

Figure 23 displays another energy band diagram is plotted with a 1 V potential being applied to the gate. When a potential is applied the Fermi level for the electron and holes will vary depending on the size of the density of states of each carrier this is what COMSOL called an intrinsic Fermi level.

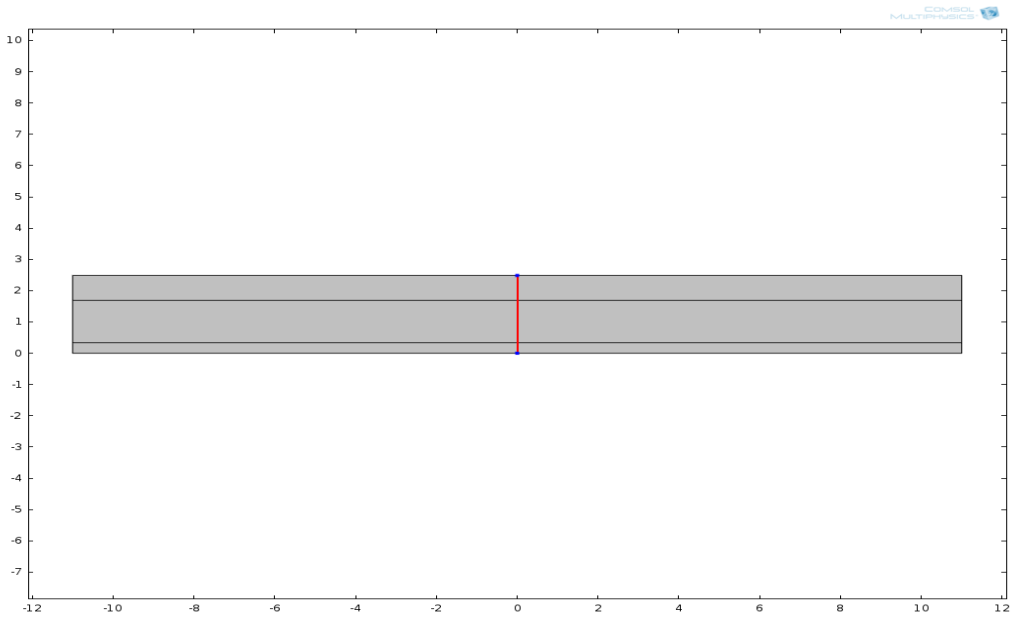

Figure 21 Using a the cut line tool

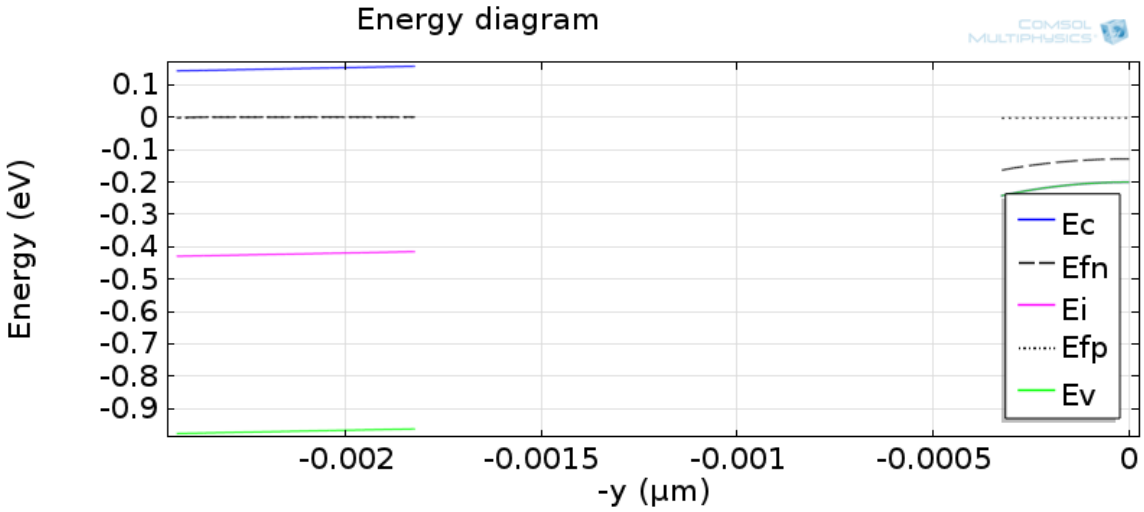

Figure 22 Energy plot at Vgs=0 V

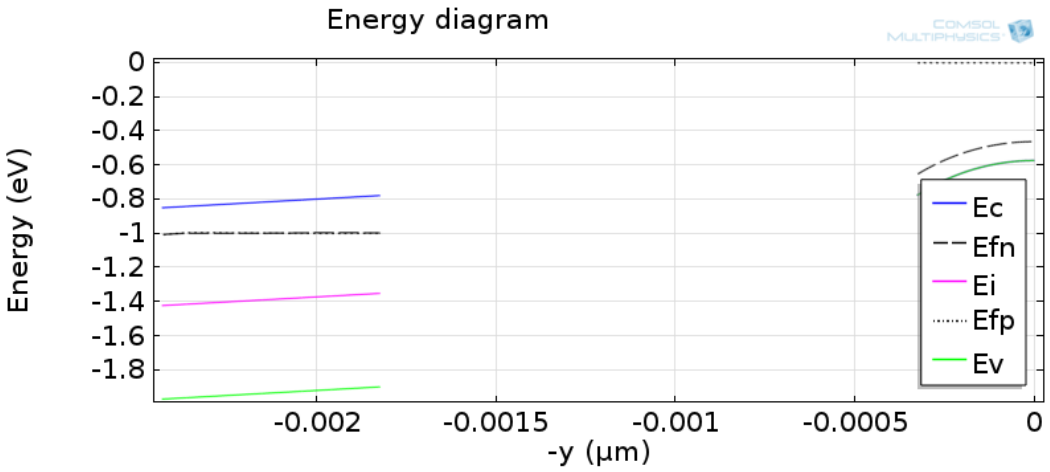

Figure 23 Energy plot at Vgs=1 V

3.4 Graphene Layer's Carrier Concentration

The graphene layer inside has many appealing features to the Electrical Engineer, but the important aspect is. How can it be controlled? The greatest challenge with graphene is trying to determine the best use of the graphene in any possible design. This is why a baseline of the transistor without the substrate layer was required. Some modifications were made in COMSOL's electron concentration equation to use the incorporate the unique massless behavior which is a better approximation for the graphene layer. Using the Cut Line feature a slice was taken through the middle of the graphene layer (see *Figure 24*). Using the Cut Line, the electron and hole concentration plots were generated to ensure the graphene layer values were reasonable in comparison to the MATLAB results. See *Figure 25,* and *Figure 27* to observe when a 0 V potential is applied to the gate. The hole concentration is great because the holes are being attracted to the lower potential, and the electrons are repelled. The inverse effect is expected in the electron concentration plots when a higher potential is applied to the gate. See *Figure 26*, and *Figure 28* which displays how the electrons are repelled at the lowest potential at the gate and attracted at the higher potential.

Using these characteristics the on/off ratio can be approximated. See *Figure 29*, this figure displays the summed value of the hole and electron concentration inside the graphene layer. This plot also displays the off region inside the layer to be approximated -0.4 V. This does not mean that there is no conductivity at -0.4 V, this means the minimal conductivity occurs at that potential. This plot is useful in estimating the drain current based on the magnitude of the combined concentration plot. It is apparent that the graphene can be used in transistor devices, but for the moment it can only be used in specific areas where the on/off ratio isn't an important factor.

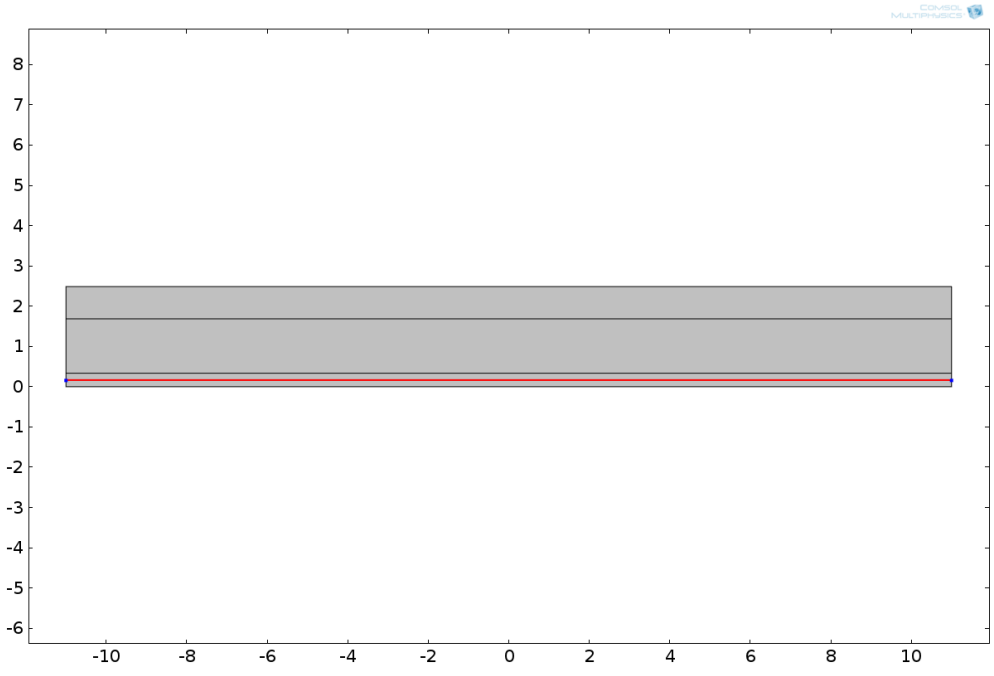

Figure 24 Cut line through the graphene layer

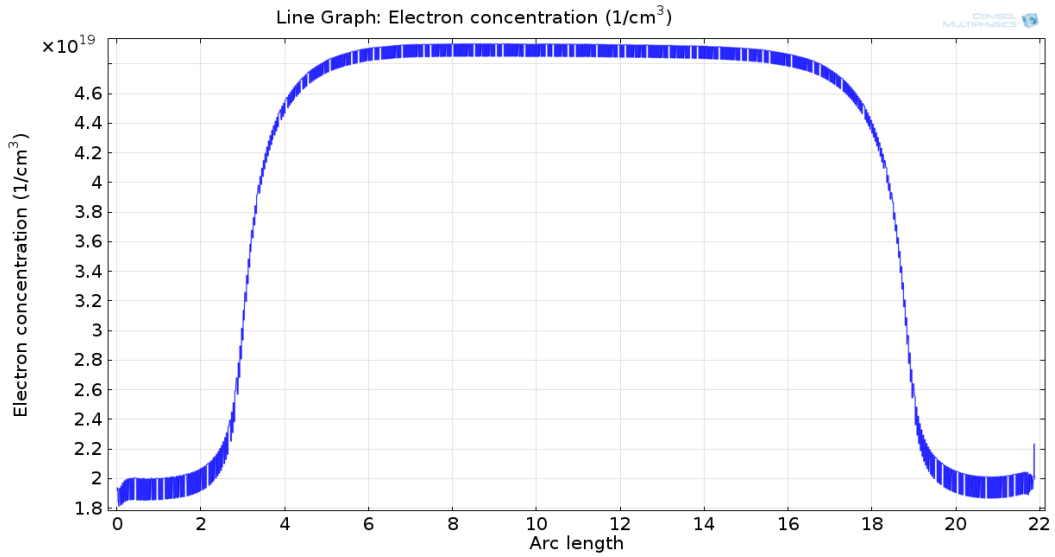

Figure 25 Electron concentration in graphene at 0 V applied at the gate

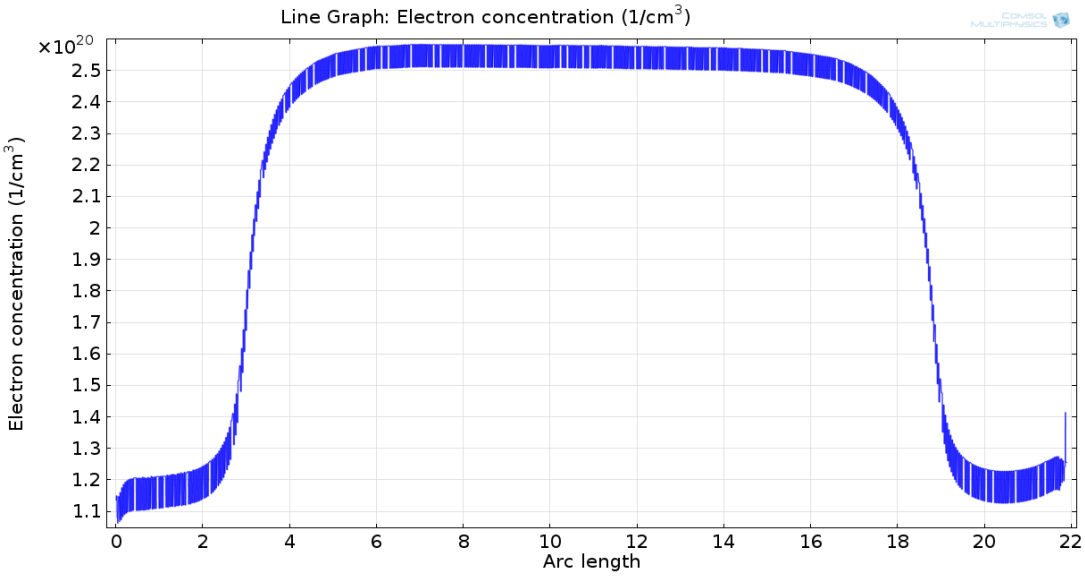

Figure 26 Electron concentration in graphene at 1 V applied at the Gate

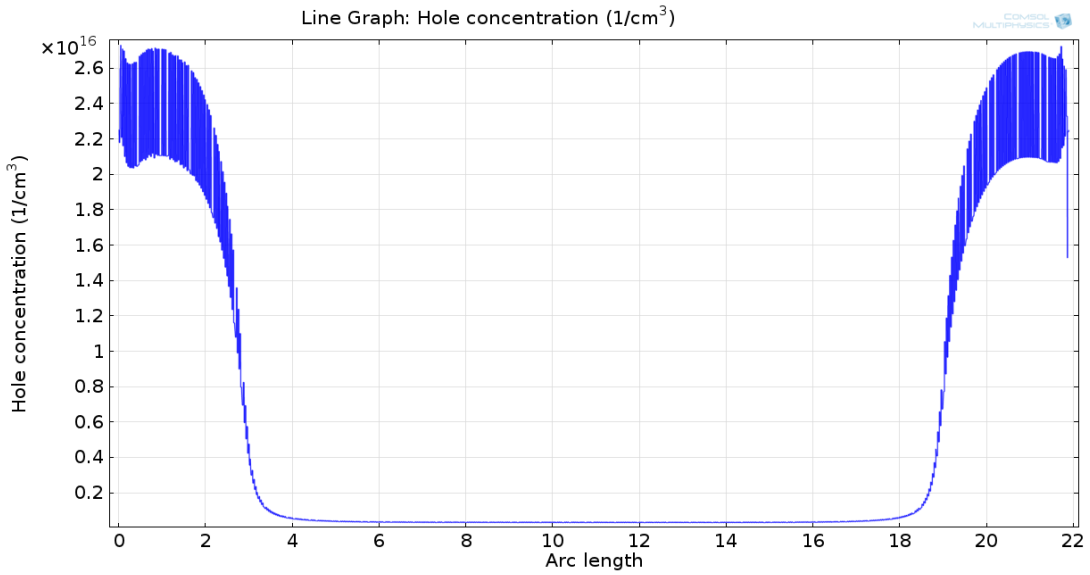

Figure 27 Hole concentration in graphene at 0 V applied at the gate

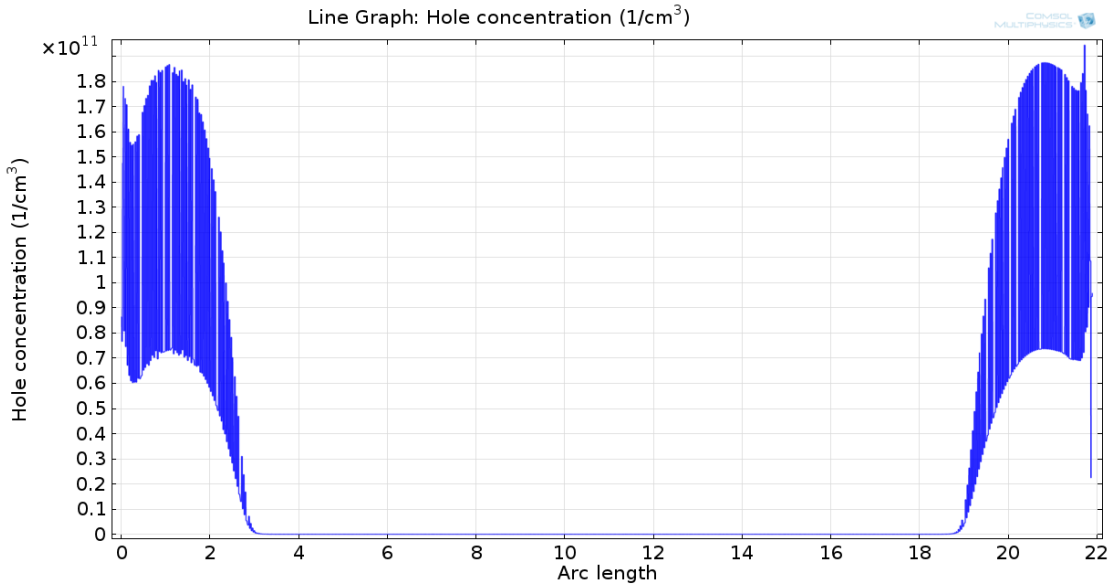

Figure 28 Hole concentration in graphene at 1 V applied at the gate

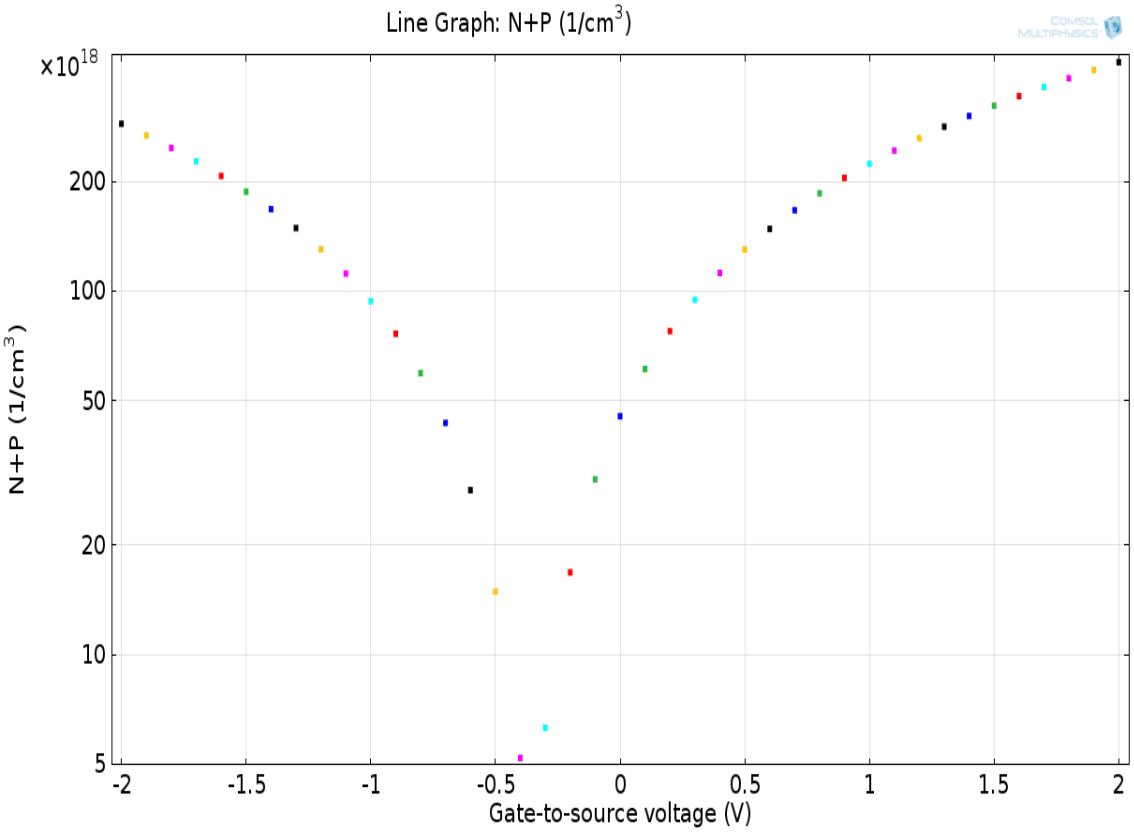

Figure 29 Hole and electron concentration in the graphene layer

CHAPTER 4

Computation of GBFET

In this section, a full analysis was performed on the GBFET to observe and record the characteristics of the transistor design. A full transistor design is used, including a doped substrate.

4.1 GBFET with an Undoped Silicon Substrate

The substrate is introduced as a controller of the graphene to vary the electron and hole concentrations. *Figure 30* displays an updated structure of the transistor, which includes the silicon substrate. In this simulation, the goal is to use the silicon to maximize the use of the graphene layer in different applications in the electrical Engineering arena. The substrate in this model is a made of not doped silicon (dielectric) which is also acting as an insulator, only the square in the middle is the substrate. The rectangles in the corners of the substrate are being used as the source and drain terminals which are at a 0 V potential. The body of the transistor, which is the bottom center of the structure has no potential applied to the terminal (grounded).

Using this structure, a variable sweep was performed at the gate. *Figure 31* displays an Electric Potential plot with 0 V applied at the gate. A 0 V potential on the gate attracts the holes from to the lower potential from the substrate which causes a higher hole concentration inside of the graphene layer. Furthermore, the opposite effect happens to the electron concentration where the electrons are repelled from the lower potential. See *Figure 32* and *Figure 33*, it is apparent that the electron concentration is significantly lower than the hole density due to these effects.

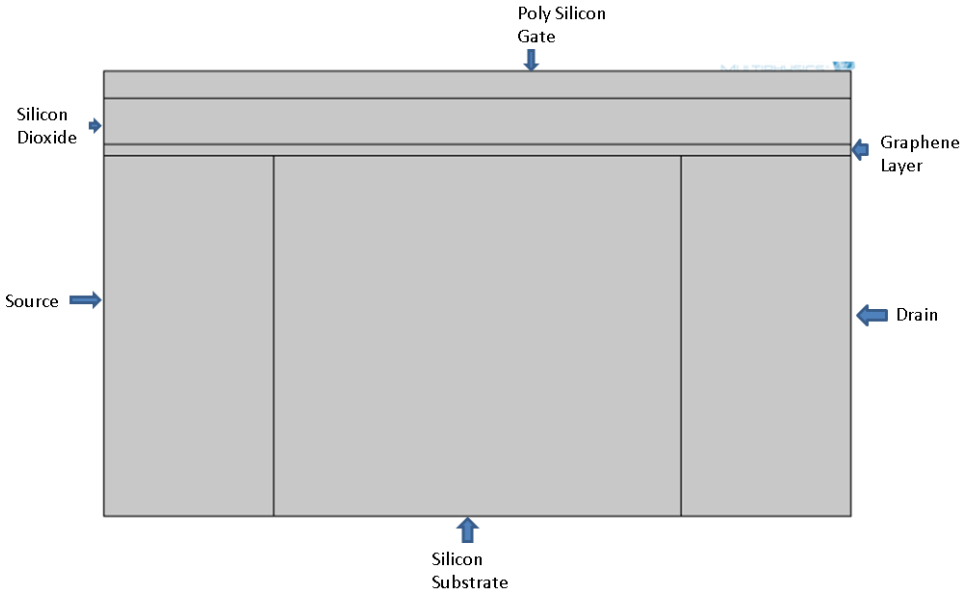

Figure 30 Transistor structure with not doped substrate

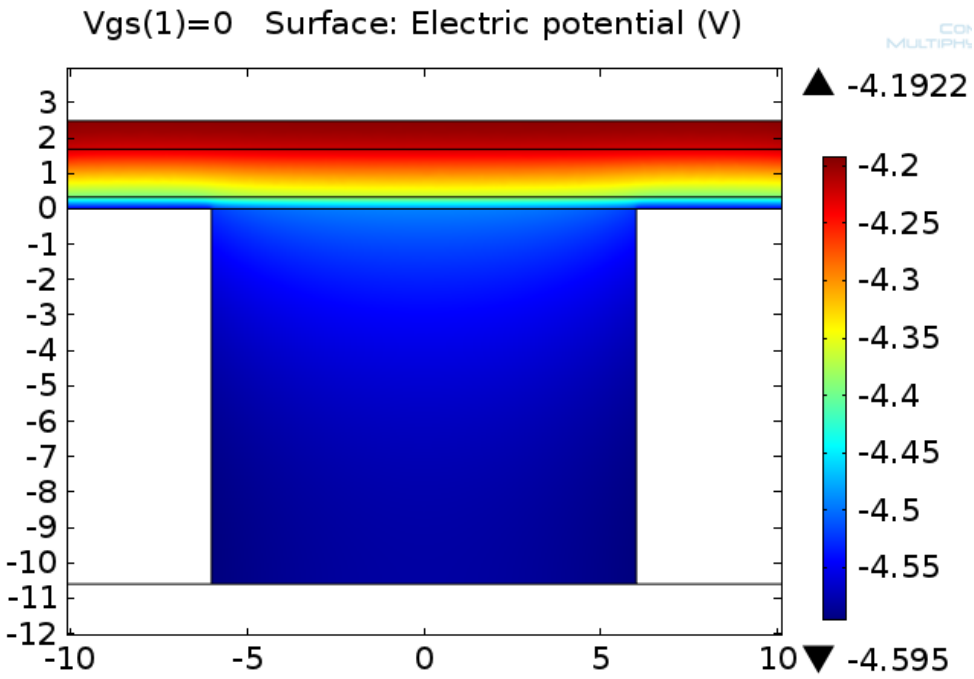

Figure 31 Electric potential at 0 V at the gate

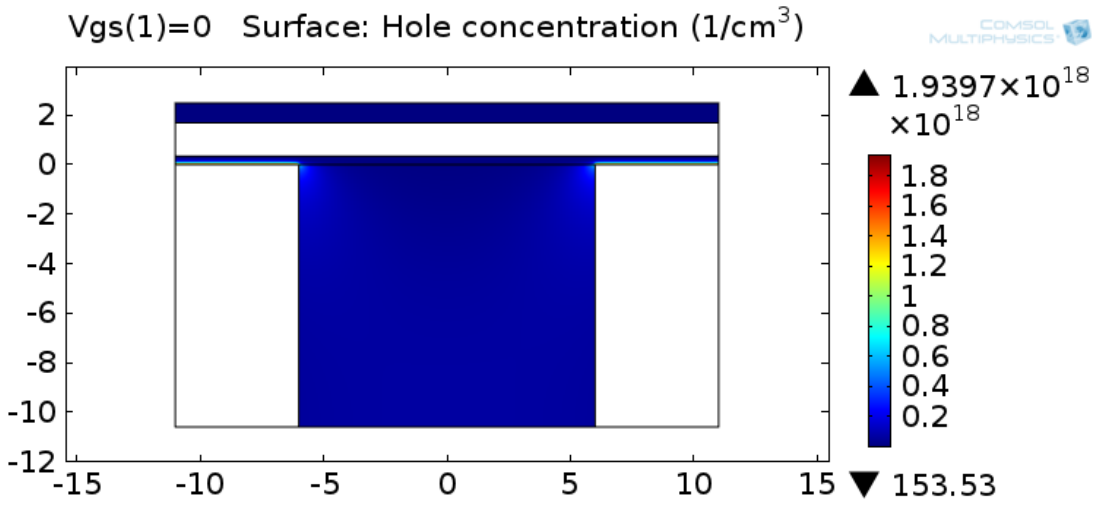

Figure 32 Hole concentration at 0 V at the gate

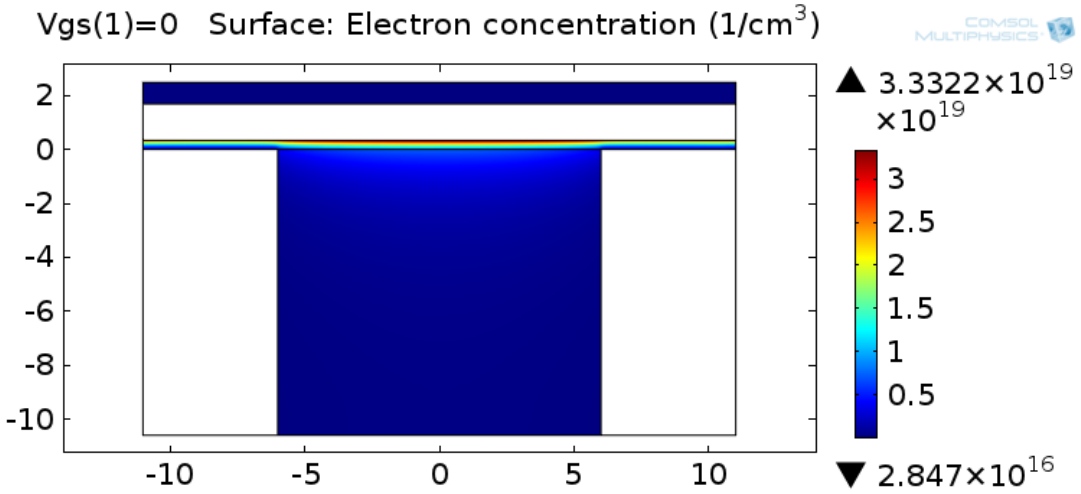

Figure 33 Electron concentration at 0 V at the gate

See *Figure 34*, *Figure 35*, and *Figure 36* which displays plots on the electric potential, hole and electron concentration at 1 V potential at the gate. Electrons are attracted to the center of the graphene layer due to the higher potential applied to the gate.

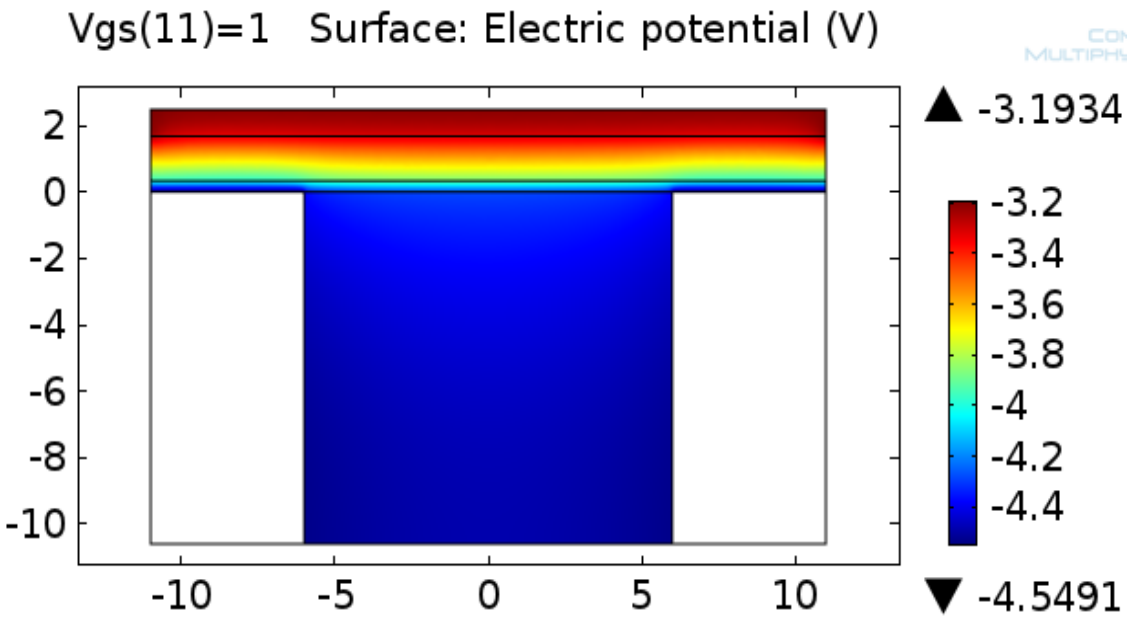

Figure 34 Electric potential at 1 V at the gate

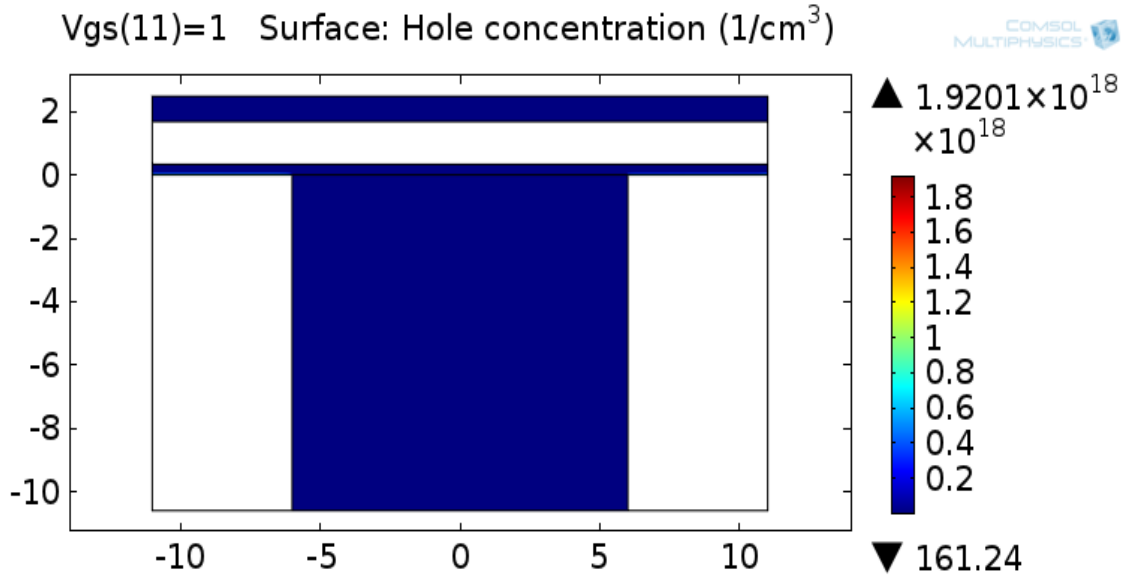

Figure 35 Hole concentration at 1 V at the gate

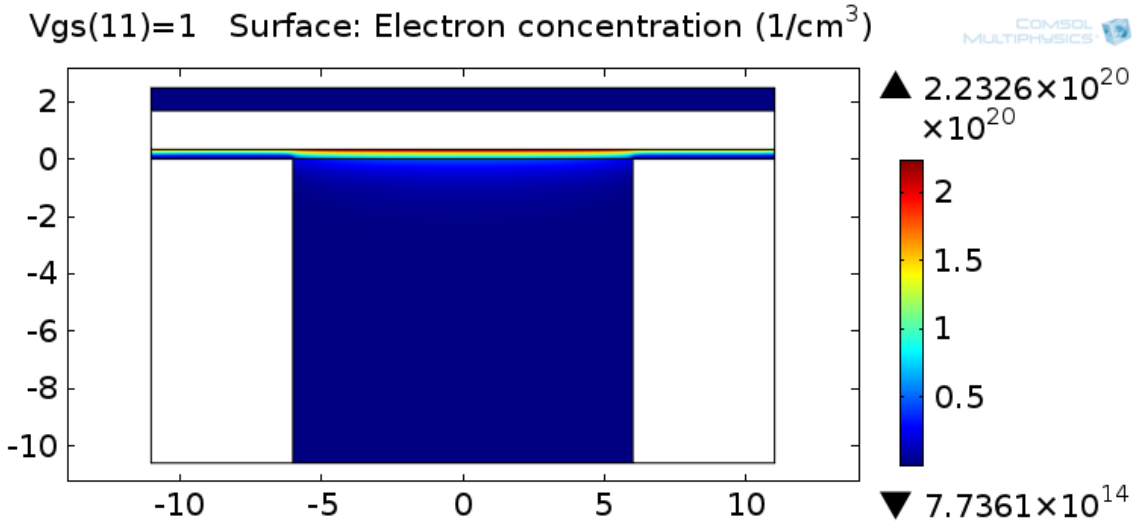

Figure 36 Electron concentration at 1 V at the gate

4.1.1 Energy Diagram of transistor with substrate. Using the cut line feature of COMSOL (See Figure 38) the energies are plotted first when the gate potential is 0 V and second when the gate potential is 1 V (See Figure 39). The difference in this energy plot is the substrate area which is acting as an insulator, so no band bending is expected to occur as compared to the poly silicon gate. Due to the charge conservation feature that's being used for the silicon dioxide insulator, the electron concentration, hole concentration, and energy are not computed because it's not being used in the semiconductor module. Therefore, there no energy data that is computed through the insulator. The FERMI level inside the poly silicon gate is shifted, which means more electrons are in the conduction band and less in the valence band. This is achieved by doping the gate with more electrons. This causes the gate to act more as a conductor.

After the gate, there is an oxide layer which has a band gap of 9 V, but due to COMSOL's charge conservation feature, it is left blank. Since the gate potential is the same as the source and drain potential, it is expected that the FERMI level is the same in both the gate and substrate layers. In this simulation, the substrate layer is not doped and therefore, the

additional electrons in the gate are transferred to the substrate to balance out the FERMI levels of the two layers. The same effect is not anticipated for the graphene layer due to the zero band gap characteristic of graphene.

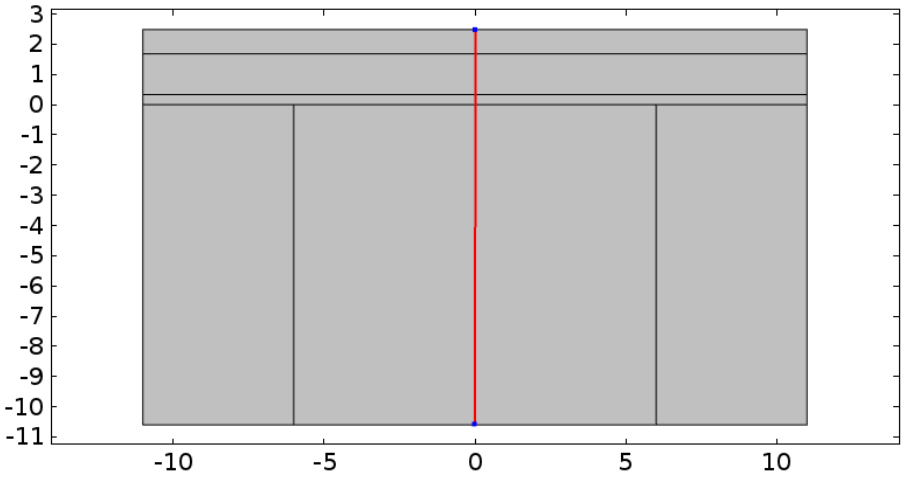

Figure 37 Cut line of the structure

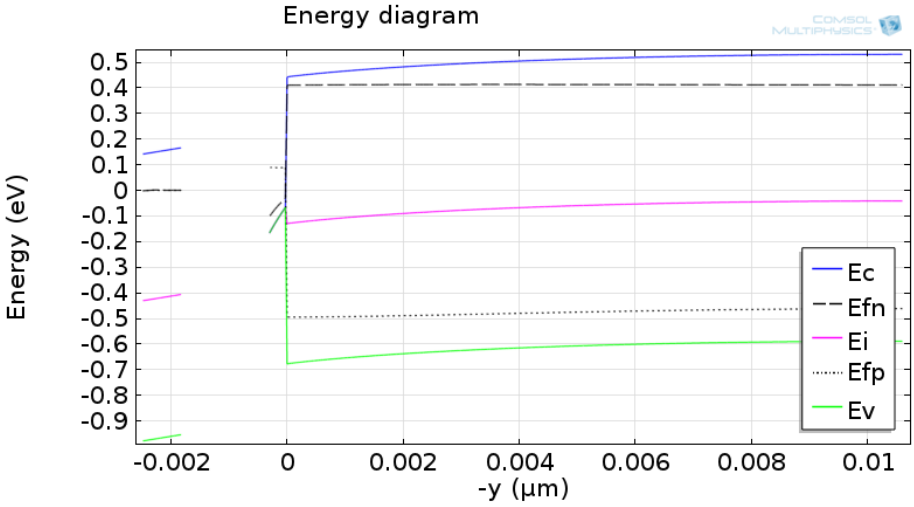

Figure 38 Energy plot of transistor structure at 0 V at the gate

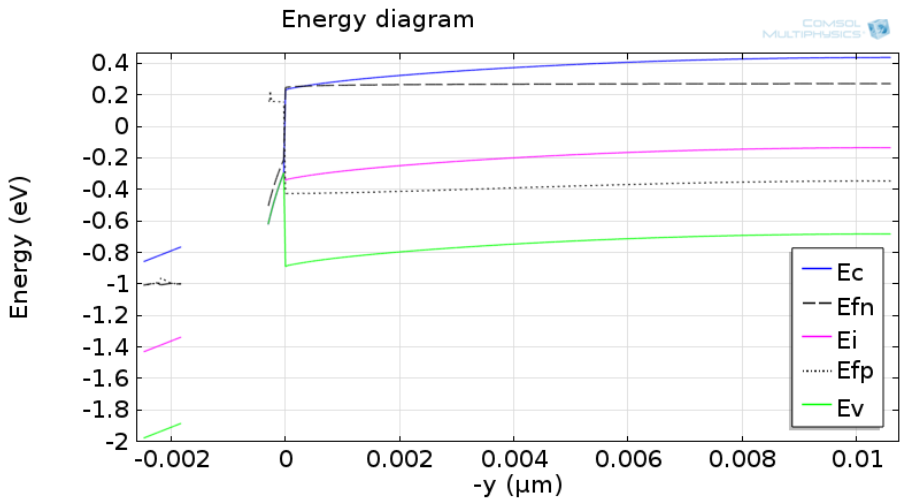

Figure 39 Energy plot of transistor structure at 1 V at the gate

4.1.2 Electron and Hole Concentration inside the Graphene layer. It is imperative to understand the behavior of the electron and holes inside the graphene layer. This analysis is an extension from the previous structure's simulation. The results are expected to be approximately the same because the substrate is acting like an insulator and thus depletion will not be created. See Figure 40 and Figure 42 to observe the electron and hole concentration inside the graphene layer with a 0 V potential at the gate. Furthermore, See Figure 41 and Figure 43 to observe the electron and hole concentration inside the graphene with a gate potential of 1 V. Lastly, Figure 44 displays the sum of both the electron and hole concentration.

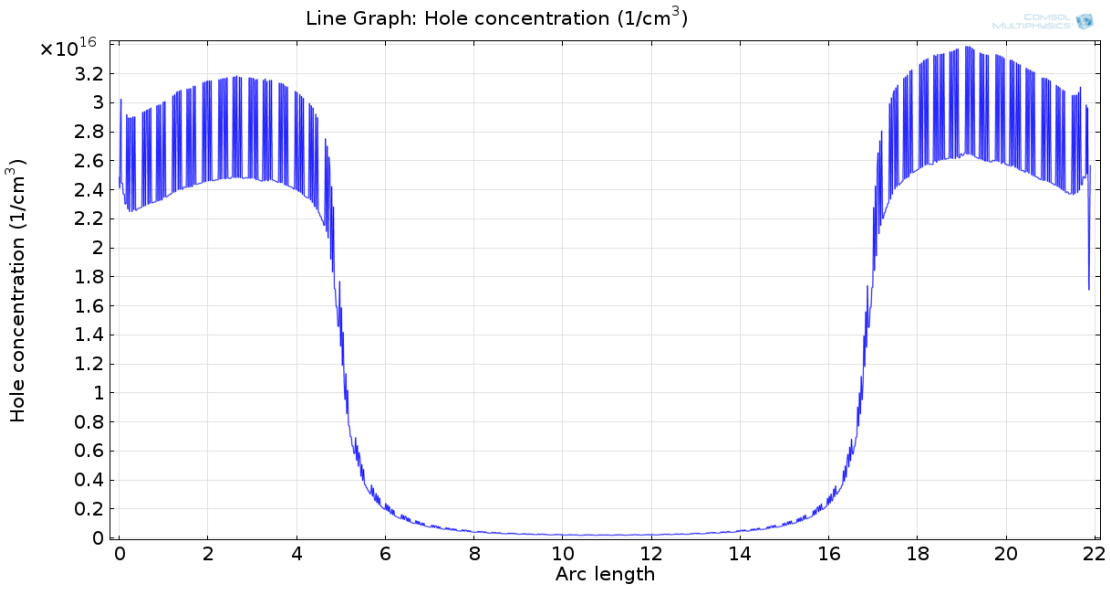

Figure 40 Hole oncentration at 0 V potential at the gate

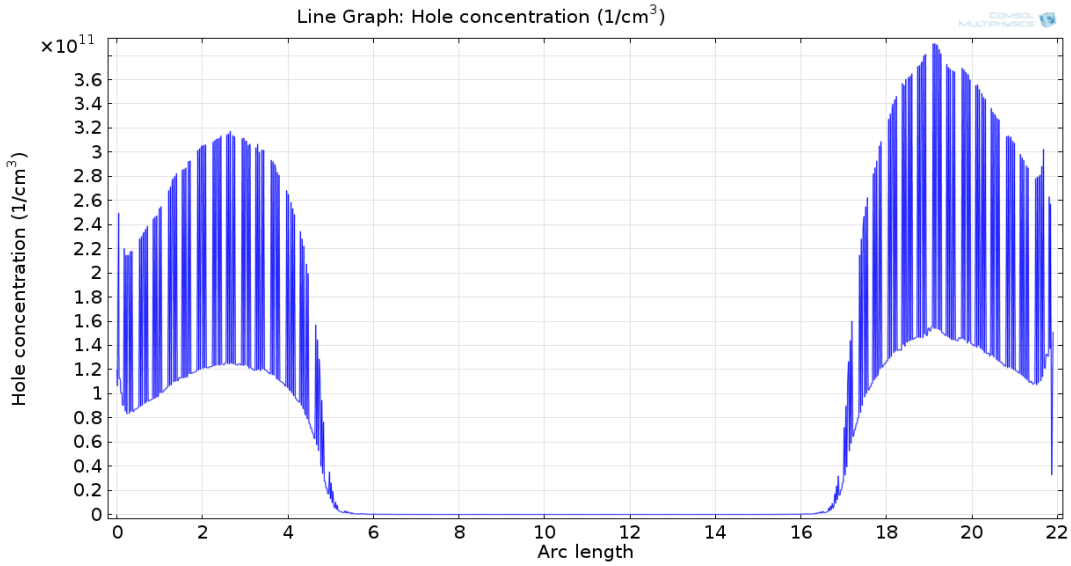

Figure 41 Hole concentration at 1 V potential at the gate

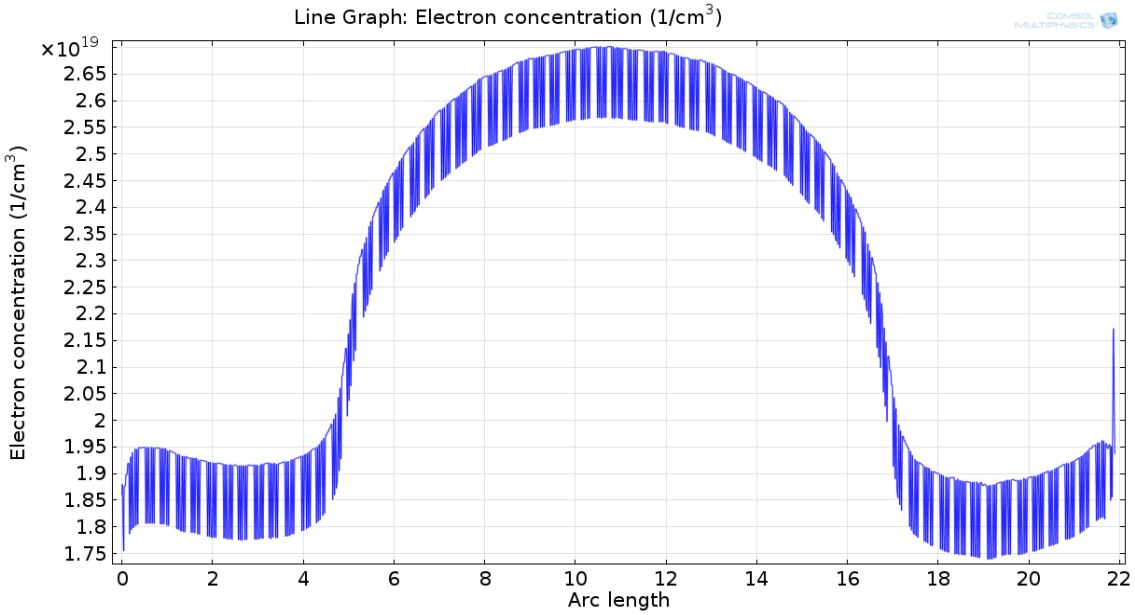

Figure 42 Electron concentration at 0 V potential at the gate

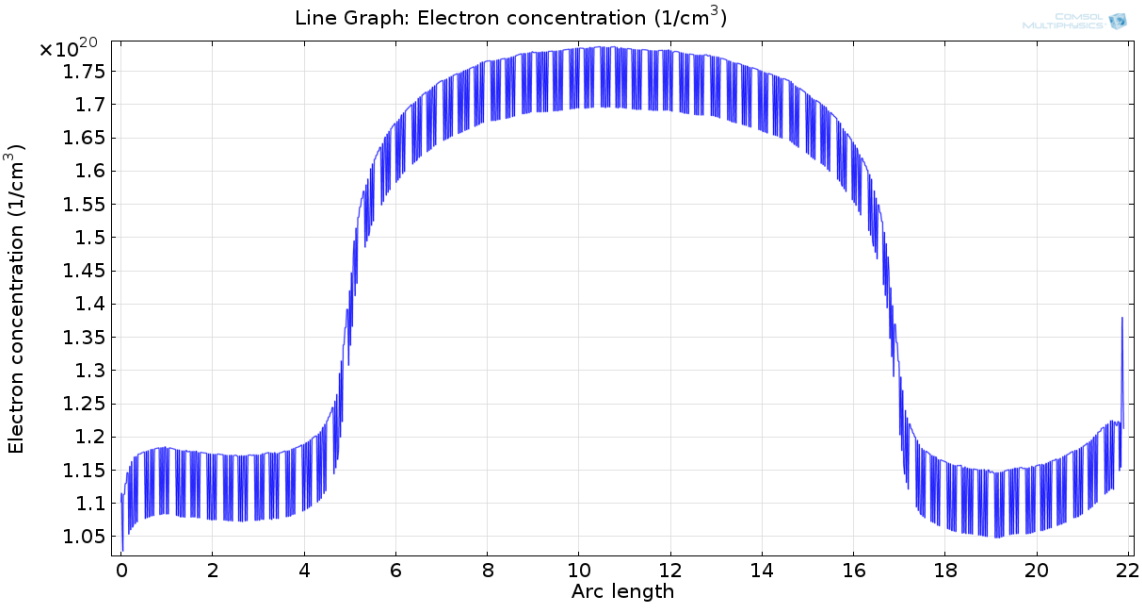

Figure 43 Electron concentration at 1 V potential at the gate

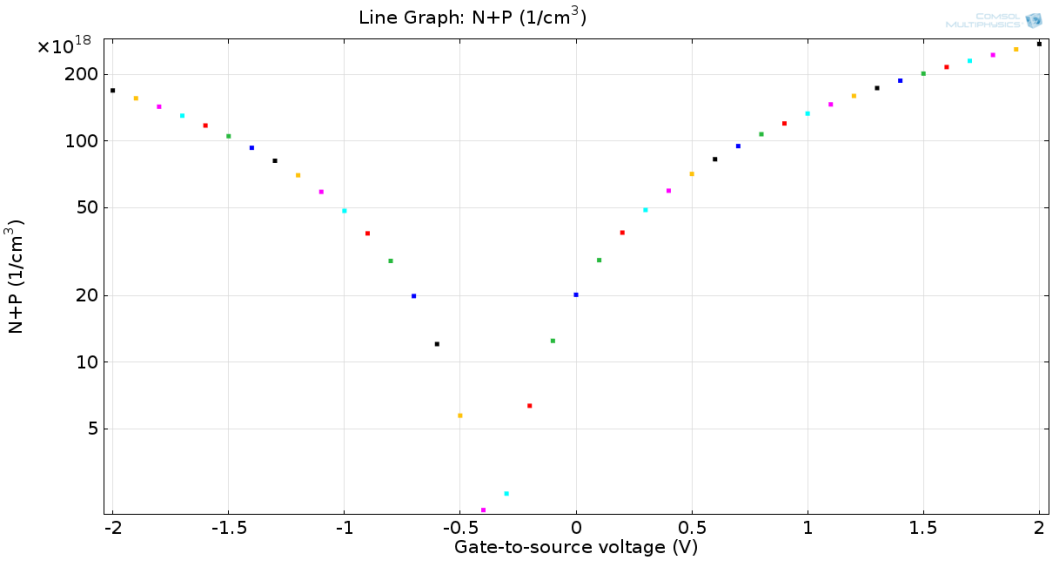

Figure 44 Electron and hole concentration

4.2 GBFET with a doped Silicon Substrate

The first two simulations were performed using a smaller structure to have more accurate comparisons between the MATLAB and COMSOL results. For this simulation, the structure is larger and represents the actual proposed size that is to be used which in turns makes the channel length longer and easier to obtain results. After observing the on/off ratio of the current transistor structure, it is apparent that the ratio can be improved through shifting the properties of the graphene layer. It is possible to shift these properties through doping. COMSOL has a convenient built-in doping model that was used in simulating the doping profiles of the models. In this simulation, the drain, source, and gate potential are set to 0 V potential. The doping profile used for this model is displayed in *Figure 45*, which effectively displays both the n doping as a positive number and the p doping as a negative number.

The “V” shaped doping profile is the proposed solution along with equal doping concentrations. The intent of having a higher p doping concentration in the middle is to balance

the higher electron concentration in the middle of the graphene layer. By using this doping profile, two pn junctions are created inside of the substrate area which is in contact with the graphene layer [15]. The doping profile below is a gradual V/U shape which created by using a modified Gaussian distribution function of the doping feature. This doping profile is used to create a high resistance which is considered the off-state inside the channel of the transistor this is due to the low carrier concentration in the graphene and substrate areas. When a high gate potential is applied to the gate, the pn junction becomes more of an nn junction where the conductivity is higher, which creates a low resistance (also known as the saturation region) which is the on state. This is also the case for the corners because it has a higher hole concentration at the corners to counteract the concentration with a high n type.

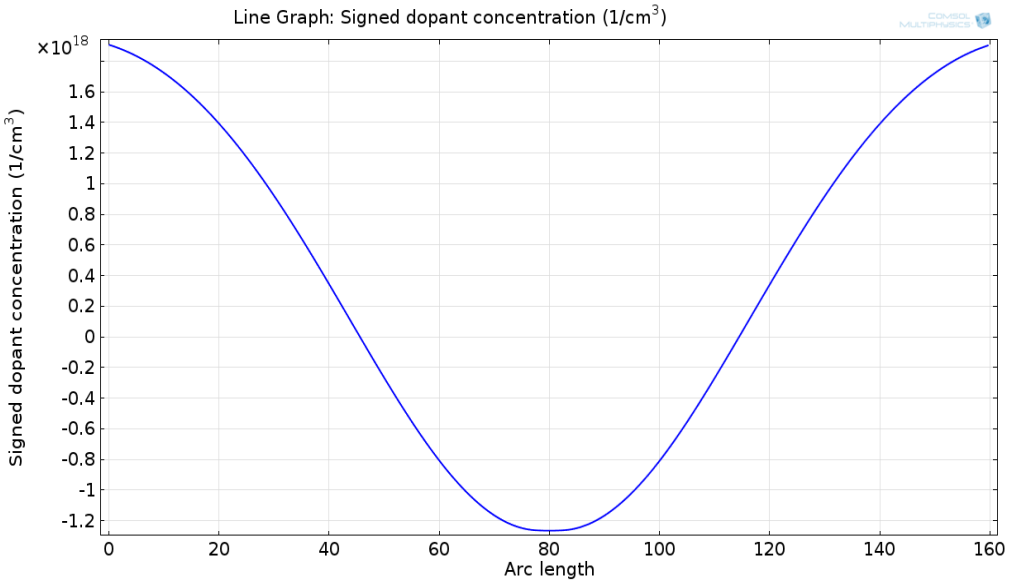

Figure 45 Gradual pn junction with NA-ND=2E18 1/cm^3 doping profile

4.2.1 Electric Potential and Carrier Concentration of the doped GBFET. The structure was changed to more accurately represent the model that is being proposed and to assure the simulations are easier to converge. At a glance, it is clear which areas are doped with n or p type in the electric potential plots. The center of the substrate is doped with p type, which makes it less conductive and has a lower potential than the areas that are doped with n type. By using this doping model a pn junction is created between the two doping concentration which in turn creates a depletion region [6]. This depletion region cannot be eliminated, but it can be varied in width depending on the drain and gate potential that's applied.

Another method of varying the depletion region is by changing the doping concentration to have been higher p region doping than the n region doping. This creates a larger barrier that would restrict the diffusion of carriers across the substrate. The electron concentration in the n region will start to diffuse into the p regions, and the majority holes start diffusing into the n region [16]. An electric field is induced by the positive and negative charges in the n and p regions near the pn junction area. This effect creates a space-charge region and since the space-charge region is depleted of any carriers, this is what causes the depletion region in the channel [5]. In this analysis the source, drain, body, and the gate are at a 0 V potential. As expected the potential plot is higher in the n region in comparison to the p region (see *Figure 46*), *Figure 47* displays a potential plot with a 1 V potential on the gate.

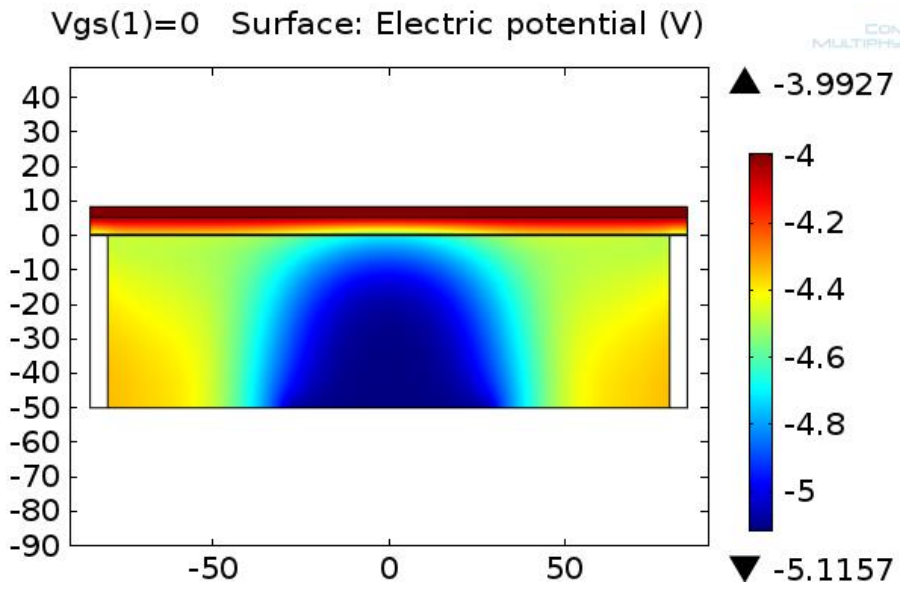

Figure 46 Electric potential at 0 V at the gate

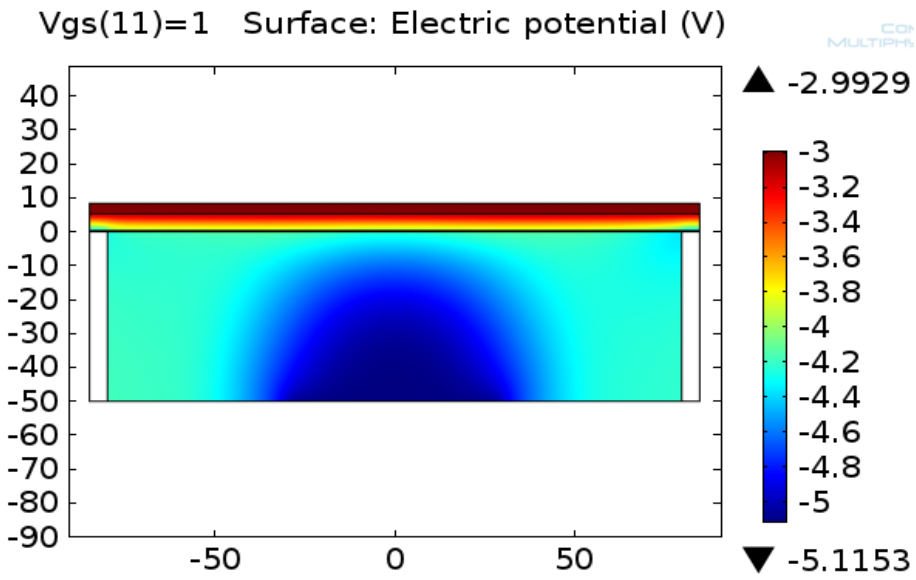

Figure 47 Electric potential at 1 V at the gate

The hole concentration plots display a high concentration in the p region near the graphene layer when compared to the rest of the structure at 0 V at the gate (see *Figure 48*). This changes when a 1 V potential is applied to the gate which the hole concentration is decreased and is mostly visible in the p region (see *Figure 49*). The effects can be seen in the electron

concentration where a 0 V potential is applied at the gate. A large electron concentration can be observed at the gate and in the graphene layer as compared to the rest of the structure (see *Figure 50*). When a 1 V potential is applied to the gate, more electrons diffuse into the graphene layer which increases the electron concentration (see *Figure 51*). The higher the potential that's applied the higher the electron concentration, this increases the conductivity of the transistor. The lower the potential that is applied the higher the hole concentration which also increases the conductivity of the transistor. This is why an equal doping profile is being simulated to attempt to reduce the conductive effects of the holes and the electrons.

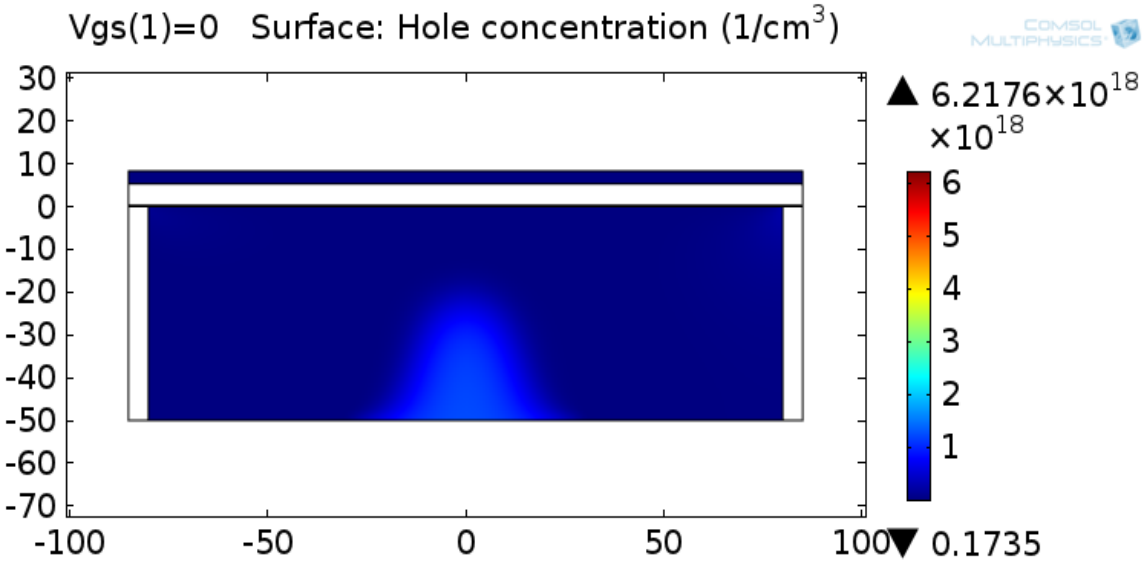

Figure 48 Hole concentration at 0V at the gate

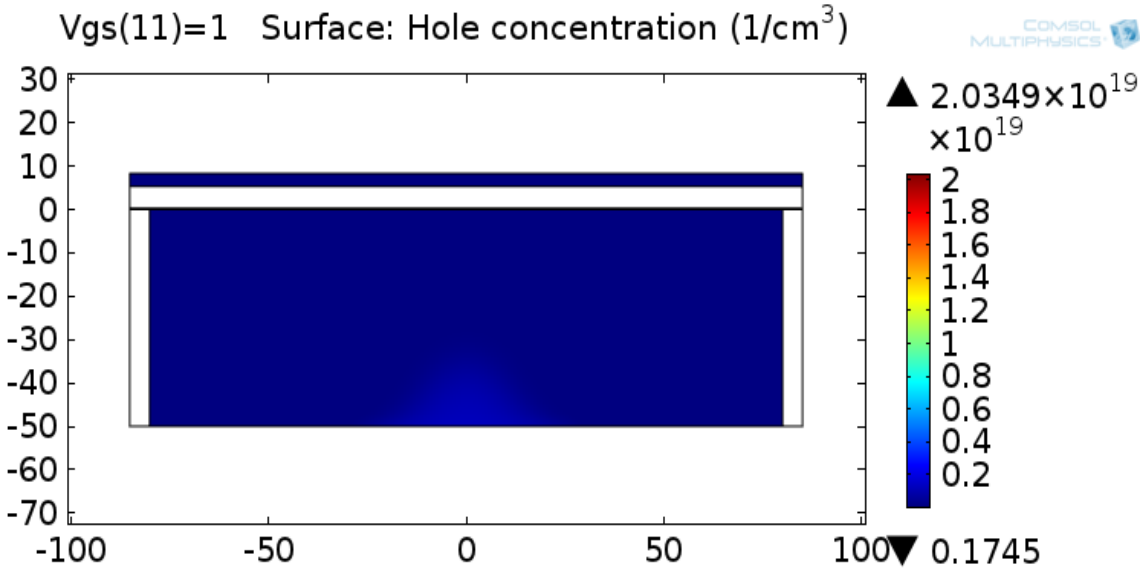

Figure 49 Hole concentration at 1 V at the gate

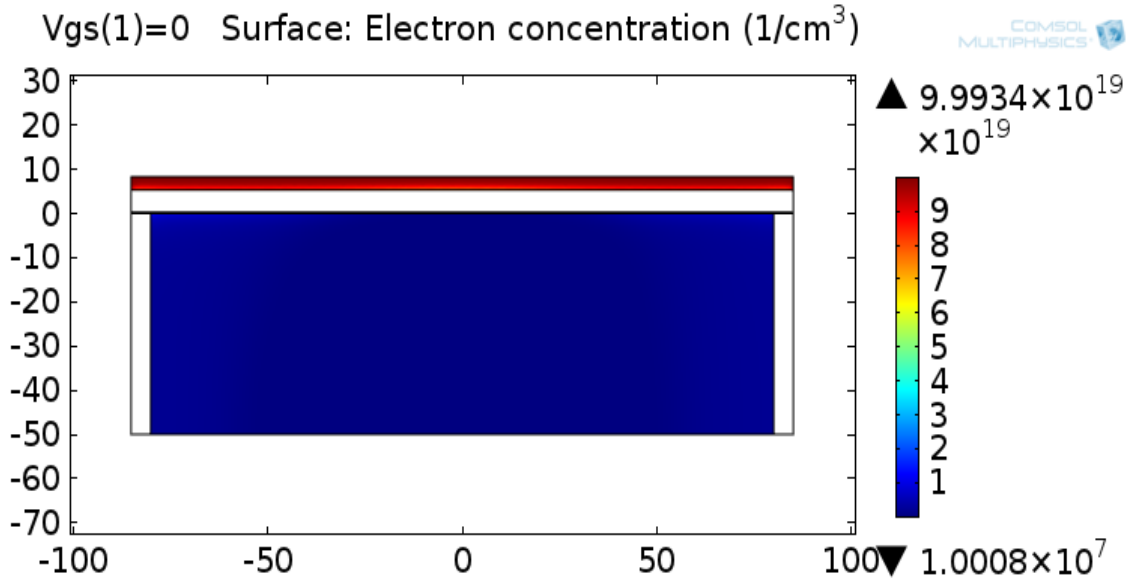

Figure 50 Electron concentration at 0 V at the gate

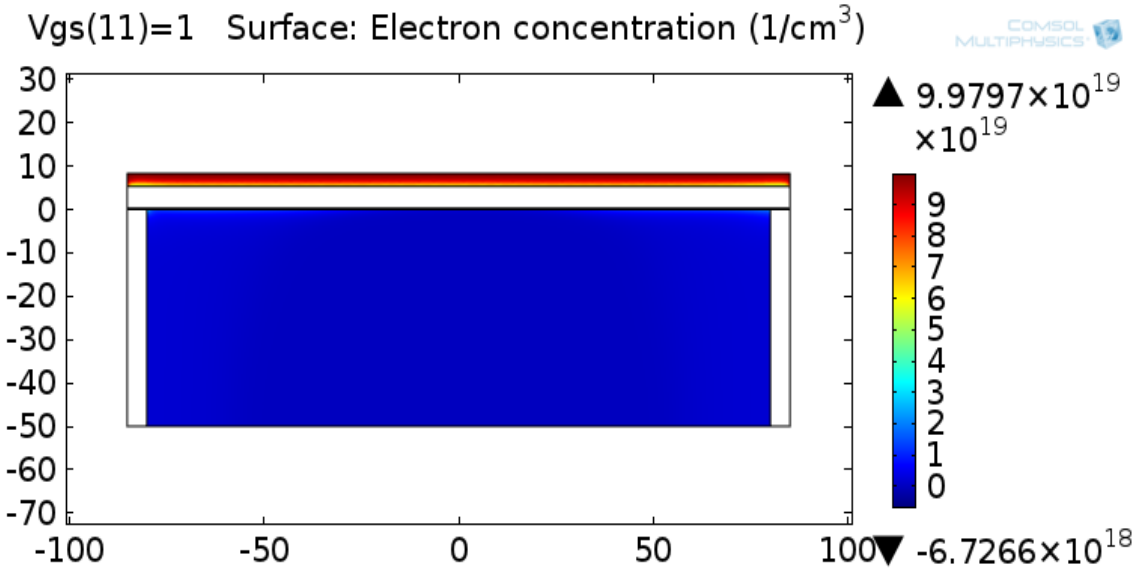

Figure 51 Electron concentration at 1 V at the gate

4.2.2 Energy Band of the doped GBFET. Using the Cut line feature in COMSOL (see Figure 52), the energy band data are plotted, now band bending is visible in the substrate. This band bending displays a depletion region being formed in the substrate near the middle beneath the graphene layer. The band bending is due to the pn junction that is caused by the p and n region's diffusing into its respective region [6]. Figure 53 displays the energy band when the source, drain, body, and the gate have a potential of 0 V applied. Next, Figure 54 displays the energy band with similar conditions except now the gate potential is set to 1 V.

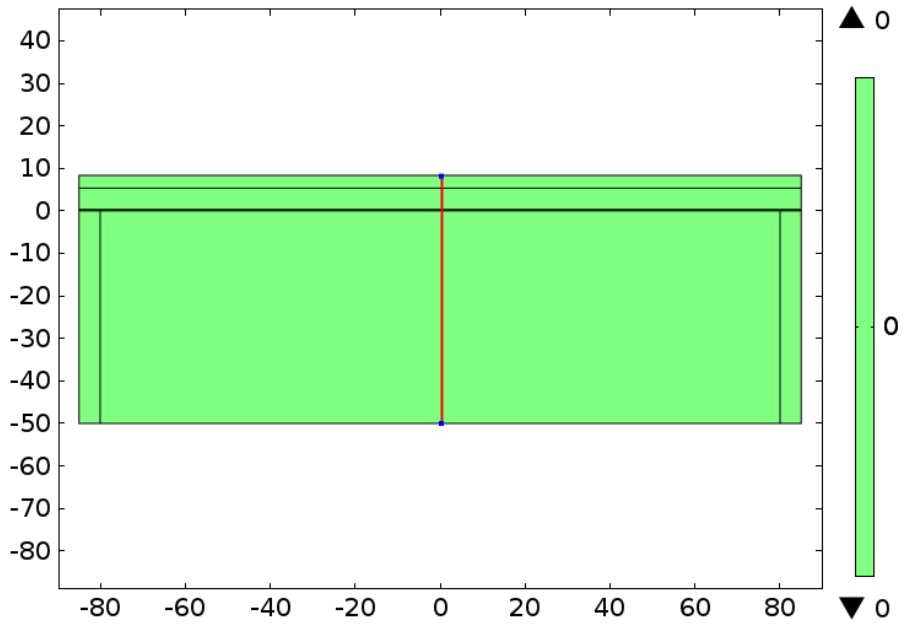

Figure 52 Cut line of the structure

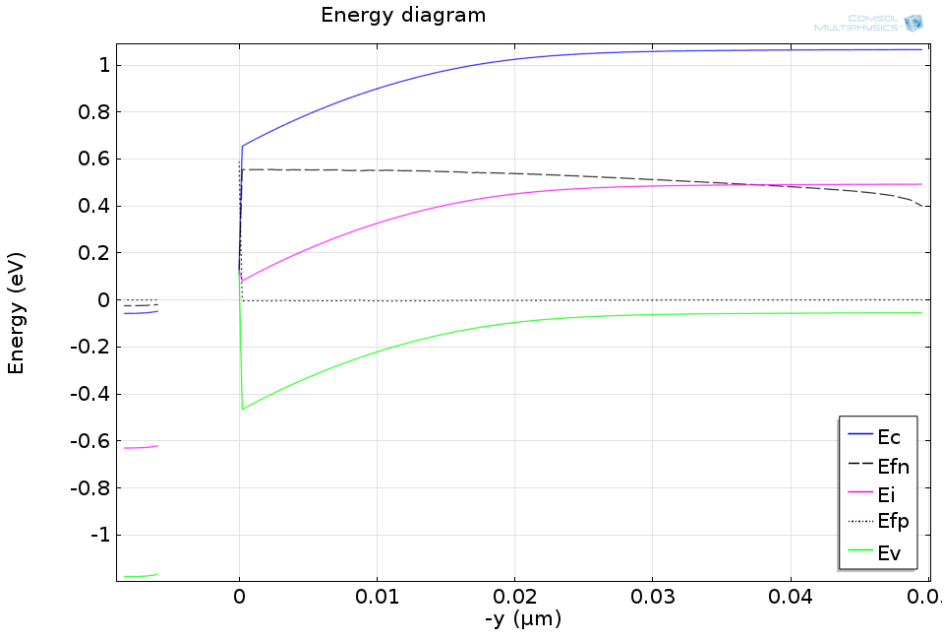

Figure 53 Energy band at 0 V potential at the gate

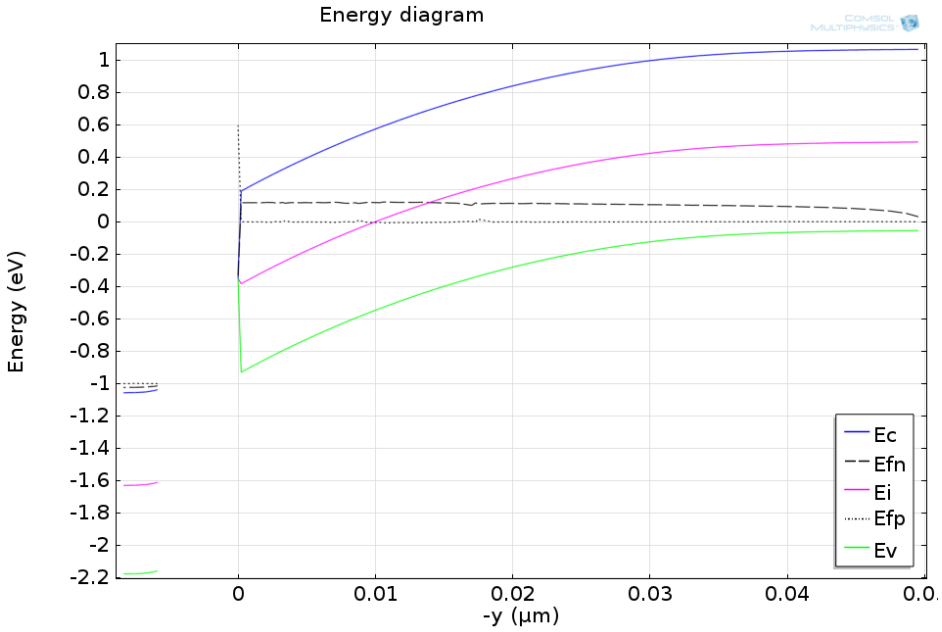

Figure 54 Energy band at 1 V at potential at the gate

4.3 Electron and Hole Concentration inside the Graphene Layer

The size of the current structure being used for this simulation is different in width and height, this makes the Cut line feature harder to align at both ends due to the small size of the graphene layer (see *Figure 55*). In the results below the misalignment can be observed, but is not off by much. Additionally, COMSOL plotted multiple mesh points on one point due to the small mesh size which is dense in the graphene layer. As anticipated from the earlier simulation the electrons are being attracted to the graphene layer from the silicon due to the potential at the gate (see *Figure 56* and *Figure 57*). The opposite effect is occurring with the holes inside the graphene layer where the hole concentration is being reduced with the different potential that is applied at the gate (see *Figure 58* and *Figure 59*). *Figure 62* displays the sum of the electron and the hole concentration which is plotted against the gate potential. Using this plot the on/off ratio

can be observed, note the change from a V shape to a U shape. This plot validates the improvement in the on/off ratio.

Furthermore, due the heterogenous effects created by the graphene and silicon it is imperative to display the depletion region in the substrate. *Figure 60* and *Figure 61* displays the electron concentration at the top of the silicon layer to observe the depletion region, as expected there is a depletion region [17]. In the plots below multiple data points are being plotted thus the plot is not just one line.

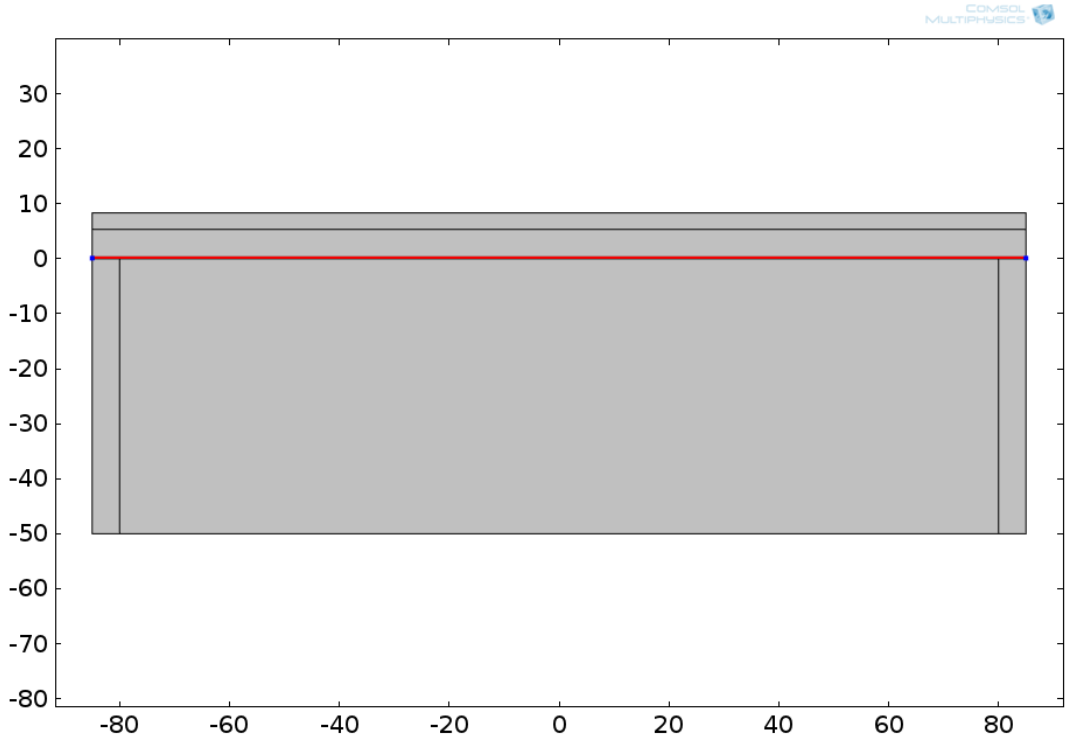

Figure 55 Cut line of the graphene layer

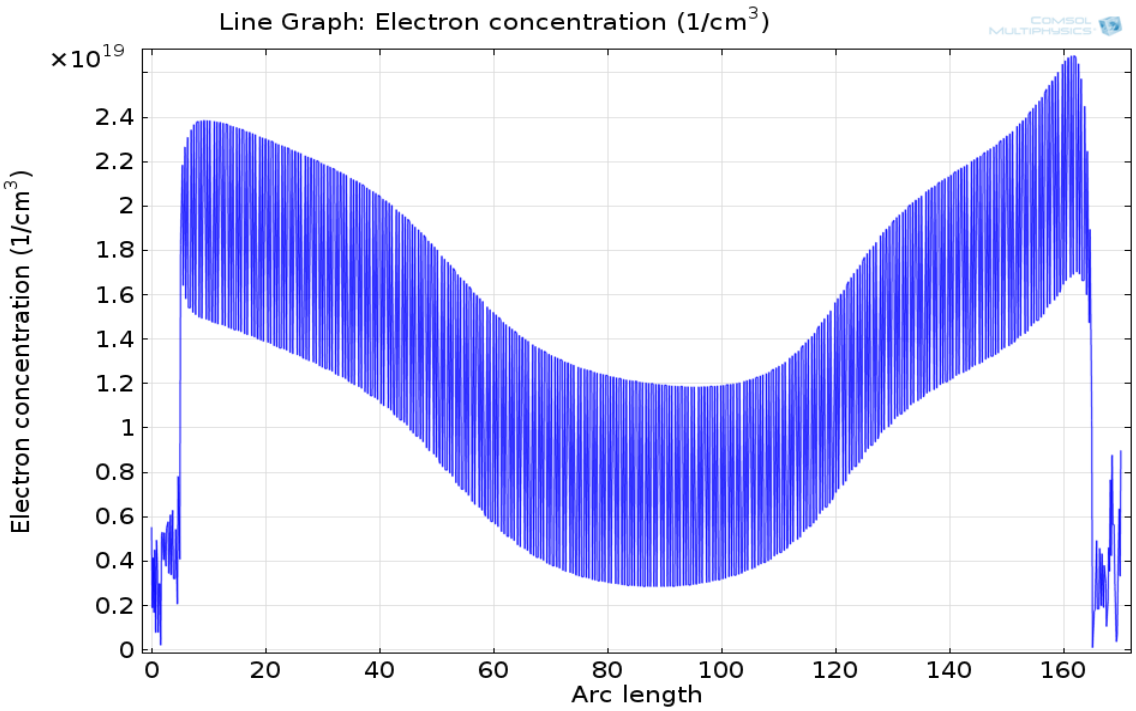

Figure 56 Electron concentration at 0 V potential at the gate

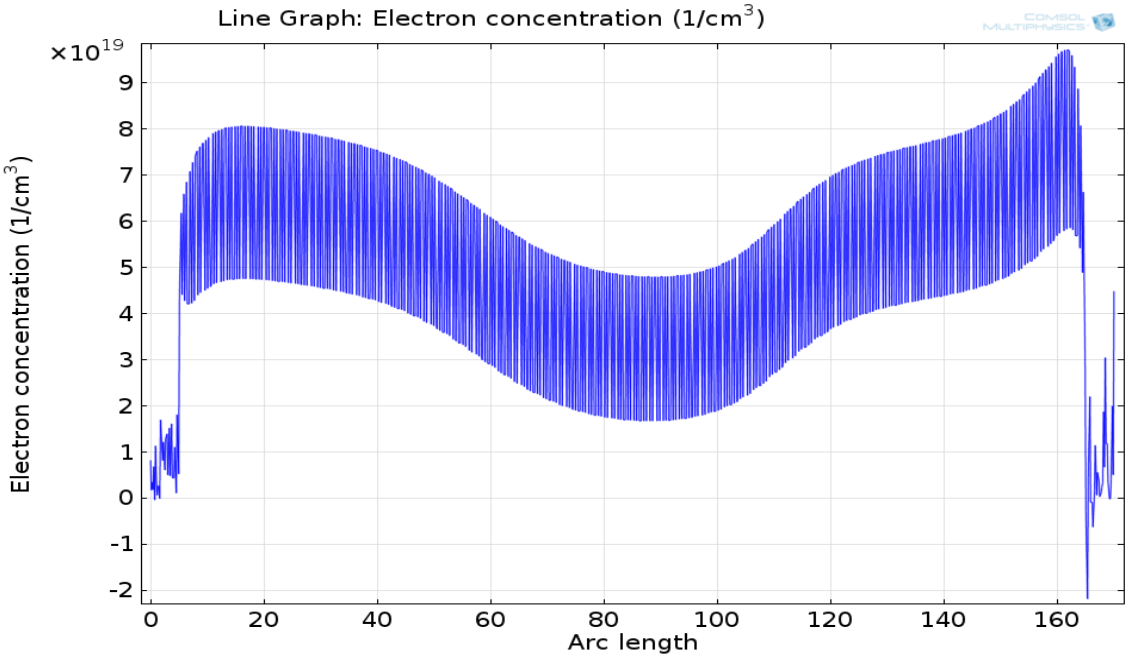

Figure 57 Electron concentration at 1 V potential at the gate

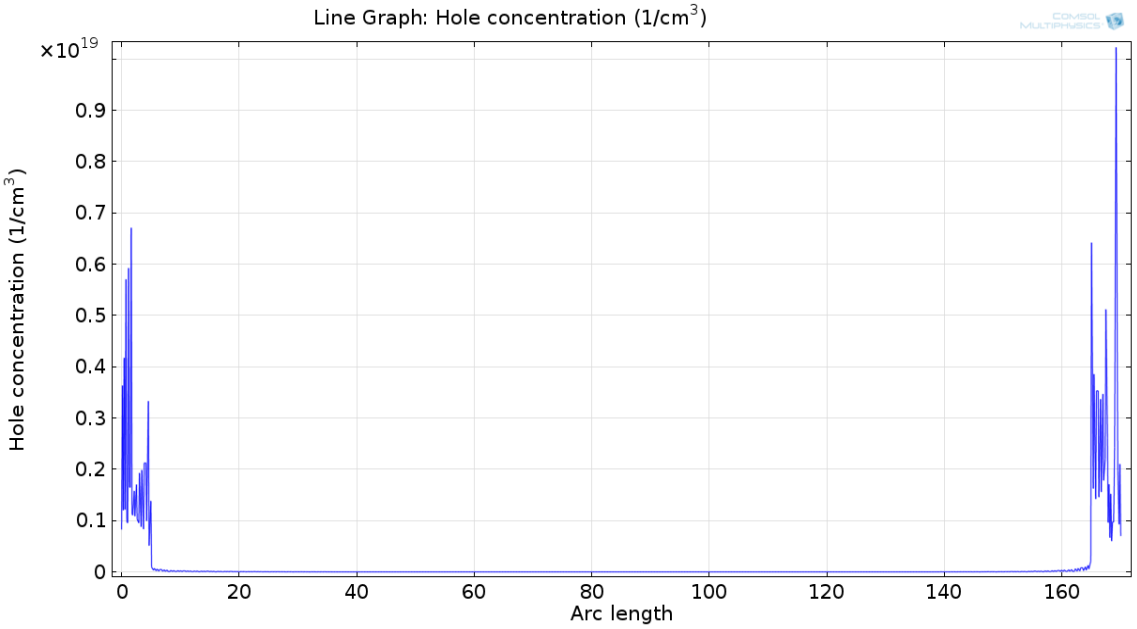

Figure 58 Hole concentration at 0 V potential at the gate

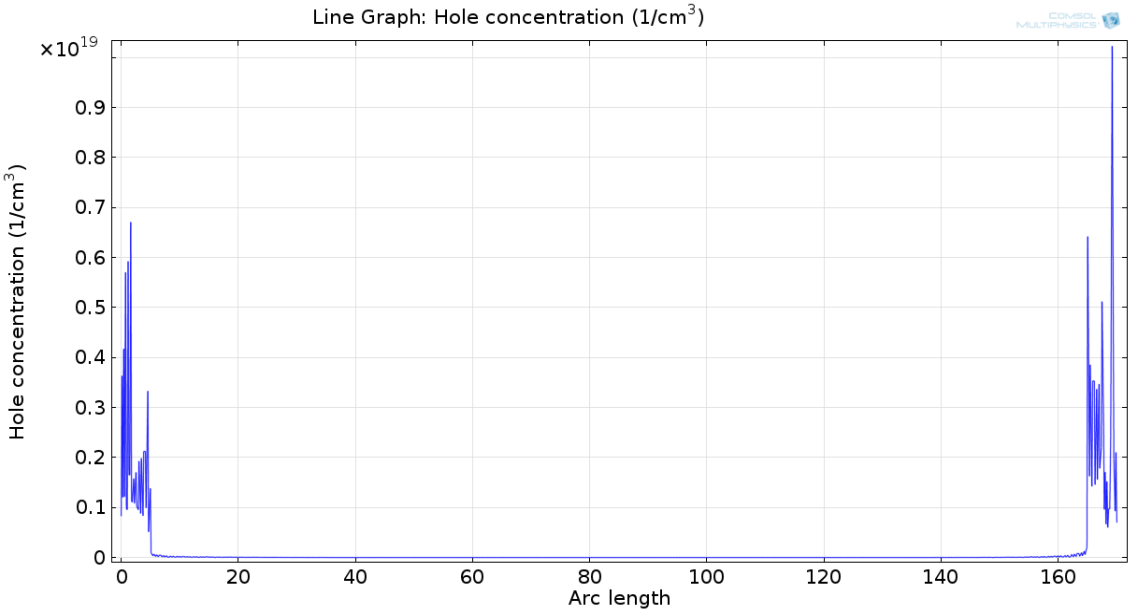

Figure 59 Hole concentration at 1 V potential at the gate

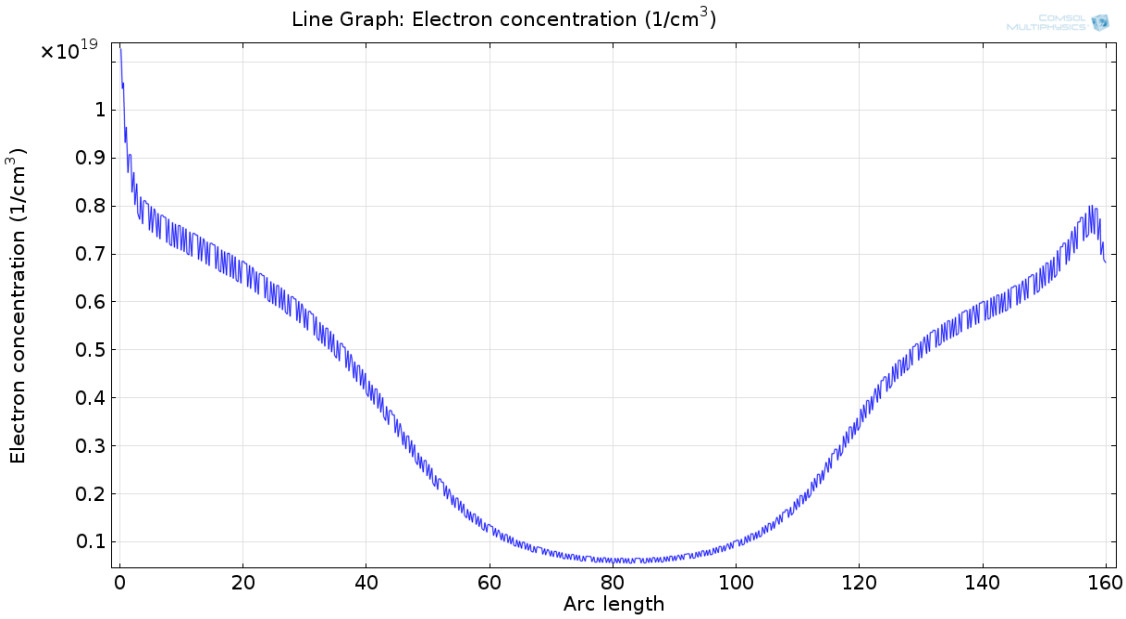

Figure 60 Electron concentration in the substrate at 0V at the gate

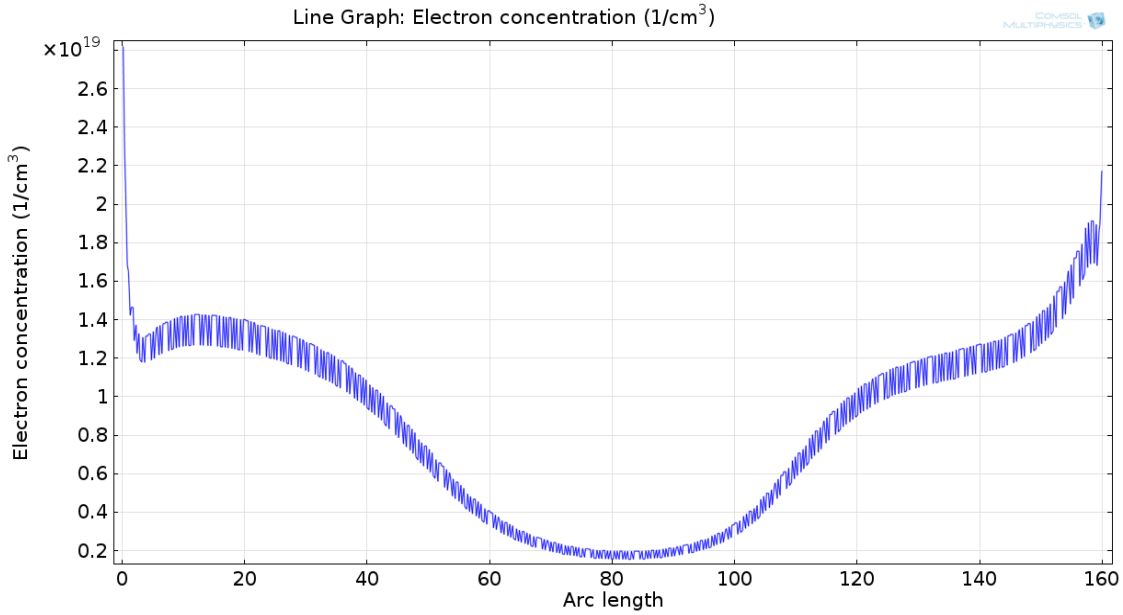

Figure 61 Electron concentration in the substrate at 1V at the gate

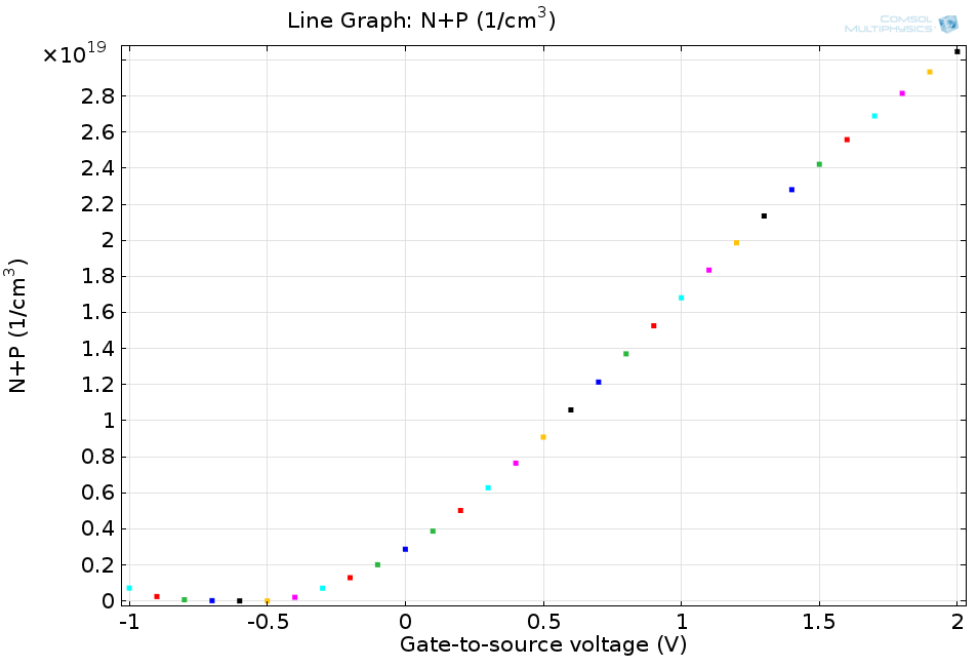

Figure 62 Electron and hole concentration plot

Additional sweeps were performed using different doping concentrations to find the optimum doping profile. The different doping concentrations that were simulated are higher concentrations which a creates a larger barrier. This larger barrier can be beneficial in creating a low and wider off region. This larger barrier ultimately improves the on/off ratio of the transistor. These additional simulations are focusing on the summed electron and hole concentrations to observe the on/off ratio. In *Figure 63*, *Figure 64*, and *Figure 65* displays the doping profile and the electron/hole sum with ND=NA=4E18 1/cm^3. An improvement in the on/off ratio can be observed with this higher doping concentration. Lastly, *Figure 66*, *Figure 67*, and *Figure 68* displays a similar analysis with a higher doping profile of ND=NA=8E18 1/cm^3. This higher doping profile provides an even better on/off ratio, which is caused by creating a larger barrier to restrict the conductivity.

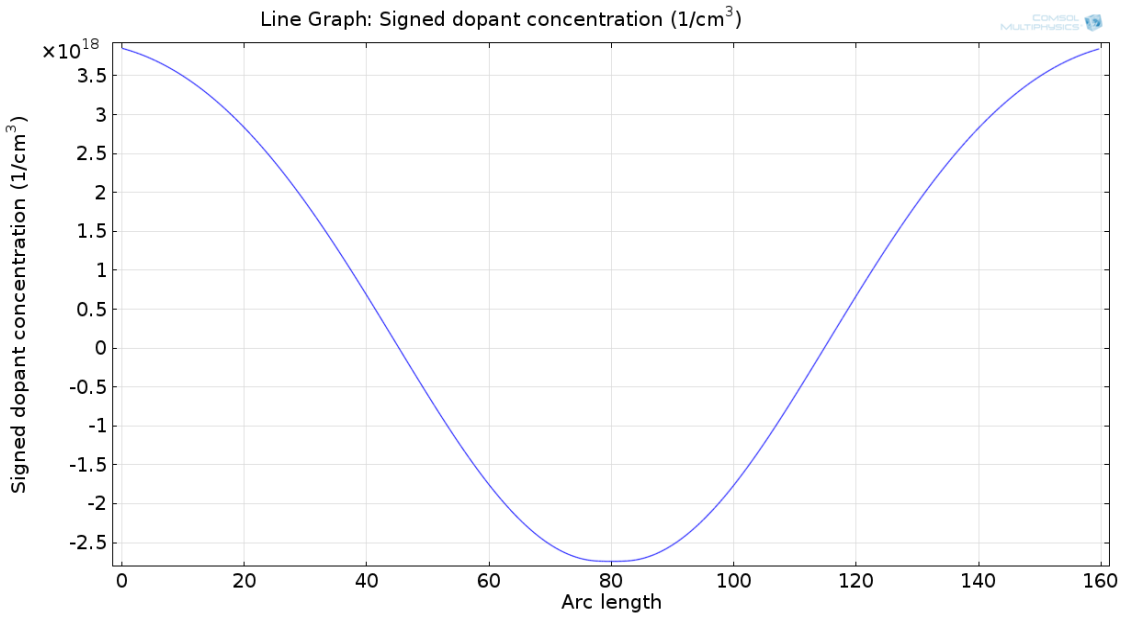

Figure 63 NA=ND=4E18 1/cm^3 doping profile

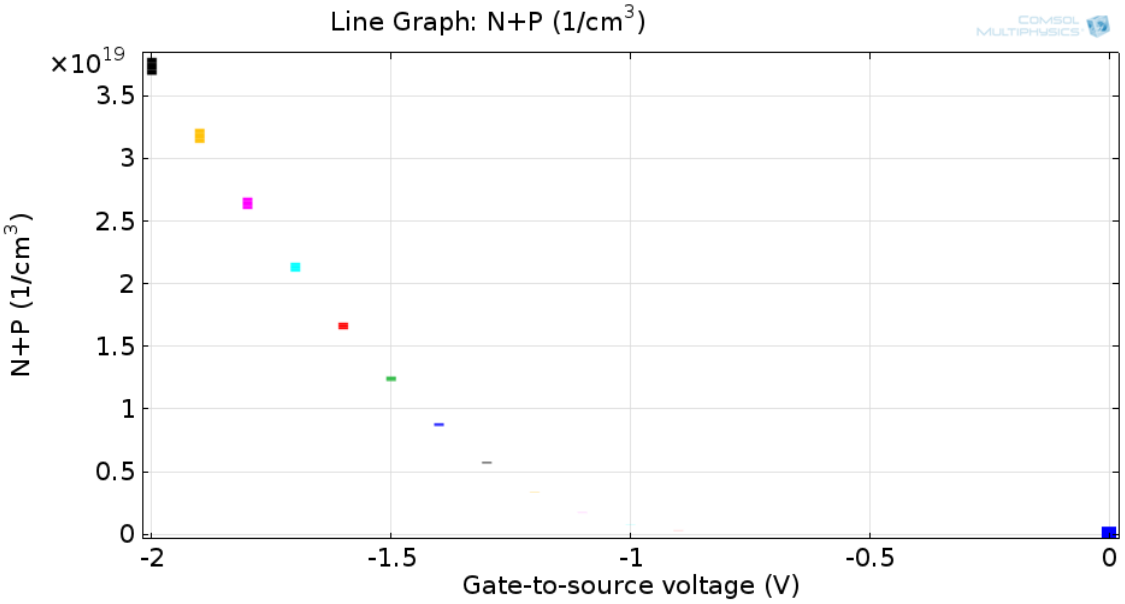

Figure 64 Electron and hole concentration sum vs gate sweep from -2-0V

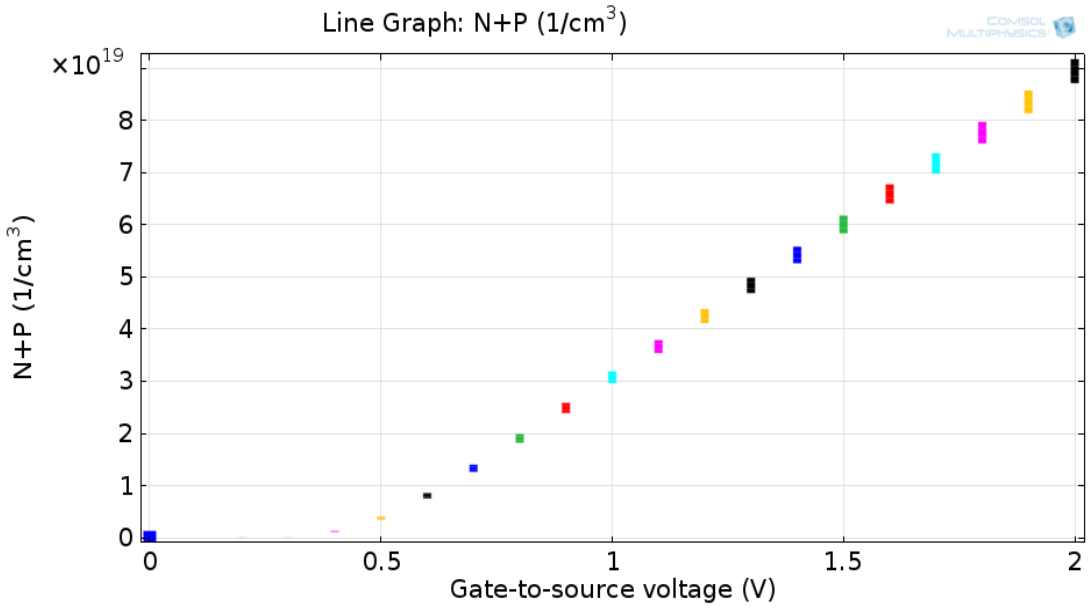

Figure 65 Electron and hole concentration sum vs gate sweep from 0-2V

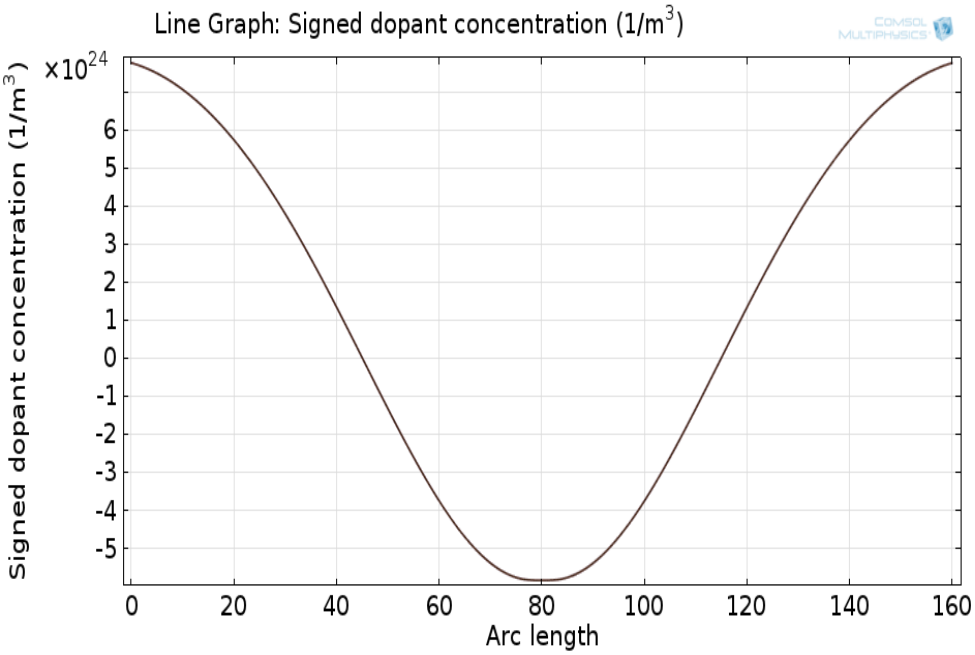

Figure 66 NA=ND=8E18 doping profile

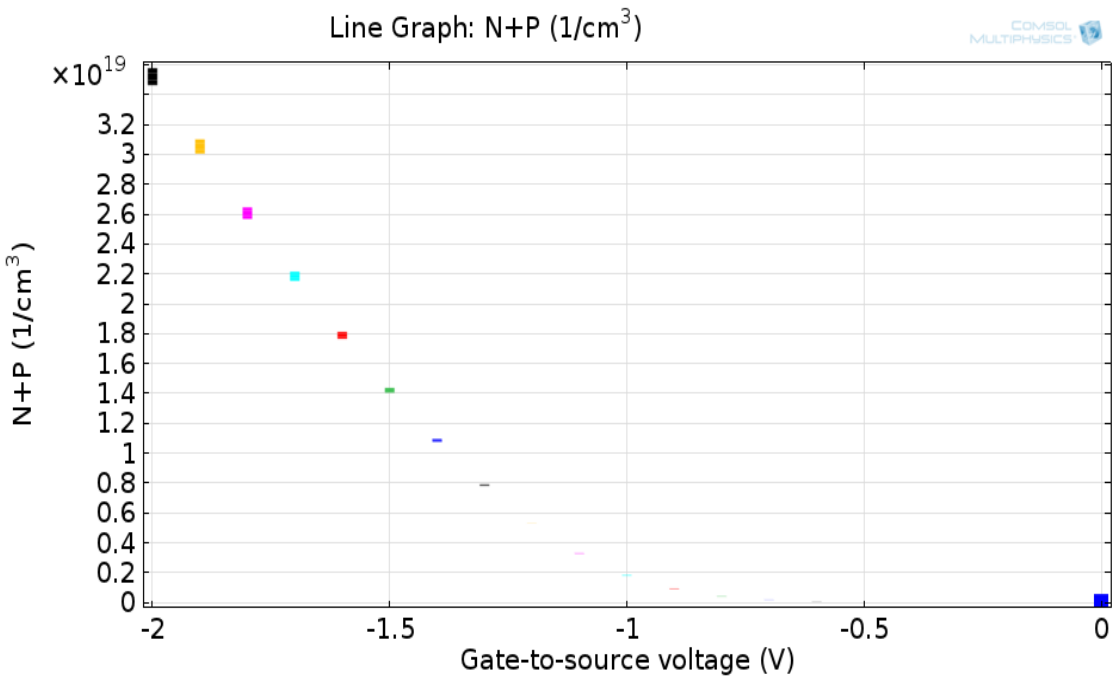

Figure 67 Electron and hole concentration sum vs gate sweep from -2-0V

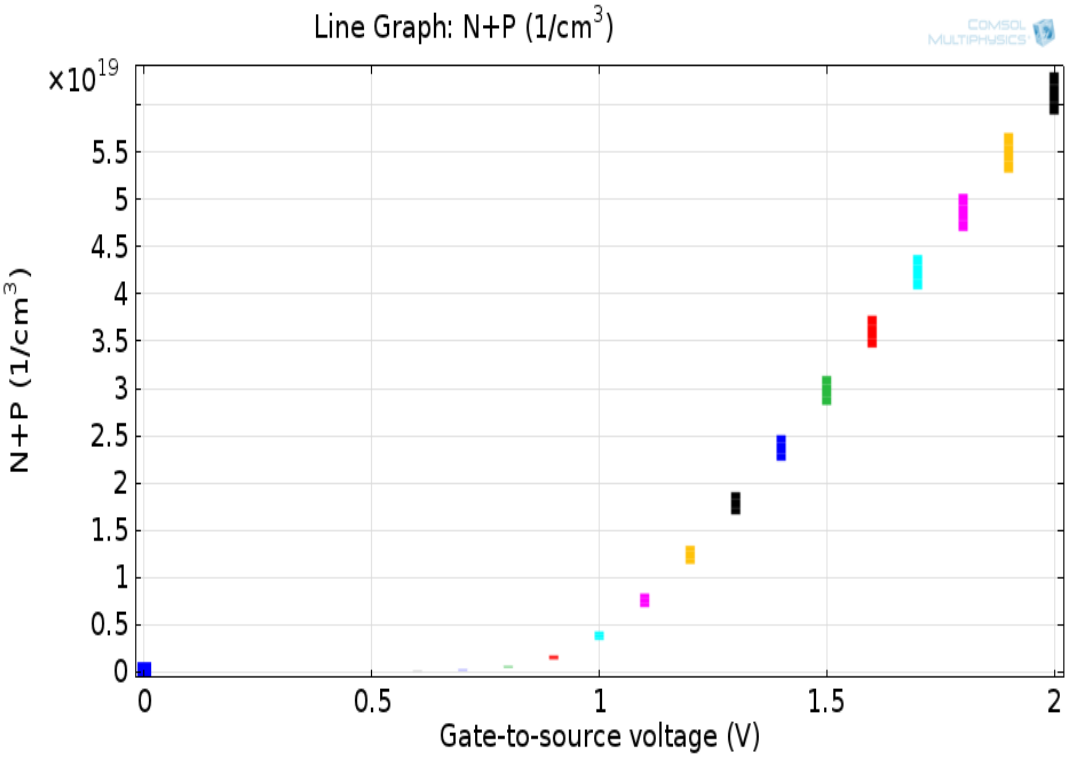

Figure 68 Electron and hole concentration sum vs gate sweep from 0-2V

CHAPTER 5

Conclusion and Discussion

The objective is co-integration of silicon and graphene to design a high performance transistor with a wide on/off ratio to be used in serveral applications. The goal was achieved where a GBFET was created and simulated using a unique doping profile. Additionally, the GBFET was modified to improve the on/off which gives it the potential to be used in more electronic applications. Initially, when the transistor design was simulated, it demonstrated a very narrow off region. For practical application such a narrow off region is not desired and thus needed to be improved. Through the unique doping profile of the transistor, the off region was improved to resemble more of a “U” shape. This same shape can vary in width depending on the doping concentration of the acceptors and donors. However, there is a limitation on how much the silicon substrate can be doped by. This wider off region allows for uses in the RF and Analog arena where the on/off ratio is not too critical. There is still room for improvement of the transistor design to achieve a true off state which would bring this transistor into the digital logic arena. Additional simulations were performed with different parameters to characterize the transistor and possibly make better improvements on the current design. A sweep was performed at the drain terminal to observe any possible abnormalities in the carrier concentration. The doping concentration was varied to observe the summed carrier concentration along with any beneficial changes. These additional results can be observed in the Appendix which can also be used for any future research.

COMSOL is a great tool that can be used to model many scenarios, but one issue that was confronted was calculating the terminal current. This issue has been brought to the attention of

COMSOL and it is confirmed that they are aware of the issue. COMSOL is performing intense research to rectify this issue and are pushing to fix this issue soon.

In an effort to appropriately determine the I-V performance of this transistor the terminal current must be computed. In the future, COMSOL should be releasing an update to improve the terminal current computation. This would greatly help in determining potential structural designs and doping profile that would generate a better on/off ratio. Additional improvements to this research would be performing a similar simulation in a three dimensional domain to include the depth. Next, additional research needs to be completed to help the GBFET achieve a similar off state as what silicon offers. An appropriate step would be in growing this transistor to obtain empirical data. This empirical data would provide sufficient data to support the transistor's actual performance. After characterizing this transistor, this transistor should be included in CAD software such as Cadence to design the new wave of faster electronic devices.

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Appendix

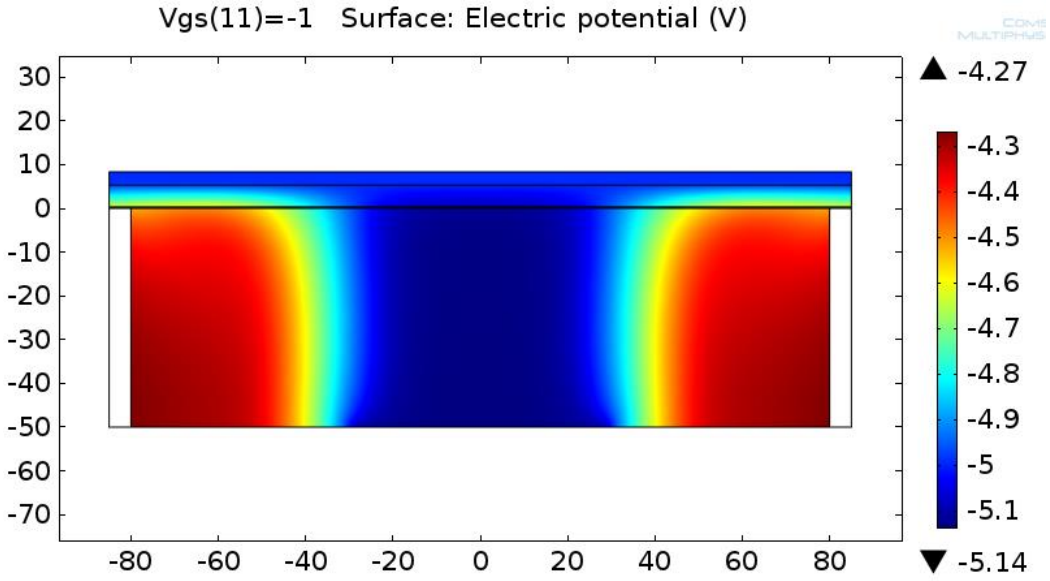

Figure A-1 Electrical potential at Vgs=-1 V, Vds= 0 V and ND/NA= 4E18 1/cm^3

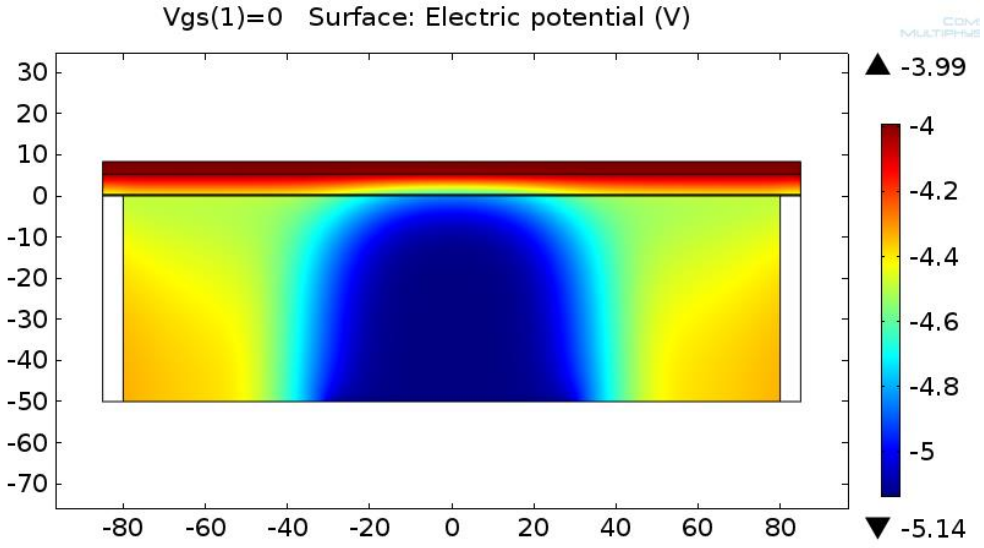

Figure A-2 Electrical potential at Vgs=0 V, Vds=0 V, and ND/NA= 4E18 1/cm^3

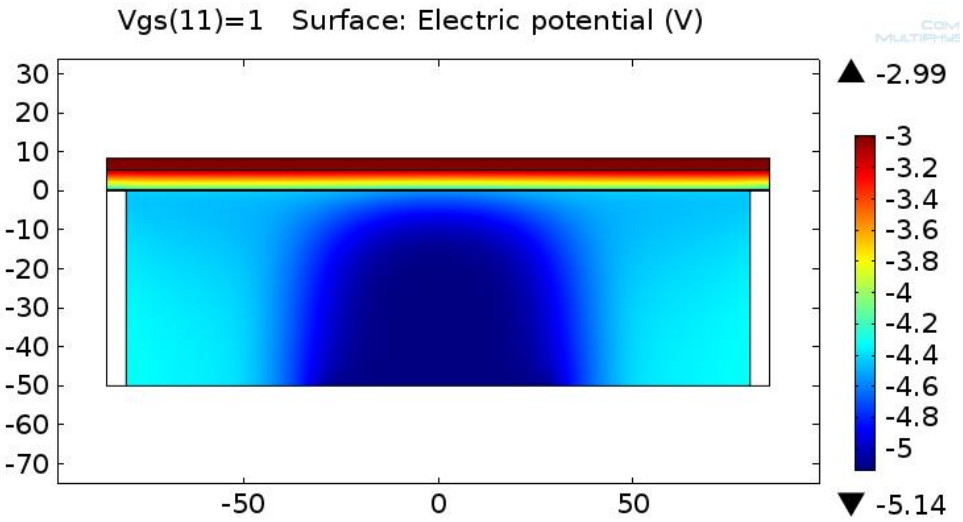

Figure A-3 Electrical potential at Vgs=0 V, Vds=1 V, and ND/NA= 4E18 1/cm^3

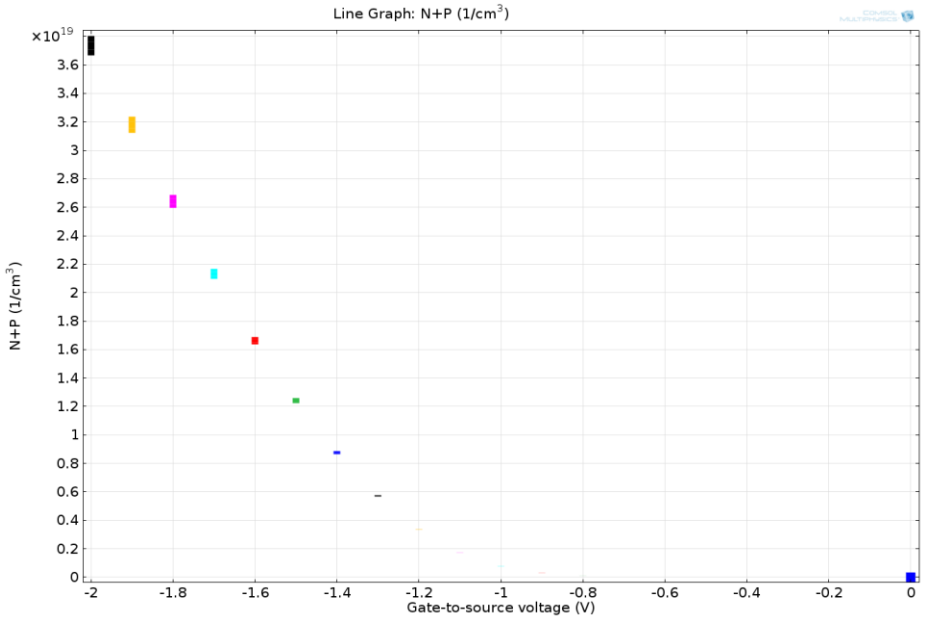

Figure A-4 Electron and hole plot at Vds=0 V and ND/NA= 4E18 1/cm^3

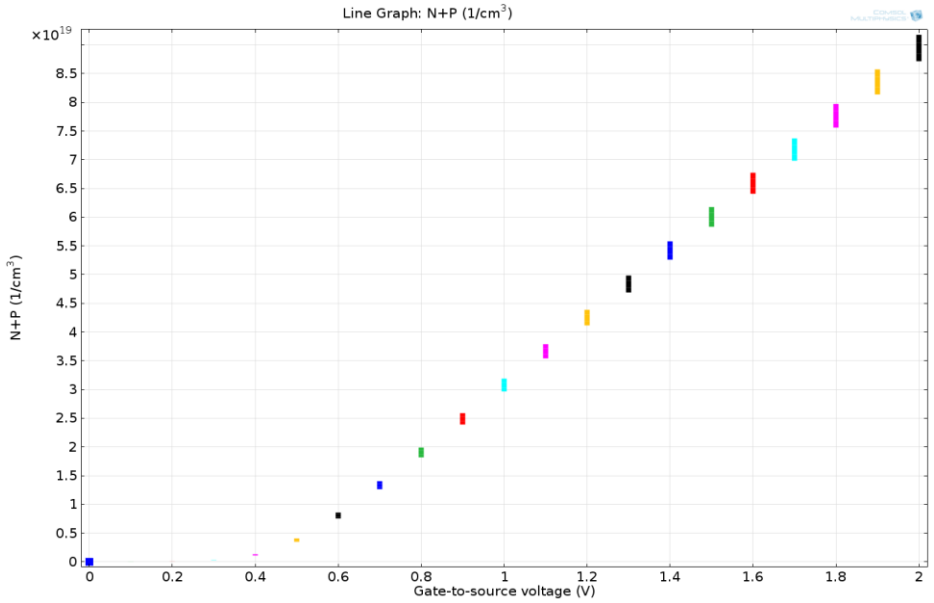

Figure A-5 Electron and hole plot at Vds=0 V and ND/NA= 4E18 1/cm^3

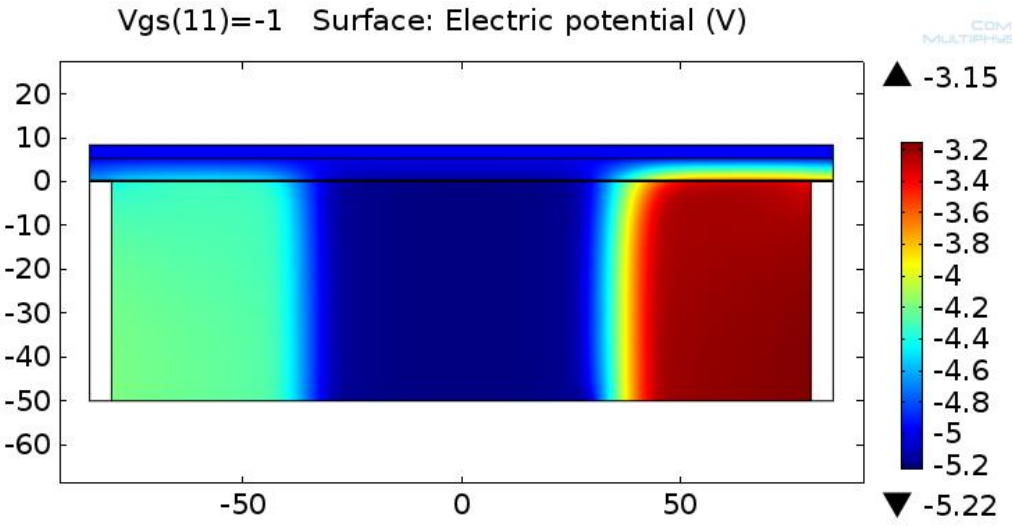

Figure A-6 Electrical potential at Vgs=-1 V, Vds= 1 V and ND/NA= 4 E18 1/cm^3

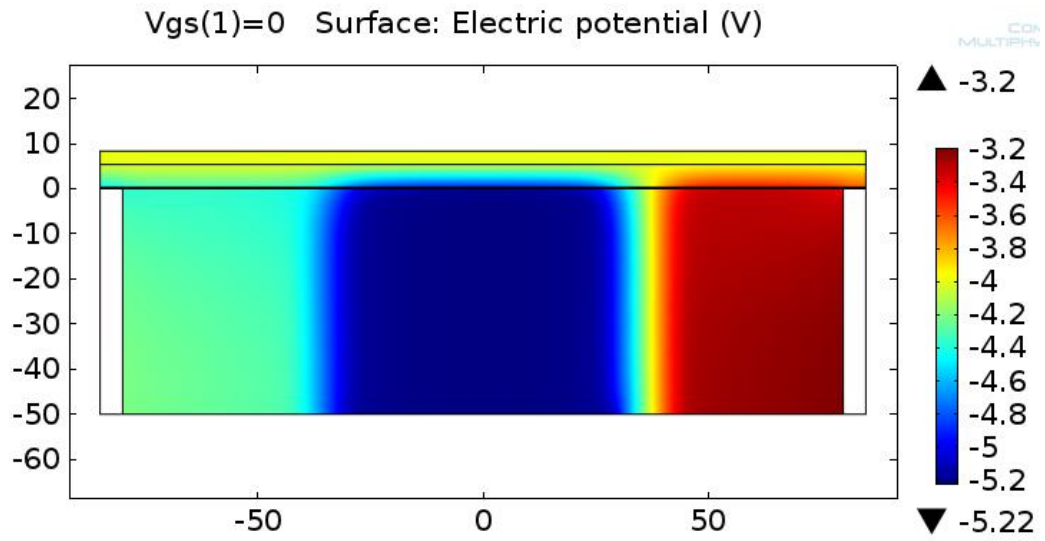

Figure A-7 Electrical potential at Vgs=0 V, Vds= 1 V and ND/NA= 4 E18 1/cm^3

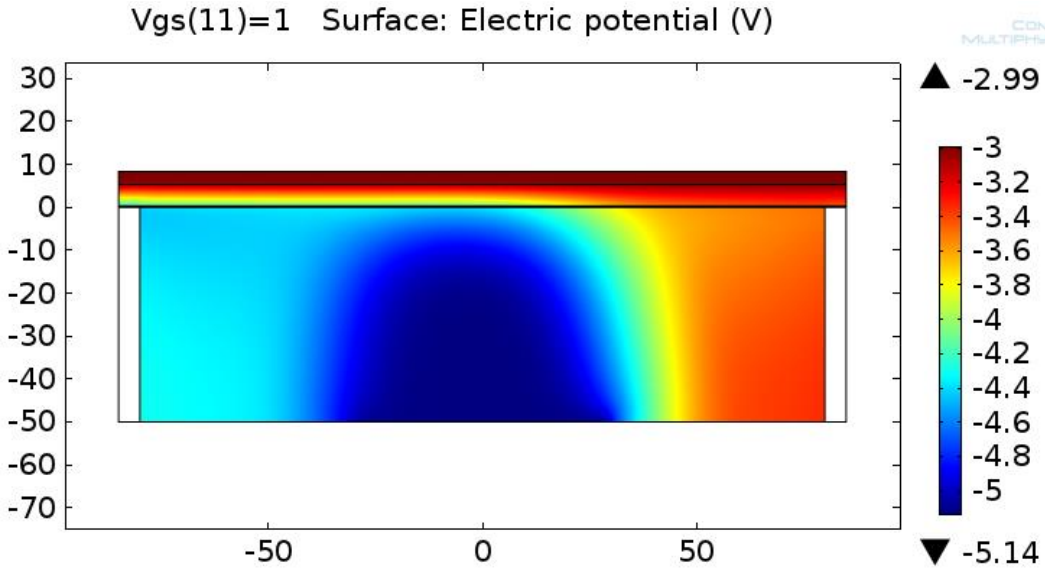

Figure A-8 Electrical potential at Vgs=1 V, Vds= 1 V and ND/NA= 4 E18 1/cm^3

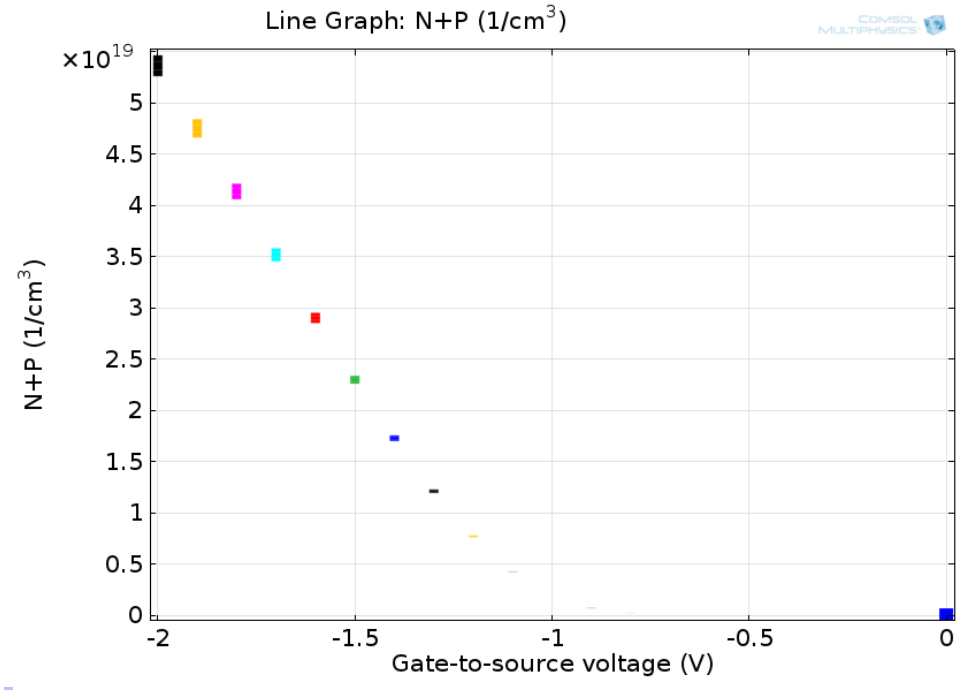

Figure A-9 Electron and hole plot at Vds=1 V and ND/NA= 4 E18 1/cm^3

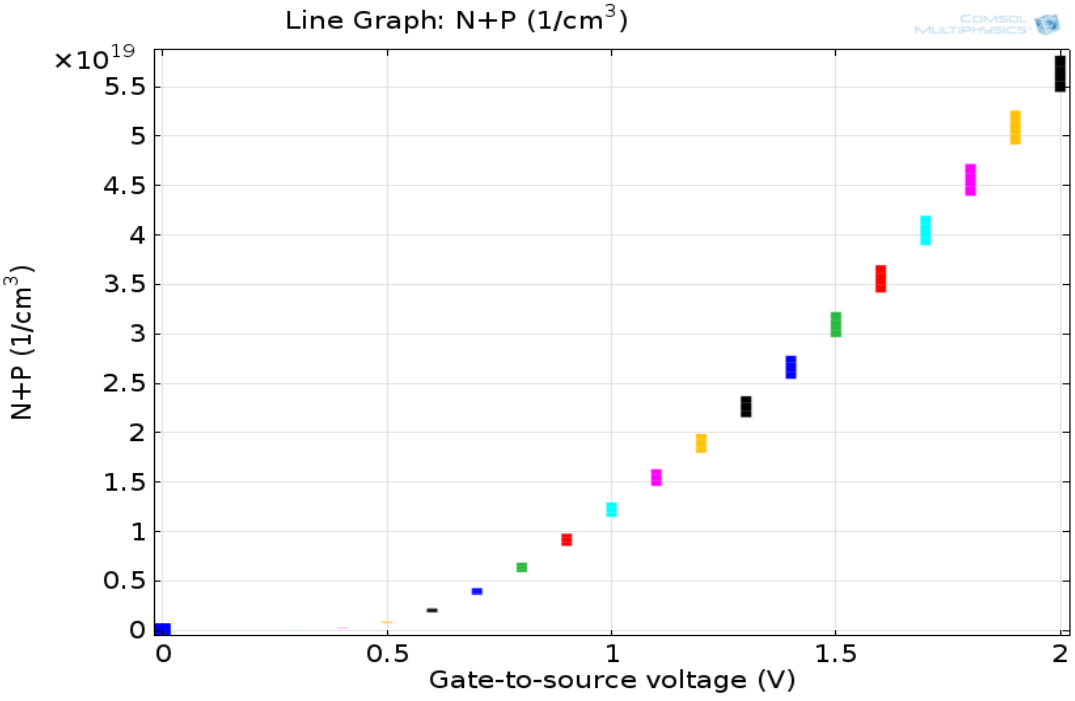

Figure A-10 Electron and hole plot at Vds=1 V and ND/NA= 4 E18 1/cm^3

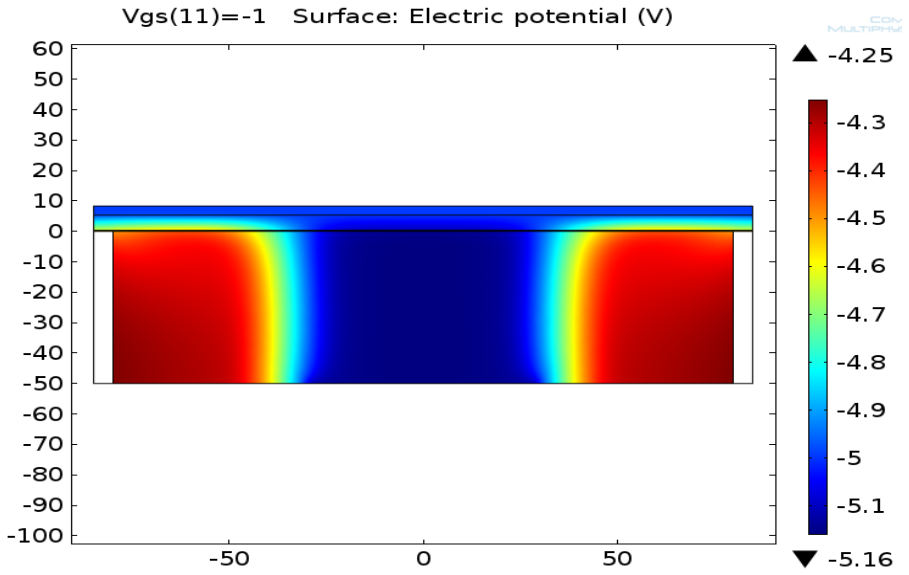

Figure A-11 Electrical otential at Vgs=-1 V, Vds= 0 V and ND/NA= 8E18 1/cm^3

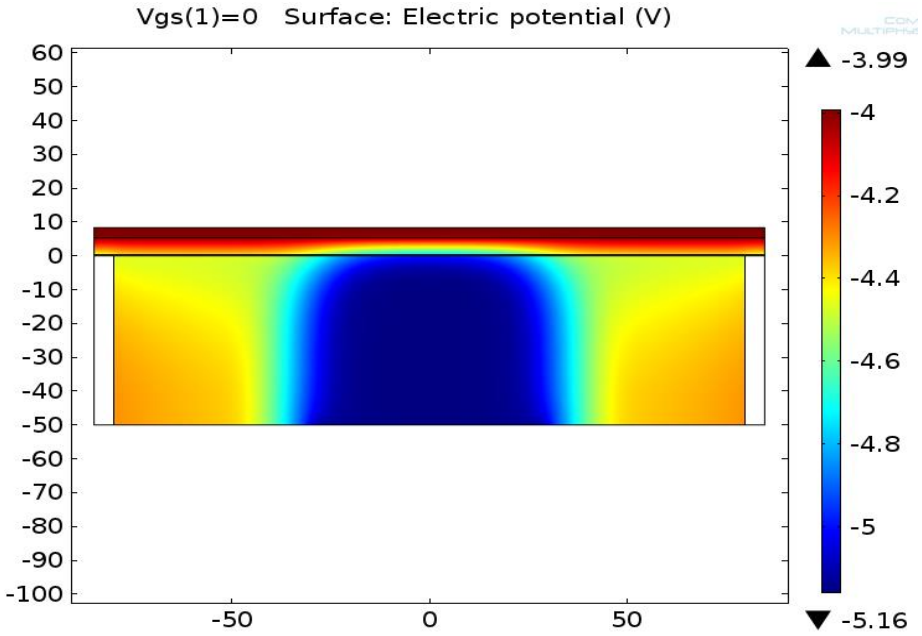

Figure A-12 Electrical potential at Vgs=0 V, Vds=0 V, and ND/NA= 8E18 1/cm^3

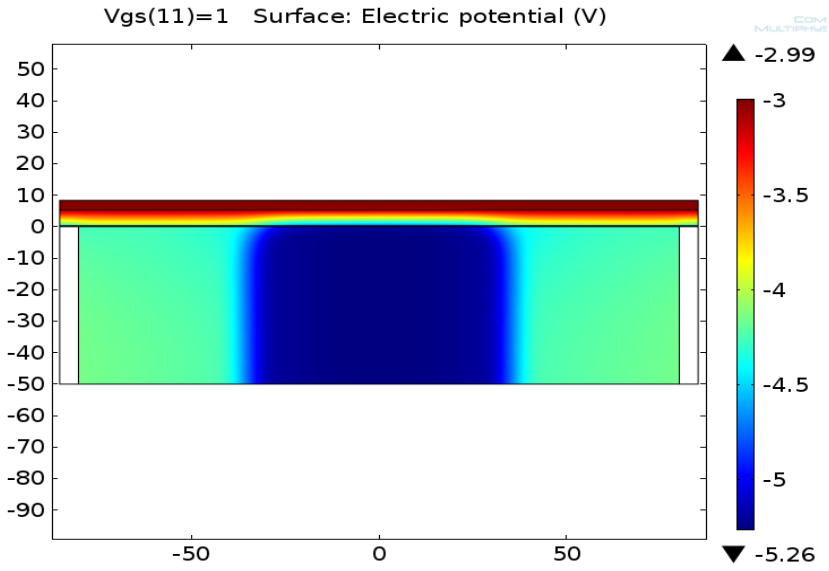

Figure A-13 Electrical potential at Vgs=1 V, Vds=0 V, and ND/NA= 8E18 1/cm^3

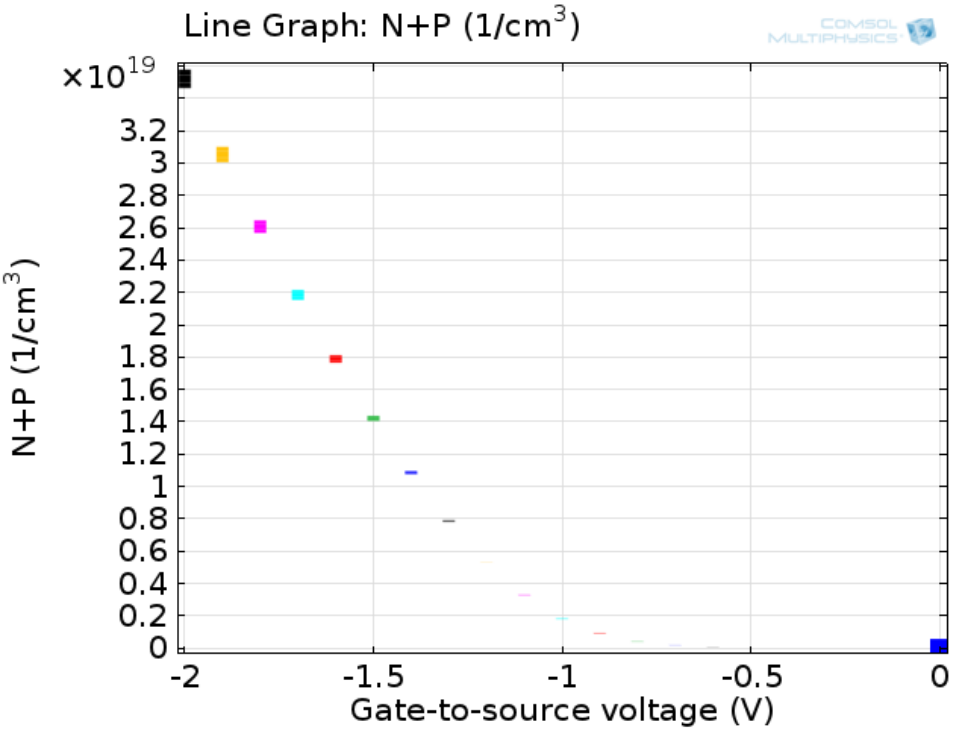

Figure A-14 Electron and hole plot at Vds=0 V and ND/NA= 8E18 1/cm^3

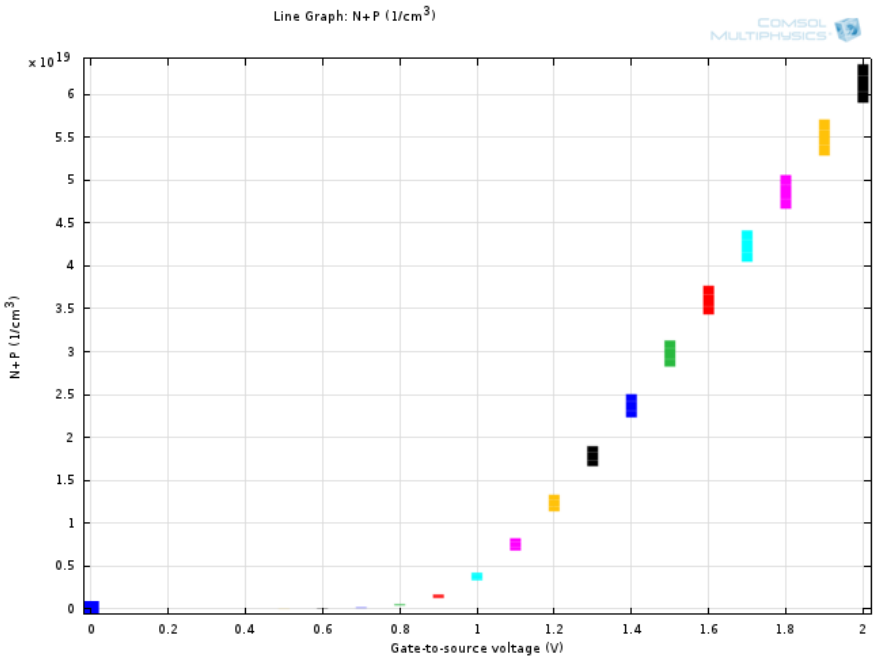

Figure A-15 Electron and hole plot at Vds=0 V and ND/NA= 8E18 1/cm^3

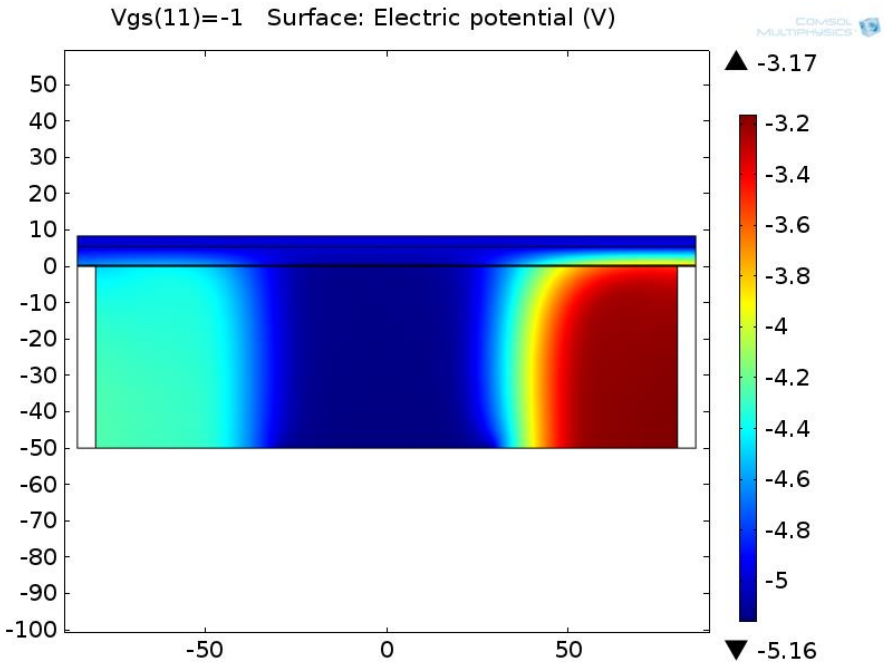

Figure A-16 Electrical potential at Vgs=-1 V, Vds= 1 V and ND/NA= 8E18 1/cm^3

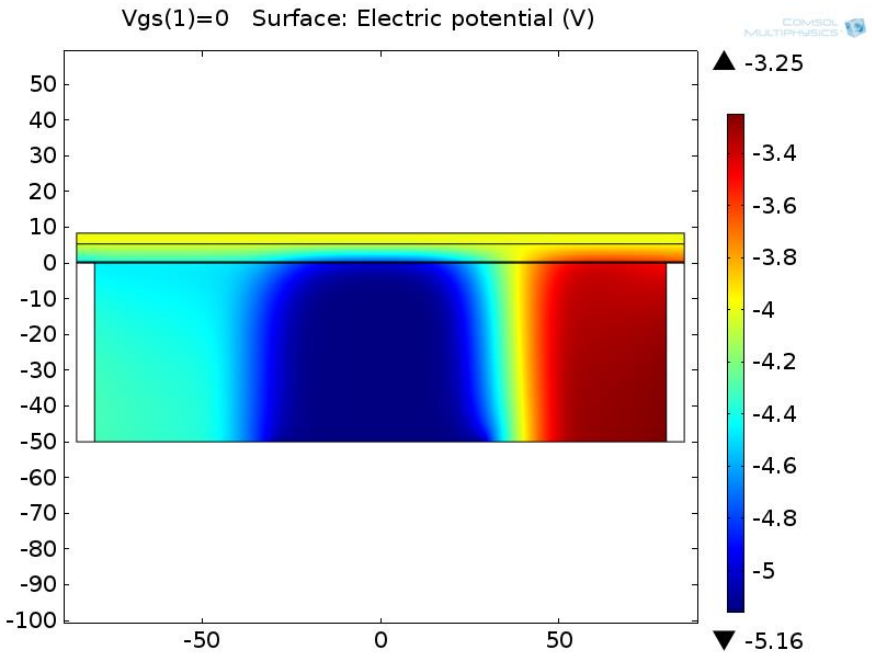

Figure A-17 Electrical potential at Vgs=0 V, Vds= 1 V and ND/NA= 8E18 1/cm^3

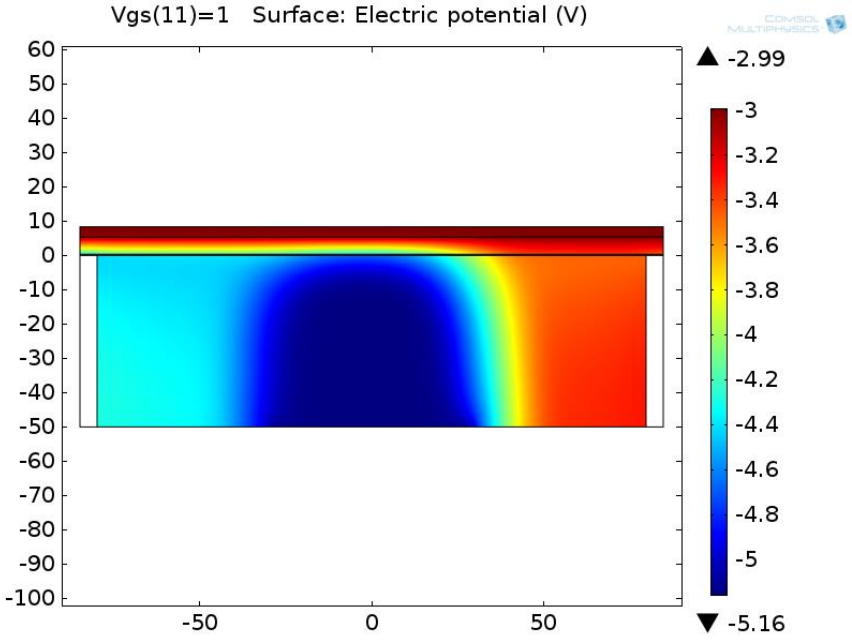

Figure A-18 Electrical potential at Vgs=1 V, Vds= 1 V and ND/NA= 8E18 1/cm^3

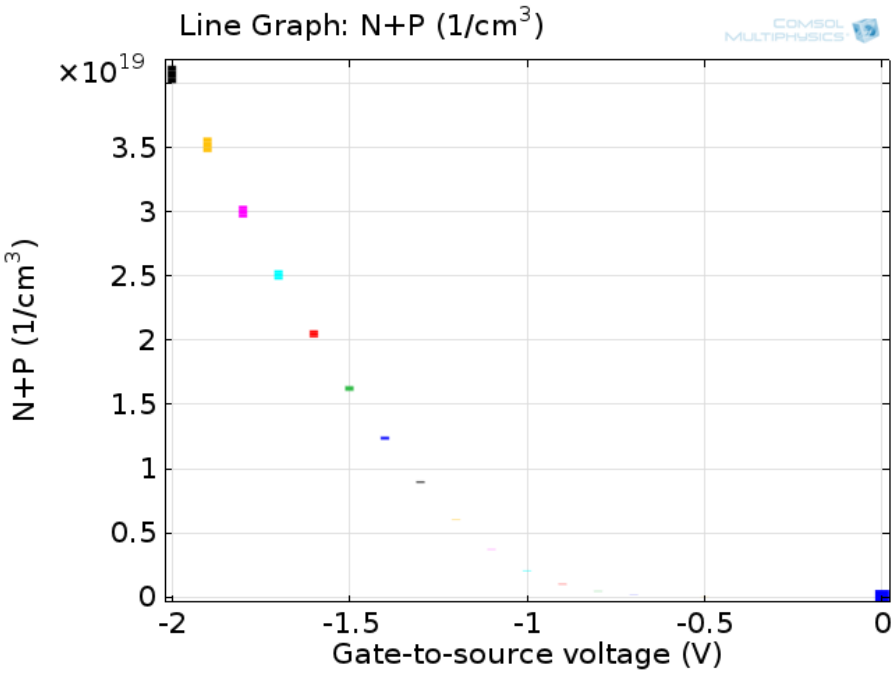

Figure A-19 Electron and hole plot at Vds=1 V and ND/NA= 8E18 1/cm^3

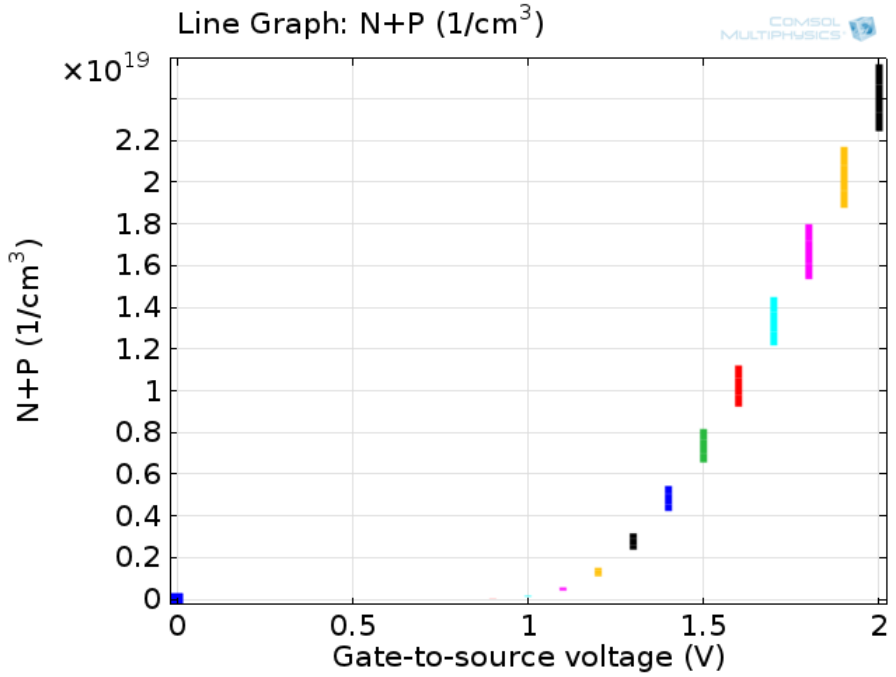

Figure A-20 Electron and hole plot at Vds=1 V and ND/NA= 8E18 1/cm^3